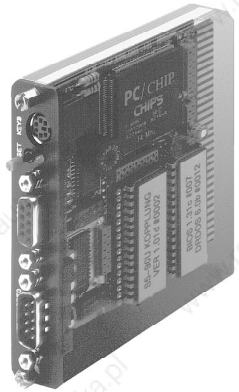
FESTO

The CPU modules
E.IPC- HC15 / HC16 / HC17



- The computer unit of your FESTO IPC concept is software and socket compatible to the world-wide PC/XT standard, operating system MS-DOS 3.3-6.2, DR-DOS 6.0, Novell-DOS 7 or QNX 2.25
- High capacity C&T processor F8680 PC/CHIP (14 MHz, 3 MIPS, Landmark 19) with 16 bit memory access, 1 MB main memory (computing speed comparable to 386SX systems).
- CGA/LCD graphic adapter to connect to screen or LC display.
- Serial interface module (RS232, RS232 opto, RS422, RS485).
- Multiprocessor capable via software controlled decoupling from the PC/XT bus.
- ROM disk with up to 896 KB capacity or RAM/Flash disk with up to 512 KB.
- Secure attachment and high noise immunity thanks to screened electronics in an aluminium housing and electronics design conforming to EMC requirements.
- Any PC compatible computer with CGA, EGA or VGA graphics can be used as a development system.

FESTO

The FESTO IPC concept

Thanks to the modular design of the FESTO IPC concept induvidual system components can be suited to very different areas of application. The system's modularity combines minimal space requirements with high PC capacity and low purchasing and maintenance costs.
Existing systems are freely extendible should requirements increase, but costs are minimised as only modules which are to be used are necessary.
The modularity of the system guarantees minimal logistic requirements as all systems use the same basic building blocks (busboard, CPU, I/O, and communication modules).
Special requirements such as integration into existing field bus systems are not a problem for the FESTO IPC concept. The current range of more than 80 modules fulfils almost every need.
Thanks to the simple and robust plug-in system, users can install or exchange individual components in seconds without the need for dealing with special complex wiring or the removal of the housing. The ease of handling means that the costs and time required for servicing and training are minimised.
The many uses of the modules and the software are not limited to one particular system. They can be rearranged in any combination to develop modified or completely new possibilities for use.
The design of the modules is strictly geared to meet the demands of industry (demonstrated by the durable aluminium housing) and guarantees full compatibility with today's mechanical and electrical environment.
All the main plugs in the FESTO IPC are in accordance with the standard for industrial PCs. The use of expensive special cables with unusual pin allocations has been avoided.

FESTO

The CPU modules E.IPC-HC1X

The Heart of every FESTO IPC concept is the CPU. The PC compatible CPU modules E.IPC-HC1X unite the CGA graphic controller, 1 MB main memory, an integrated serial interface module with RS232 standart adapter (fitted as required with RS422, RS485 or customerspecific), an I²C bus controller and a bootable silicon disk (max. 896 KB) in one housing. This is all controlled by a high capacity single chip processor F8680 (PC/Chip) by C&T. The 16 bit memory access and the modern design put the 8086 compatible processor with 2 MIPS in the same performance class as the 20286 and 80386SX computers. The user has the free choice of the largest software stock in the world.
With the PLC programming systems which are available, LogiCAD, Festo FST and PLC emulator, the CPU module can also be programmed and used like a PLC. Due to decoupling from the PC/XT bus of the busboards, the CPU modules become capable of multiprocessing and can be operated in master/slave mode with other E.IPC-HC1X CPU modules. Here the I²C bus with a transfer rate of up to 90 KBit/s controls communication between the master and slave modules or between external customer-specific I²C modules. Several FESTO IPC concepts can be linked via the external I²C bus within one device or one system.
A hardware watchdog timer, designed for industrial use monitors the running of the program together with the SuperState BIOS adapted to suit the F8680 processor. As the system configuration is stored in an EEPROM and not the usual battery or rechargable battery backup the CPU modules E.IPC-HC1X are truly maintenance-free.
The keyboard socket (for PC/XT compatible keyboards), the freely programmable push button (e.g. useable as a reset push button), the serial interface and the LED status display are easily accessible and clearly labelled on the front of the cast aluminium housing which conforms to EMC requirements.The use of standard connectors, widely used throughout the PC world permits the use of preassembled cables and minimises the amount of wiring required.

FESTO

Contents

Update status

Hardware updates

Serial number	Hardware version	Alteration
as PM924602-20XXXX	H01	Actual version

Notes regarding installation and use

Scope of delivery

The following belong to the scope of delivery of the CPU modules E.IPC-HC1X:

- A CPU module E.IPC-HC10 to E.IPC-HC17
- installation notes
- disk with help programs and software drivers and the ROMKIT program for creating a bootable ROM disk drive (not for E.IPC-HC10).

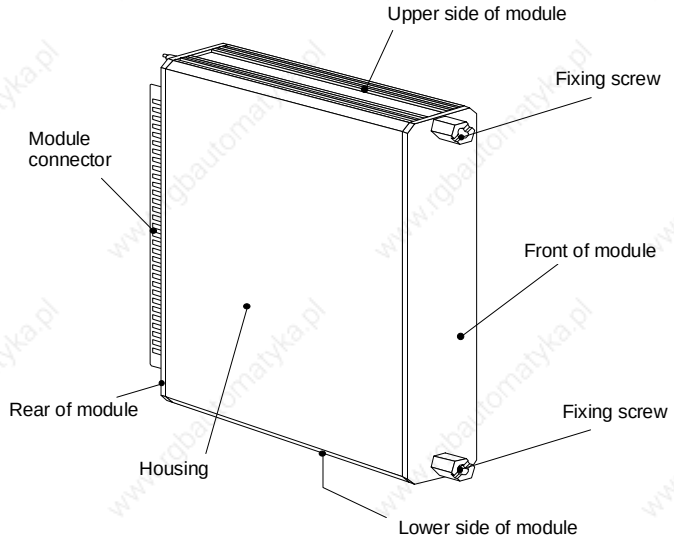
Use and implementation

The modules E.IPC-HC15, E.IPC-HC16 or E.IPC-HC17 are FESTO IPC components, designed for control and visualisation.
The module is intended for use in a FESTO IPC installation only. All modules used must be screwed tightly to the FESTO IPC busboard when in operation and the voltage must be supplied via the E.IPC bus.

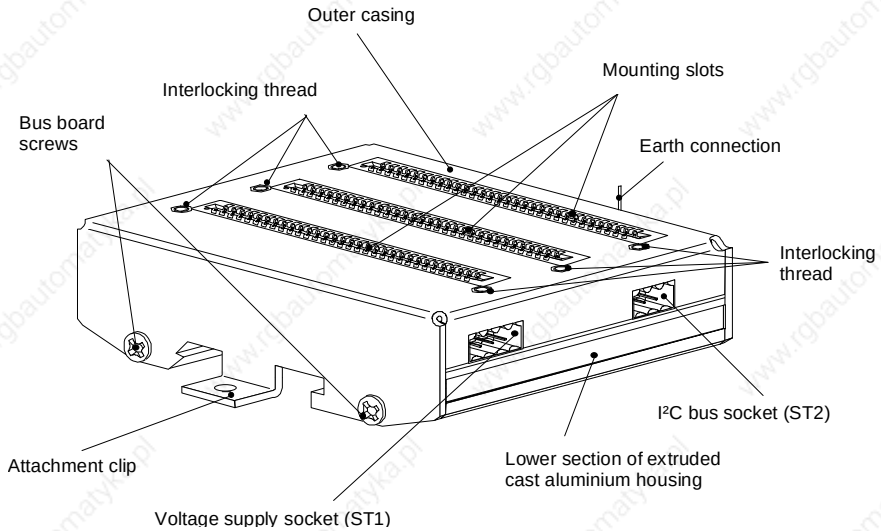
If several CPU modules are being used on the E.IPC bus, then the CPU modules must be set either to “Shared Master Mode” or to “Slave Mode” (please refer to the chapter “The setup menu”). If not, the CPU modules could suffer lasting damage.

If an RGB monitor or an LC display are connected to the video interface of the CPU module, please ensure that the +10 V ... +36 V voltage of the video interface is switched off (please refer to the chapter “The setup menu”). Furthermore, please ensure that the frequency ranges of the RGB monitor or LC display correspond to the frequency ranges of the video output of the CPU module.
Not following these instructions, could cause lasting damage to the connected devices.

The design of a E.IPC module



The design of a E.IPC busboard



The connection of the CPU module E.IPC-HC1X

To install, insert the E.IPC-HC1X CPU module into a free location on your FESTO IPC busboard.

> **Warning:**
>
> Always make sure that all power to your system is switched off before installing your FESTO IPC

In order to guarantee secure attachment, screw the module to the front of the busboard with the two fixing screws provided. While tightening the screws, use one hand to gently press the module into place.

If necessary, now connect the module to the monitor and keyboard with the appropriate cables. In order to conform with EMC requirements, please use screened cables only.
When connecting the cables, please refer to the instructions in the busboard manual and those of the other E.IPC modules and the sections “The keyboard interface” and “The CGA video interface” in this manual.

All modules are integrated into the FESTO IPC installation in this way, in as far as the relevant manuals do not indicate any peculiarities.

Please remember to make a back-up copy of the disks included in the scope of delivery!

Commissioning

When all the cables have been connected, switch on the operating voltage while observing the signal LED of the CPU module. The LED must be active the moment the operating voltage is switched on and go out again after about 2 seconds or flash briefly or, depending on programming, continue flashing at 1 s intervals (watchdog display). In addition, a short audible signal will be sounded after about 5-10 seconds depending on the configuration. If a CGA/RGB screen has been connected, then the switch-on message must be displayed on this. In the case of an LCD or BAS monitor the screen output is not activated until later. If a ROM disk has been installed (e. g. with the Basic systems), the operating system and the user program will now be loaded from the ROM disk drive. Otherwise, a different boot disk drive must be installed (e. g. disk drive or hard disk).
If a ROM disk has been installed, the message '`Diskette drive failure on drive A:`' may be ignored.

Changing the CPU configuration during start-up

The user can influence the starting procedure while the CPU is started by simultaneously pressing the key on the front of the CPU and with a key combination on a connected service keyboard. The somewhat awkward operation of this service function is deliberate and is intended to prevent accidental triggering of these functions, since inadvertent operation could permanently damage your E.IPC system and any components connected.
Any changes in configuration carried out in this way will not be accepted automatically in the parameter EEPROM and are only active until the next starting procedure.
To change the CPU configuration permanently, please use the HC10SET program (see: `HC10SET program`).

Key combinations for activating functions

In order to activate a function, press the CPU key and keep it held down. Now press the ALT key. This too, should be kept pressed down. To complete the procedure press either the V, L, D or C key.

> **Note**: The V, L, D or C keys are to be activated briefly only. On no account must these keys be kept pressed down, since this will cause the keyboard buffer to overflow and prevent the required function from being executed.

CPU key + ALT + V

This activates the +10 V ... +36 V supply voltage on the CGA connection in order to activate a CGA/FBAS converter (E.IPC-CV10), if connected, and to display the screen contents on a connected video monitor (e. g. E.IPC-IB10).

> **WARNING!** The supply voltage may only be activated if an appropriate adapter is connected to the CGA output of the CPU. With any other connected screens, the voltage supply may cause permanent damage.

CPU key + ALT + D

This switches to LCD operating mode for the LC displays E.IPC-DIS1/DIS2.

CPU key + ALT + L

This switches to LCD operating mode.

CPU key + ALT + C

This switches to CRT operating mode.

CPU key + ALT + M

Switches to master operating mode. For this the operating mode "ISA-BUS: Share (MST)" or "Shared (SLV) and the operating mode HC1X Key: Master/Slave must be set in the

BIOS SETUP menu.

CPU key + ALT + S

Switched to slave operating mode. For this the operating mode "ISA-BUS: Share (MST) or Shared (SLV) and the operating mode HC1X Key: Master/Slave must be set in the BIOS SETUP menu.

CPU key + CTRL + ALT + ESC (RESET SETUP)

Deletes the parameter EEPROM and resets the CPU to factory settings. The factory settings can be seen in the two pictures *Setup menu, page 1 and page 2* on the next pages. This key combination can always be actuated (also during operation).

CPU key + CTRL + ALT + SPACE BAR (RESET ROM/RAMDISK)

Deletes the existing combined ROM/RAM disk in the system. All data and modifications in the RAM area of the ROM/RAM disk are deleted. The data in the ROM area are preserved. The effect of this key combination is the same as that of "init RAM: Enable" (see: *SETUP menu, page 2*).

The SETUP menu

During the booting-up procedure (e. g. during the memory test), press the **F2** key on a connected service keyboard to start the SETUP program. You can now access the SETUP menu.

> **Note:** The SETUP menu is a part of the HC1X-BIOS and is stored in the ROM. The configuration changes made will not be stored in the usual way in a battery-backed RAM (as is unfortunately still the case with industrial computers), but completely maintenance-free and permanently in EEPROM.
> If the SETUP menu is activated via the F2 key, a screen or LCD display and a service keyboard (standard PC/XT) must be connected.

Alternatively, the SETUP menu can also be activated during operation by starting the HC1SETUP.EXE program. In this case, the SETUP screen will also be transmitted via a remote maintenance program, if applicable (e. g. Fernterm). After the Setup menu hass been quitted, the CPU will be restarted ("cold start").


```
BIOS v3.00          HC1X System Configuration Utility          SN 000000
                      EXTENDED SETUP PAGE 1 OF 2

Time:                 10:57:21          Shutdown COM1:      Disable
Date:                 Jun 29, 1995      Shutdown CGA:       Disable
                                        Shutdown KEYB:      Disable
Diskette Drive A:     3.5", 1.44 MB
Diskette Drive B:     Not Installed     Software Reset:     Disable
                                        XT-Bus Refresh:     Disable
Base Memory:          704 KB
Expanded Memory:      Disable           Boot Up Sequence:   A:, C:

Additional RAM:       192 KB            Harddisk Drive(s):  Enable HD1X
Optional RAM:           0 KB            HDD Assignment:     Normal

Screen:               Color (80x25)     Standby HD1X-0:     Disable
POD:                  Run all tests     Standby HD1X-1:     Disable

Help line ..................................................................

cursor keys to select entries
+- to change an entry                   PgDn for Extended Setup Page 2
ESC to exit without saving              F10 to save then exit
```

Setup menu (page 1) with factory settings

You can select the individual specifications via the arrow keys (up/down).
You can choose between the various settings with the + and - keys.
You can access the extended SETUP menu with the PgDn key (scroll down). You will find more information on the following pages.
If you wish to exit the SETUP menu and transfer the modifications you have made to the parameter EEPROM, then press key F10. If you wish to exit the SETUP menu without saving the modification, then press the ESC key.

The Settings of the setup menu (page 1)

Time:

This is where you can enter the current time. The format is "**Hour:Minute:Second**" (e. g. 18:45:59). Unlike standard PCs, the real-time clock of the E.IPC system is not in the CPU module. For further details, please refer to the chapter *System clock.*

Date:

This is where you can enter the current date. The format is **"Month, day, year"** (e. g. Feb 13, 1993).

Diskette drive A/B:

Please enter here the type of diskette drives connected, if applicable. Possible settings are:

not installed	no drive
360 KB	360 KB / 5.25"
1.2 MB	1.2 MB / 5.25"
720 KB	720 KByte / 3.5"
1.44 MB	1.44 MB / 3.5"

Even if the disk drive is only connected for service purposes and the system is otherwise operated without disk drive, the drive can still be entered. When the installation is started, brief reference is made on the screen to the missing drive. However, the booting up process is slowed down by an entered, but non-existent disk drive. The ROM or RAM disk drives are not affected by this setting, as these are addressed via their own drivers.

Base Memory:

Here, you can enter the required main memory of the E.IPC-HC1X CPU module. The standard values are 704 Kb without VGA graphics card and 640 Kb with VGA graphics card. The remaining working memory (additional memory) can be used as a RAM disk without backup or EMS memory (expanded memory). If a VGA graphics adapter is beeing used (E.IPC-VM1X), the set memory size of 704 Kbyte, this will be automatically reduced to 640 Kb.

Expanded Memory:

This setting determines whether EMS memory is required and whether the additional memory of the CPU or a memory expansion is to be used on the option socket. The additional memory is the range of the 1 MB pseudostatic CPU memory which is not used as DOS working memory. The possible settings are:

Disable
no EMS memory

Use additional RAM
use CPU buffer memory

Use optional RAM
use memory via the option socket

Additional RAM:

This indicates how much buffer memory is available. The size of the buffer memory is dependent on the main memory set (base memory).

Base Memory	Additional RAM
704 KB	192 KB
640 KB	256 KB
512 KB	384 KB
384 KB	512 KB
256 KB	640 KB
128 KB	768 KB

Optional RAM:

Displays how much RAM is on the option socket

Screen:

Here you can indicate which graphic standard is to be used. Possible settings are:

Color (80x25)	Internal CGA adapter 80 x 25 characters
Color(80x40)	Internal CGA adapter 40 x 25 characters
EGA or VGA	Requires E.IPC-VM1X
Monochrome	Monochrome graphic adapter (is not used with E.IPC)

Note! If you have selected a graphics card which is not available in your system (e. g. monochrome), your connected screen will not display anything. You have the option of switching back to CGA mode by pressing the key combination of CPU push button + ALT + C.

POD: (Power on diagnostics)

Here you can specify wheter the CPU should complete all internal diagnose tests during the boooting-up procedure (starting up). Deactivating the diagnose tests will accellerate the booting-up procedure considerably. The possible settings are:

Run all tests	Starting from a ROM disk in approx. 10 sec.
Skip most tests	Starting from a ROM disk in approx. 5 sec.

Shut down COM1:

Here you can deactivate the integrated COM interface (SM11 only).

ENABLE	Interface is deactivate
DISABLE	Interface is ready-to-operate

Shut down CGA:

Here you can deactivate the integrated CGA adapter

ENABLE	CGA adapter is deactivated
DISABLE	CGA adapter is ready-to-operate

Shut down KEYB:

Here you can deactivate the keyboard adapter

ENABLE	Keyboard adapter is deactivate
DISABLE	Keyboard adapter is ready-to-operate

Software Reset:

Here you can trigger a reset on the XT bus after the "power up" of the CPU.

ENABLE	Trigger software reset
DISABLE	Trigger hardware reset only

XT Bus refresh:

Here you can transmit a refresh signal (/DACK0) on the XT bus

ENABLE	Transmit refresh signal
DISABLE	Suppress refresh signal

Boot Up Sequence:

Here, you can establish the boot sequence, if several bootable disk drives are to be used at the same time. Possible settings are:

A:, C:	Drive A: has priority
C:, A:	Drive C: has priority

Hard disk drive(s):

Here, you can set how many E.IPC-HD1X hard disk modules are to be used in your E.IPC system. Possible settings are:

Disable HD1X	no E.IPC-HD1X module
Enable HD1X	one or two E.IPC-HD1X modules in the system
HD1X-0 only	one E.IPC-HD1X module on primary address
HD1X-1 only	one E.IPC-HD1X module on secondary address

HDD Assignment:

This setting determines the boot sequence if several hard disk modules are used simultaneously. Possible settings are:

Normal	External SCSI hard disks have priority over E.IPC-HD1X
Alternative	E.IPC-HD1X have priority over external SCSI hard disks

Number of hard disks	Setting of HDD assignment	
	Normal	Alternative
1	HD0: HD1X	HD0: HD1X
1	HD0: SCSI	HD0: SCSI
2	HD0: HD1X (primary) HD1: HD1X (secondary)	HD0: HD1X (secondary) HD1: HD1X (primary)
2	HD0: SCSI HD1: HD1X	HD0: HD1X HD1: SCSI
2	HD0: SCSI-0 HD1: SCSI-1	HD0: SCSI-1 HD1: SCSI-0
3	HD0: SCSI HD1: HD1X (primary) HD2: HD1X (secondary)	HD0: HD1X (secondary) HD1: HD1X (primary) HD2: SCSI
3	HD0: SCSI-0 HD1: SCSI-1 HD2: HD1X	HD0: HD1X HD1: SCSI-1 HD2: SCSI-0
4	HD0: SCSI-0 HD1: SCSI-1 HD2: HD1X (primar) HD3: HD1X (secondary)	HD0: SCSI-1 HD1: HD1X (primary) HD2: HD1X (secondary) HD3: SCSI-0

Standby HD1X-0:
Standby HD1X-1:

Here, you can set the duration in seconds, after which the E.IPC-HD1X hard disk modules are to switch to standby mode.

The Settings of the setup menu (page 2)

The second page of the SETUP menu can be accessed by pressing the **PgDn (scroll down)** key (page 2 of 2).

By pressing the **PgUp (scroll up)** key, you can exit the second page of the SETUP menu (extended) and return to the first page of the SETUP menu (standard). Apart from this, all other key functions of the first page (standard) SETUP menu also apply in this instance.

Text font:

This is where you select either the standard or an alternative set of characters.

Inverse Video:

This permits you to switch the screen to inverse. This setting is only important in conjunction with LC displays.

Speaker:

This is where you can activate or deactivate the use of the HC1X CPU signal generator.

CPU:

This setting enables you to define whether the CPU is to operate in the 8086 or 80186 mode.

CPU-CLK:

This is where you define the processing speed of the CPU. Possible settings are:

14.32 MHz
7.16 MHz
4.77 MHz
3.58 MHz

The 7.16 MHz setting increases noise immunity and reduces the current consumption and heat generation of the CPU module.


```
BIOS v3.00          HC1X System Configuration Utility          SN 000000
                      EXTENDED SETUP PAGE 2 OF 2

Text Font:  Normal        Inv. Video:  Disable       Speaker:  Enable

CPU:        80186         Serial:      COM1,3F8h,4   Display:  CRT/DISx
CPU CLK:    14.32 MHz     HC1X LED:    Watchdog      10..36V:  Disable
ISA-BUS:    Share (MST)   HC1X Key:    Reset         I²C-PCD:  FEh
BUS CLK:    CPU CLK/2     assign:      Nothing       I²C-RTC:  A2h
EP-Disk:    Auto-detect   Watchdog:    SuperState R  I²C-UPS:  N/U
init. RAM:  Disable       Wait F1/F2:  Enable        BG10:     C0h

Help line ------------------------------------------------------------

cursor keys to select entries          PgUp for Extended Setup Page 1
+- to change an entry
ESC to exit without saving             F10 to save then exit
```

SETUP menu (page 2) with factory settings

ISA-BUS:

This defines the mode of operation of the E.IPC bus. Possible settings are:

Exclusive	This CPU has exclusive access to the bus. Changeover to slave is not possible during operation.
Disconnect	This CPU does not have access to the bus. Changeover to master is not possible during operation.
Share (MST) (IRQ7 allocated)	This CPU is the master in an E.IPC system consisting of several CPU modules. Changeover to slave is possible during operation.
Share (SLV) (IRQ7 allocated)	This CPU is a slave CPU in an E.IPC system consisting of several CPU modules. Changeover to master is possible during operation.

The Share (MST) and Share (SLV) settings are required, if the master CPUs are required to hand over control of the bus during active operation in order to permit slave CPUs access specific modules on the E.IPC bus. With the Share settings, hardware interrupt 7 is assigned to prevent conflicting situations on the E.IPC bus.

BUS-CLK:

Determines the clock pulse on the E.IPC bus. The bus clock pulse is dependent on the CPU clock pulse set (CPU CLK). Possible settings are:

CPU CLK	The bus clock pulse corresponds to the CPU clock pulse.
CPU CLK/2	The bus clock pulse corresponds to half CPU clock pulse.
CPU CLK/3	The bus clock pulse corresponds to the CPU clock pulse/3.
CPU CLK/4	The bus clock pulse corresponds to the CPU clock pulse/4.

The **CPU CLK** setting is not recommended for a CPU clock pulse of **14.32 MHz**, since not all E.IPC modules are able to operate with a bus clock pulse of **14.32 MHz**. The E.IPC bus has only been specified up to 8 MHz.

EP-Disk:

This is where you can set which logic drive is to be allocated to a ROM/RAM disk. Possible settings are:

Disable	ROM/RAM disk switched off
Auto-Detect	Diskette drive has priority over ROM/RAM disk (with inserted diskette)
Is Drive A:	ROM/RAM disk is drive A: (boot drive)
Is Drive B:	ROM/RAM disk is drive B:

Init. RAM:

A ROM/RAM disk where the ROM and RAM have been combined into a logic drive may no longer boot up if the RAM contents have become invalid. In this case, this setting is to be set to **Enable**. The RAM disk is then deleted during the next boot procedure and the setting automatically reset to **Disable**. The function of this setting is the same as that of the key combination **CPU key + ALT + CTRL + SPACE BAR**.
When set at **always** the RAM disk will be initialised at every restart.

Serial:

Defines the address of the internal serial interface on the HC1X CPU. Possible settings are:

Disable	Interface switched off
COM1,3F8H,4	COM1, IO address=3F8h, IRQ=4
COM2,2F8H,3	COM2, IO address=2F8h, IRQ=3

HC1X LED:

Defines the operating mode of the CPU signal LED. Possible settings are:

Power-On	Status display (permanently on)
Master/Slave	LED displays bus access
Watchdog	LED displays watchdog trigger

I²C-Bus	LED displays access to I²C bus
Software	LED is controlled via user program

HC1X Key:

Defines the operating mode of the CPU signal LED. Possible settings are:

Reset	Push button releases hardware reset
Master/Slave	Manual switch between master and slave via the CPU key and service keyboard
PC-Key	Push button provides keyboard scan code
Software	Push button is interrogated by user program

assign:

Defines which key scan codes will be transmitted with push button setting **HC1X Key: PC-KEY.** The following keys may be allocated:

nothing
F1-F10
ESC, ENTER, SPACE, L SHIFT, R SHIFT, CTRL, ALT
CAPS, NUM, SCROLL, TAB, BKSP, INS, DEL
GRAY +, GRAY -

All other keys may be allocated using the HC10SET.EXE program.

Watchdog:

Defines the operating mode of the watchdog timer. Possible settings are:

Disable	Watchdog is switched off
SuperState R	Watchdog timer is operated by SuperState BIOS
IRQ0 (INT 8)	Watchdog is operated by standard BIOS

Note: Test programs such as "Landmark Speedtest" or "Checkit" should not be started in watchdog mode *IRQ0 (INT 8)*, as this may switch off the IRQ0, which can lead to the watchdog timer being triggered.

Wait F1/F2:

This is where you can set whether the message "**Press F1 to continue, F2 to Setup**" is to be displayed and whether there should be a 3 second wait for pressing a key during booting up.

Display:

This is where you can set whether a CRT/RGB screen or an LC display has been connected to the CGA interface of the HC1X CPU. Possible settings are:

CRT	CGA/RGB screen

LCD	LC display
CRT/DISX	E.IPC-DIS1/DIS2 with I²C bus control if available, otherwise CGA/RGB screen

10..36V:

Defines whether the +10 V ... +36 V supply voltage on pin 7 of the CGA interface is to be active or not. This voltage must be switched on if the RGB/FBAS converter E.IPC-CV10 is used, but should otherwise always be switched off.

I²C-PCD:

Defines the I²C bus address of the CPU internal I²C bus controller for multi-master communication.

I²C-RTC:

Defines the I²C bus address of the real-time clock, which is read during booting up. The "N/U" setting (not used) switches off the BIOS support for the real-time clock.

I²C-UPS:

Defines the I²C bus address of the optional USV module E.IPC-USV1. The "N/U" setting (not used) switches off the BIOS support for the USV module.

BG10:

Determines the I²C bus address of the LCD display

N/U	Deactivates BG10 support
C0h-DEh	Selected I²C bus address

The internal ROM/RAM disk

The CPU modules E.IPC-HC15 to HC17 are equipped with an internal ROM disk and a battery buffered RAM disk (zero power RAM), on which the operating system and several important additional programs for the CPU module are stored. The RAM disk provides space for user data and programs which can be imported using a diskette drive or the “Fernterm” program.
A special feature of the ROM/RAM disk, is that both the ROM and RAM section are on one drive. The assignment of the ROM/RAM disk on the drive can be defined in the BIOS setup menu. If the space in the RAM section of the ROM/RAM disk is insufficient or greater data security and a maintenance-free CPU are of particular importance, then the user programs can be stored by the user in the ROM section using the accompanying ROMKIT program.

Further information about the ROM/RAM disk can be found in the “E.IPC Romkit” manual.

The E.IPC flash disk

In addition to the EPROM and RAM memory, the CPU modules E.IPC-HC16 and E.IPC-HC17 have a 512 KB flash memory which provides an additional drive. This flash drive is addressed via the unit driver FFSDRV.SYS which is loaded in the system file CONFIG.SYS. At delivery the CPU modules E.IPC-HC16 and HC17 are programmed so that the drivers are automatically loaded. The drive allocation of the flash disk is defined via a further unit driver SWAPFFS.SYS. The entry

DEVICE=SWAPFFS.SYS C:

defines for example that the flash disk is addressed via drive C.

How the E.IPC flash disk operates

The E.IPC flash disk is a semi-automatic flash file system. Programs and data can be copied from diskette or via Fernterm onto the flash disk as for a RAM disk.
User programs can be open and modify files which are on the flash disk.
The limitation in contrast to a RAM drive is that sectors which are allocated are not automatically released. Thus every modification reduces the free memory available on the flash disk.

Note:

Take care that an application program does not continually modify files an the flash disk as the available flash memory will be exthaused in a very short time. Continually modified files should be stored on the RAM disk drive (ZPRAM).

Reorganisation the E.IPC flash disk

If the available memory on the flash disk is exthaused, the flash disk can be reorganised to release allocated memory sectors. To do this access the program CHKFFS.EXE.

The program CHKFFS.EXE

To start reorganisation enter the following line

A:\> **CHKFFS/F**

The flash disk will then be fully reorganised. All programs and data on the drive will remain intact and unused sectors will be released.

The program CHKFFS.EXE is also required to install the flash disk the first time or to determine the current status of the flash disk.

You can access an overview of the functions in CHKFFS.EXE with:

A:\>**CHKFFS/?**

```
CHKFFS V1.00 - (c)1995 Beck Computer-Lösungen GmbH
HC1X flash disk reorganisation utility

 call: CHKFFS [/h | /?] | [/f | [/p [/b]] [/q]]

      /h | /?     - shows this help
      /f          - force reorganisation
      /p          - first time preparation
      /b          - reserve 128k for bios update
                         (only available with /p)
      /q          - quiet mode, suppress messages
```

To ascertain the status of the flash disk, access CHKFFS.EXE without parameters:

A:>**CHKFFS**

```
CHKFFS V1.00 - (c)1995 Beck Computer-Lösungen GmbH
HC1X flash disk reorganisation utility
512K flash memory found
number of erase/prog-cycles: 3
512 K flash disk found
flash disk driver installed (C:)

-------------------------------
```



```
 sectors allocated:   11 ( 1%)
 sectors removed:      0 ( 0%)
 sectors available: 1009 (99%)
-------------------------------
```

The HC10SET program

The **HC10SET.EXE** program enables you to set some important operating parameters of the HC1X CPU outside the SETUP menu. Amongst other things, you can set the operating modes of the signal LED, the CPU push button, the watchdog timer and the ROM disk with this program. All settings are made via command line parameters. The HC10SET program recognises two important operating modes:
In the first operating mode, the current CPU parameters can be displayed and modified. Modified operating parameters are activated immediately. This operating mode is active as standard.
In the second operating mode, the operating parameters, which are stored in the parameter EEPROM of the CPU can be displayed and modified. Modifications in this operating mode are permanently stored until the next modification via HC10SET and are not activated until the next restart of the CPU. This second mode of operation is selected by specifying the parameter **-EE** when calling up the HC10SET program.

Display of the current operating parameters by calling **HC10SET** (without parameters):

```
HC10SET Version 2.00  (C) 1994 Beck Computer-Lösungen GmbH, Wetzlar
Programming the HC1X specific functions

Actual state:

Mode          Value Description
──────────────────────────────────
Key          (T):  2  key is reset key
LED          (L):  4  watchdog-refresh-indicator
COM-Port     (C):  1  COM1 (Addr=3F8h, IRQ=4)
CPU mode     (P):  2  80186 mode
System bus   (M):  2  system bus on (master)
Watchdog     (W):  4  SuperState-BIOS controls watchdog
Display      (D):  3  CRT/DISx
AV voltage   (V):  1  +10..36V off
CPU clock    (S):  1  CPU clock: 14.32 MHz
XT-Bus clock (X):  2  XT-Bus clock: 1/2 CPU clock: 7.16 MHz

Get help with HC10SET -?
```

Display of operating parameters in EEPROM via calling of **HC10SET -EE**:

```
HC10SET Version 2.00  (C) 1994 Beck Computer-Lösungen GmbH, Wetzlar
Programming the HC1X specific functions

Permanent EEPROM state:

Mode        Value Description
──────────────────────────────
Key          (T):  2  key is reset key
LED          (L):  4  watchdog-refresh-indicator
```



```
COM-Port     (C):  1  COM1 (Addr=3F8h, IRQ=4)
CPU mode     (P):  2  80186 mode
Watchdog     (W):  4  SuperState-BIOS controls watchdog
USV          (U):  1  off
USV relais   (R):  -  not available yet
EP disk      (B):  1  standard
<F1>/<F2>    (F):  1  wait for pressing <F1>/<F2>
System bus   (M):  2  system bus on (master)
Display      (D):  3  CRT/DISx
AV voltage   (V):  1  +10..36V off
CPU clock    (S):  1  CPU clock: 14.32 MHz
XT-Bus clock (X):  2  XT-Bus clock: 1/2 CPU clock: 7.16 MHz
```

A list of all functions may be obtained by calling up the HC10SET program with parameter *-?*.

> **Note:** Please note that the *HC10SET.EXE* (as are any other programs) is undergoing continual further development and that this manual may therefore not necessarily reflect the current software status. Therefore, please note any modification documented in the *HC10SET.HST* file.

The real time clock

The real time clock of a FESTO IPC installation is not located in the CPU module, but in the E.IPC-PS10 voltage converter module or in the E.IPC-BP50 busboard.
In order to guarantee that the FESTO IPC installation is truly maintenance-free, the real time clock is supplied not by batteries but by a Goldcap capacitor which retains data for a period of 3 days. If a 3 day buffer is insufficient, then the CPU module can be equipped with a battery buffered memory with an integrated real time clock such as the E.IPC-ZL16 or E.IPC-ZL17.

When the system is started, the current clock time is read automatically via the internal I^2C bus from the power supply module and transferred to the system clock of the E.IPC-HC1X CPU module.
The routines for reading and writing onto the real time clock are contained in the software development kit which is available as an accessory.
To set the real time clock, the correct time and date must first be set in the usual manner in the SETUP menu of the HC1X BIOS. Upon exiting the SETUP menu, the current time is then transferred to the real time clock via the I^2C bus.

If several E.IPC-HC1X CPU modules are operated on one busboard or in an I^2C network, all CPUs can likewise access the real time clock of a master system.

> **Note:** If several E.IPC-PS10 power supply modules are operated in one I^2C network, only one real time clock may be active. To switch off the real time clock, please refer to the appropriate instructions in the manual for the E.IPC-PS10 power supply module.

The parameter EEPROM

The E.IPC-HC1X CPU modules are fitted with a 512 byte EEPROM for storing the operating parameters. The following data are stored in the EEPROM:

- BIOS setup data
- I/O initialisation of digital outputs with customer-specific data. This initialisation occurs within 500 ms of the FESTO IPC installation being switched on or after a hardware reset on the CPU (triggered by the reset push button or the hardware watchdog).
- RGB or LCD operating mode
- Master/slave mode

Programs for filing of customer-specific I/O data in the EEPROM are contained in the enclosed driver diskette, high-level language routines and libraries for addressing the EEPROM in your own applications form part of the software development kit, which is available as an accessory. For further information, please refer to the instructions for the service interrupt of the CPU.

The integrated CGA graphics adapter

The Festo CPU modules E.IPC-HC1X are fitted with a CGA compatible graphics interface. Via the 9-pin SUB-D socket, both RGB monitors with 15.625 kHz deflection frequency (standard CGA) and LCD displays can be connected. The operating mode is stored in the EEPROM via the Setup program.
The graphics interface permits the representation of 80x25 or 40x25 characters in text mode (16 colours) or of 320x200 dots in graphics mode (4 or 2 colours). A special mode also permits representation of 640x400 dots (2 colours). All CGA compatible programs can be run in these modes (with the exception of special mode).
The character set used in text mode can be loaded via software and can be exchanged for customer-specific character sets.
RGB-TTL monitors with 15.4 kHz horizontal deflection frequency and 50 Hz refresh display frequency can be connected. An optional intensity input is required to represent 16 colours.

Up to 16 tones of grey can be displayed on monochrome LCD displays (max. of 4 is recommended). To ensure good legibility of existing OEM applications, the BIOS colour palette can be adapted by means of a help program contained in the software development kit.

A list of LCD and TFT displays which can be operated on the E.IPC-HC1X CPU modules as well as instructions on connection can be obtained on request. Ready-to-connect displays for front panel, wall or top-hat rail assembly with optional touch screen are available on request.

The I²C bus

The E.IPC-HC1X CPU modules are equipped with an I²C bus controller (Philips/Signetics PCD8584), which permits both master and slave operation. The two I²C bus circuits are designed to interface with the PC/XT bus, the keyboard plug and the internal I²C plug ST5. The I²C bus is a device bus with which up to 128 network slaves (theoretical value) can communicate via two bidirectional cables (one clock circuit and one data circuit). The maximum bus length is 5 m at a data rate of 100 bit/s. This is used primarily for communication between the E.IPC modules (in addition to the PC/XT bus, e. g. for reading the real-time clock in the network module), for communication between CPU modules in multiprocessor mode as well as for communication between individual E.IPC installations. Customer-specific I²C bus devices and modules can also be connected, if these comply with the Philips I²C standard. The software development kit available as an accessory contains drivers and sample programs for incorporating the I²C communication into the user's own applications.

> **Technical note:** As the I²C bus operates at TTL level (open collector bus) and offers only limited noise immunity, the user must ensure that the bus cables are routed and used only in a housing and an environment conforming to EMC requirements. Should this not be possible, networking via the I²C bus should be dispensed with and a field bus system used instead.

Examples of customer-specific I²C applications are:

- Service and diagnostic devices (for connection via the keyboard plug of the E.IPC-HC1X CPU module instead of a PC/XT keyboard)
- Display and keypad units in front panels of equipment or in control cabinet doors
- Infrared remote control for E.IPC systems (IR transceiver fitted into the CPU module instead of the interface module)
- Low-priced networking of time-uncritical digital and analog I/O modules
- Simplified implementation of customer-specific E.IPC modules (e. g. with the help of the hardware development kit) for sample systems. If actuation is via the I²C bus, then the expensive bus interface for the PC/XT bus can be dispensed with.

Reset push button and signal LED

In order to switch over and display the operating status of the E.IPC-HC1X CPU module, the latter is fitted with a push button at the front and a signal LED. Both input/output elements can be programmed for different operating modes (e. g. button as reset button or LED as automatic master/slave display). The information as to whether a CPU is being operated in master or slave mode is filed in the parameter EEPROM in order to avoid collisions on the PC/XT bus during system startup. The operating mode of the push button and the signal LED can be set with the help of the enclosed HC10SET.EXE program. The push button and the LED can also be addressed by the user's own applications via the service interrupt.

The watchdog timer

In order to ensure maximum operational reliability of the E.IPC-HC1X CPU module, this has been fitted with a hardware watchdog. Depending on the operating mode set, the watchdog system is operated via the system BIOS, which monitors the general CPU function or the application program takes over control of the watchdog and thus ensures the correct operation of the software.
As soon as the watchdog timer has been activated, it must be reset by the application program one per second, otherwise there will be a hardware reset or a hardware interrupt, depending on what has been programmed. The watchdog can be programmed with the enclosed HC10SET.EXE program. The watchdog can also be incorporated into the user's own applications via the service interrupt.

The speaker

The E.IPC-HC1X CPU modules are equipped with an internal 85dB signal generator which can be used in the same way as a standard PC loudspeaker and controlled by software.

Multiprocessor operation

One of the most important features of the E.IPC-HC1X CPU module is the facility of master/slave operation whereby, in slave operation, the CPU modules are isolated from the PC/XT bus via the programmable bus driver. In this way, several slave CPUs can be operated together with a master CPU on a common PC/XT bus or busboard. Each slave CPU is a fully functional PC thanks to its internal CGA graphics, ROM/RAM disk drive and optional serial interface. The E.IPC system recognises several operating modes:

1. Standard operation with a CPU
2. Multiprocessor operation with a fixed master
3. Multiprocessor/multimaster operation with alternating master CPUs

Communication between the CPUs as well as the right of access to the bus are made via the I^2C bus.
Important is the ISA-BUS setting in the SETUP menu. This is where the operating mode of the E.IPC bus can be defined in its configuration.
If the system comprises only one CPU or if a CPU is to operate exclusively as master, the ISA-BUS option is to be switched to **exclusive**.
If the CPU is to be used solely as slave without access to the E.IPC bus the ISA-BUS setting is to be switched to **disconnect**.
If several CPU modules are to be operated on one E.IPC bus with alternating access to the bus (multimaster mode), the ISA bus option is to be switched to **Share (MST)** on one CPU module and to **Share (SLV)** on all other CPU modules. Switching from master to slave is then effected via the service interrupt. Via the hardware interrupt 7, the CPU modules in the share mode also check whether the bus really is free prior to assigning to it.
In the case of CPU modules operated in slave mode, bridge connector J2 must also be

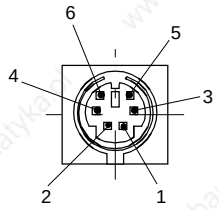
removed from inside the CPU module to prevent the watchdog reset of a slave CPU from triggering a reset on the E.IPC bus.

Caution! If several CPU modules with the Exclusive setting are operated on one E.IPC bus, this can lead to permanent damage to the CPU modules!

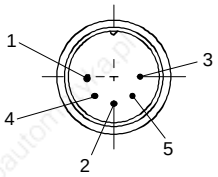
The keyboard interface

The allocation of the E.IPC keyboard plug corresponds to the original IBM PS2* layout. Standard XT keyboards or reversible XT/AT keyboards in operating mode PC or XT may be connected. The service adapter for connecting a keyboard with the 5-pin standard XT/AT plug is available as an accessory item (order designation E.IPC-ZK10).
In addition to pins for the keyboard signals, there are also two pins for the I²C bus, data and clock signals. Moreover, in field operation, external customer-specific devices (e. g. displays, keyboard) as well as intelligent operating and diagnostic devices can be connected, providing these are fitted with the standard I²C bus interface from Philips/Signetics.

Pin number	Signal PS1 mini DIN	Signal standard XT/AT
1	Keyboard data	Keyboard clock
2	I²C-Bus data	Keyboard data
3	GND	-
4	+5 V	GND
5	Keyboard clock	+5 V
6	I²C bus clock	

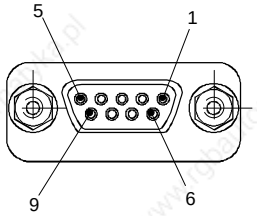


E.IPC mini DIN socket
(to suit plug **JST mini DIN 6-pin)**



Standard XT/AT keyboard plug (DIN 41524), see table for allocation.
Adapter for DIN 41524 socket on E.IPC mini DIN plug: see order information at end of this manual.

The CGA compatible video interface



9-pin SUB-D connector (DIN 41652)

* activated via software, **max. 250 mA**
** Do not connect pin 2 in RGB mode.

Pin numb.	RGB allocation	LCD allocation
1	GND	GND
2	DOTCLK**	DOTCLK
3	RED	DOT2
4	GREEN	DOT1
5	BLUE	DOT0
6	INTENSITY	DOT3
7	+10 V ... 36 V DC*	+10 V ... 36 V DC*
8	Horiz. sync.	Latch pulse
9	Vert. sync.	FLM

The E.IPC-HC1X CPU module is fitted with a CGA compatible graphics interface. Depending on the operating mode, both RGB monitors with 15.625 deflection frequency (standard CGA) and LCD displays can be connected via the 9-pin socket. The operating mode is stored in the EEPROM via the setup program. To connect the LC displays, please refer to the appropriate chapter in the LC display manual.

A voltage of +10 V ... +36 V DC can be supplied to pin 7 of the video interface by software via the service interrupt or via the HC10SET.EXE program which is enclosed (see HC10SET program). This supply voltage is normally switched off. The level of the supply voltage depends on the operating voltage of the complete E.IPC system and may be loaded with a maximum of 250 mA.

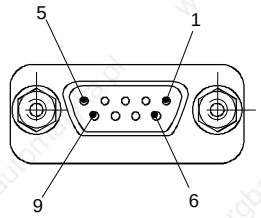
Warning! The supply voltage of +10 V ... +36 V at the video interface may only be switched on when an appropriate adapter (e. g. the E.IPC RGB/BAS adapter) has been connected. Otherwise, the connected monitor or LC display could be damaged.

The graphic modes of the CGA/LCD interface:

Mode	Representation	Resolution	Colours
1	Text	40 x 25	16
3	Text	80 x 25	16
4	Graphics	320 x 200	4
5	Graphics	320 x 200	2
6	Graphics	640 x 200	2
-	Graphics	640 x 400	2

The serial interface (optional)

The internal serial interface of the E.IPC-HC1X CPU module can be fitted with either RS232, RS422, RS485, 20 mA or to suit customer-specific requirements (see table for interface modules). The interface has been designed for high speed transfer rates of up to 56700 bit/s (depending on the interface equipment) and is compatible with the industrial standard both as regards programming and allocation (8250 compatible).
I/O addresses and interrupt may be programmed via the SETUP menu and the HC10SET.EXE program.



9 pin SUB-D plug connector
(DIN 41652)

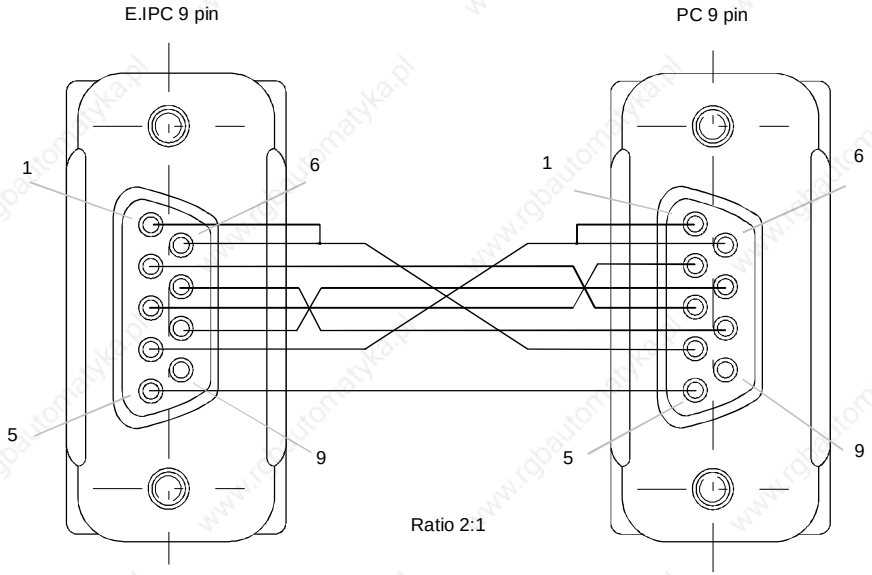
The allocation of interface converter E.IPC-SM10/SM11, fitted as standard from E.IPC-HC15 onwards:

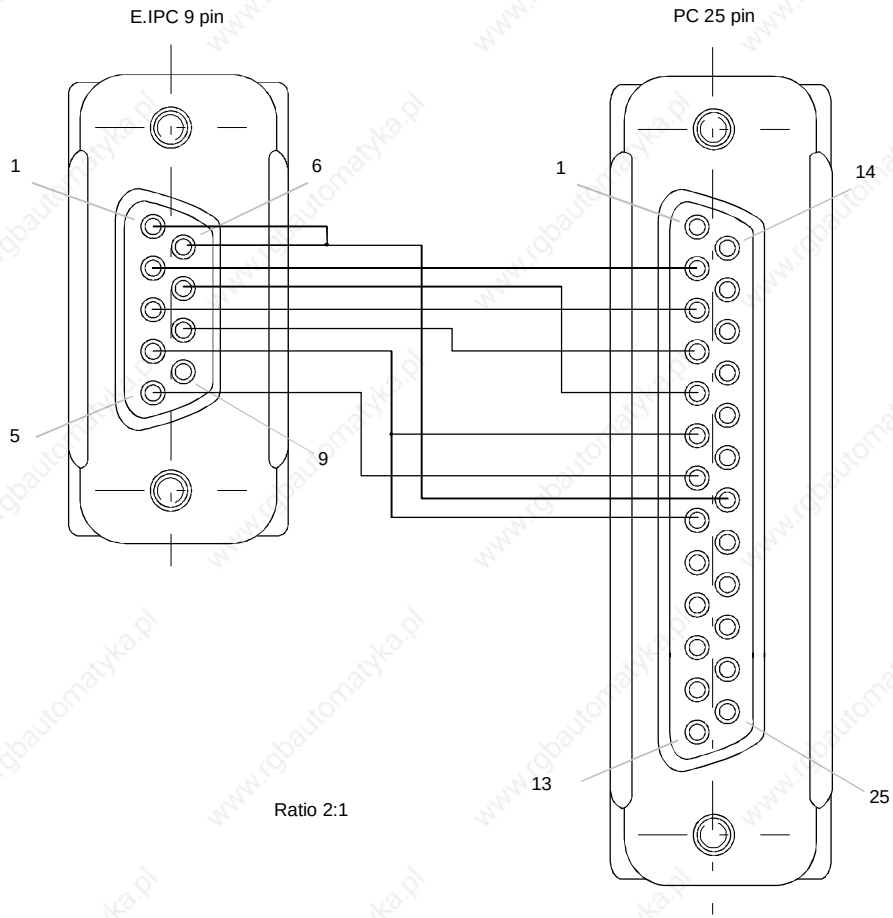
Pin number	Direction	Signal	Meaning
1	In	DCD	Data carrier detect
2	In	RXD	Receive data
3	Out	TXD	Transmit data
4	Out	DTR	Data terminal ready
5		GND	Signal ground
6	In	DSR	Data set ready
7	Out	RTS	Request to send
8	In	CTS	Clear to send
9	In	RI	Ring indicator

List of available interface modules

Order number	Description
E.IPC-SM11	RS232 with 7 KV ESD protection
E.IPC-SM20	TTY/20 mA, opto isolated
E.IPC-SM30	RS422/RS485
E.IPC-SM40	RS232, opto isolated, 1 KV
E.IPC-SM60	RS485, opto isolated

A standard zero modem cable is required (allocation see below) for coupling the HC1X CPU to another PC compatible processor via the RS232. With suitable transfer software (e. g. DOS6 Interlink or LapLink), programs and data can thus be interchanged with the HC1X CPU. The zero modem cable is available as an accessory under the order designation E.IPC-ZK11.





Zero modem cable to connect the E.IPC-HC1X CPU module to another PC or CPU module (only in connection with the serial interface converters E.IPC-SM10, E.IPC-SM11 or E.IPC-SM40).

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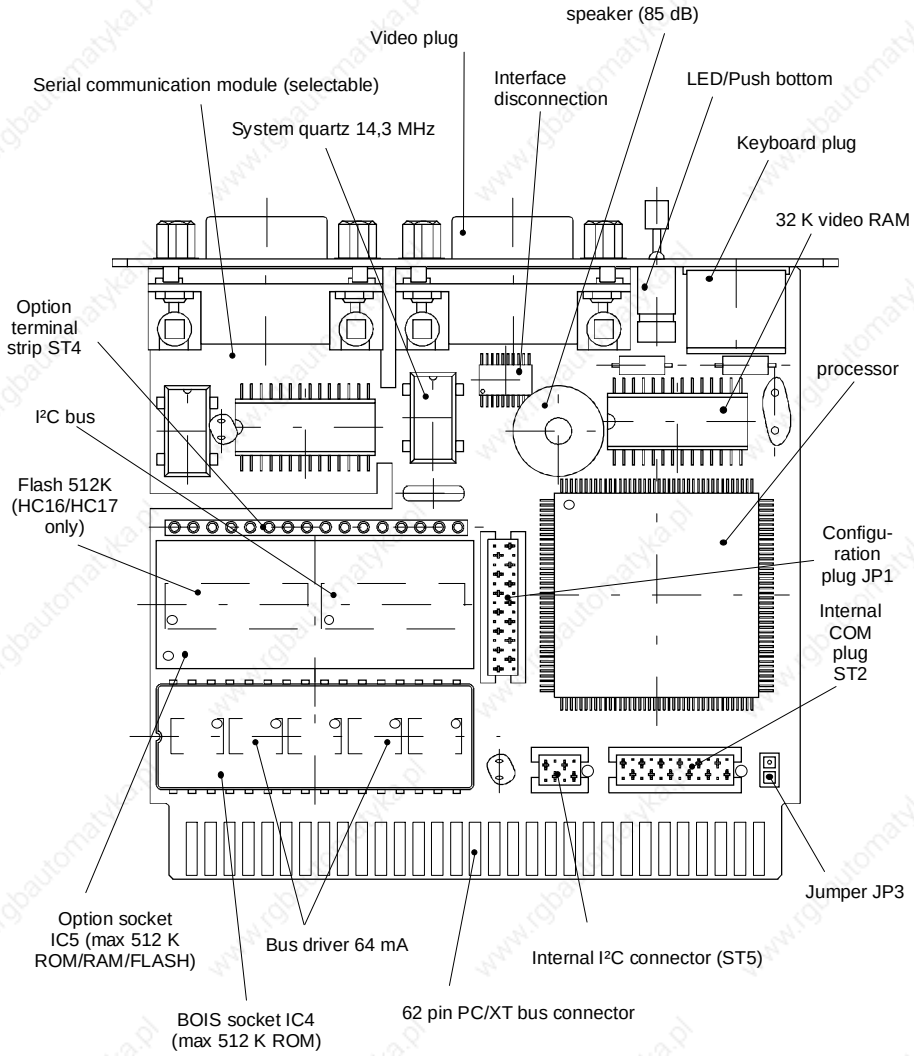
The internal layout of the E.IPC-HC15/HC16/HC17 CPU modules



Ratio 1:1

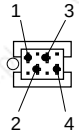
FESTO

The bridge connectors J1 and J2

Bridge connector	open	closed
JP3	Slave operating mode No reset at PS1 bus	Master operating mode CPU controls power-on and watchdog reset at PS1 bus

Bridge connector J1 currently does not have a function and remains permanently open. Bridge connector J2 controls the reset on the E.IPC bus. This bridge connector must always be closed during normal operation in order for the modules on the E.IPC bus to be supplied with a reset signal. In master/slave mode, bridge connector J2 must be closed only on one CPU (master) on the E.IPC bus.

The internal I²C bus plug (ST5)

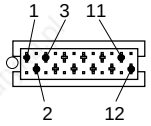


4-pin micro-match socket connector (matching connector for flat ribbon connector: **AMP-0-215083-4,** Bürklin part no.: **58F460**)

Pin number	Signal flow	Signal
1	In/Out	I²C clock
2	In/Out	I²C data
3	Out	GND
4	Out	+5 V

For customer-specific applications, the I²C bus can be connected via the internal I²C bus plug ST5 to the serial communication module by means of a standard flat ribbon cable.

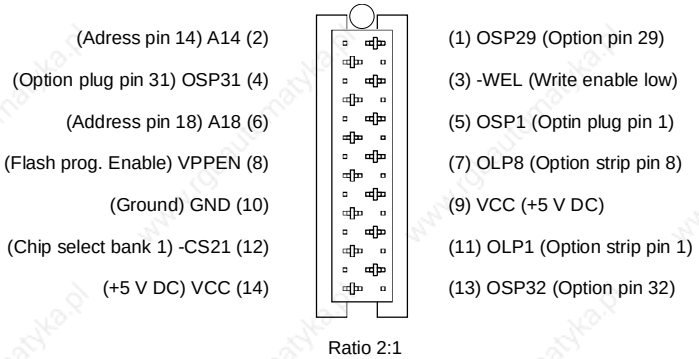
The internal COM plug (ST2)



12-pin micro-match socket connector (matching connector for flat ribbon connector: **AMP-1-215083-2,** Bürklin order no.: **58F468**)

Pin number	Signal flow	Signal	Meaning
1	Out	+5 V	
2	In	UART-Clock	Pulse from COM module
3	In	DCD	Data carrier detect
4	In	DSR	Data set ready
5	In	RXD	Receive data
6	Out	RTS	Request to send
7	Out	TXD	Transmit data
8	In	CTS	Clear to send
9	Out	DTR	Data terminal ready
10	In	RI	Ring indicator
11		GND	Signal ground
12	Out	+10..36 V DC	

The configuration plug for the option socket (JP1)



Ratio 2:1

14-pin micro-match socket strip (matching connector: **AMP-1-215464-4,** Bürklin order no.: **58F450**)

Depending on the fitting of the option socket (RAM/ROM, FLASH 128 Kb/512 Kb, extension module etc.) an appropriate code plug must be placed in the configuration plug JP1. The option socket is required to convert the internal ROM disk to max. 896 Kb or to establish a RAM disk with up to 512 Kb.

Warning: Faulty configuration plugs can lead to permanent damage to the modules used or the CPU module.

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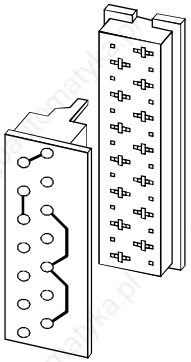
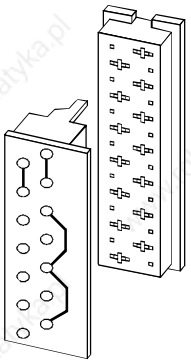
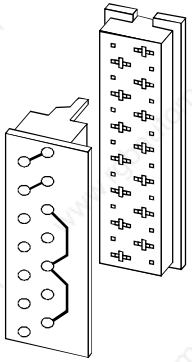
Sample configurations for the configuration plug JP1



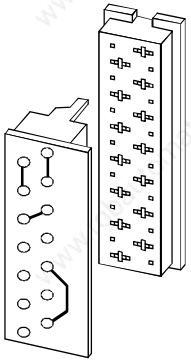
EPROM 512 KB:
(e. g. 27C040)



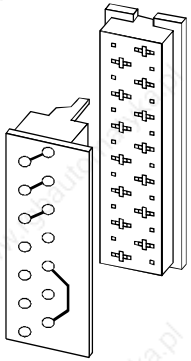
SRAM 128 KB:



Flash ROM 512 KB:
(e. g. AM29F040)



PSRAM 512 KB:
(e. g. 518512PL)



Flash ROM 128 KB:
(e. g. AM29F010)

Preconfigured plugs are available as accessories (please enquire).

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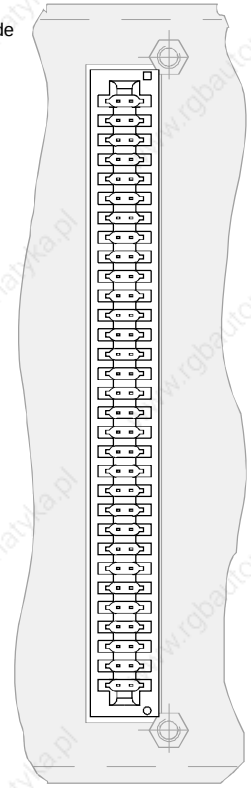
The PC/XT compatible E.IPC bus

Plug designations: ST3 ... ST7



Solder side		Fitting side	
GND	B1	A1	-I/O CH CK
RESET DRV	B2	A2	D7
+5 V	B3	A3	D6
IRQ2	B4	A4	D5
free (-5 V)	B5	A5	D4
DRQ2	B6	A6	D3
free (-12 V)	B7	A7	D2
programmable (res, -0WS)	B8	A8	D1
10 V ... 36 V (+12 V)	B9	A9	D0
GND	B10	A10	I/O CH READY
-MEMW	B11	A11	AEN
-MEMR	B12	A12	A19
-IOW	B13	A13	A18
-IOR	B14	A14	A17
-DACK3	B15	A15	A16
DRQ3	B16	A16	A15
I²C-Clock (-DACK1)	B17	A17	A14
I²C-Data (DRQ1)	B18	A18	A13
frei (-DACK0/-RFSH)	B19	A19	A12
CLOCK	B20	A20	A11
IRQ7	B21	A21	A10
IRQ6	B22	A22	A9
IRQ5	B23	A23	A8
IRQ4	B24	A24	A7
IRQ3	B25	A25	A6
-DACK2	B26	A26	A5
T/C	B27	A27	A4
ALE	B28	A28	A3
+5 V	B29	A29	A2
OSC	B30	A30	A1
GND	B31	A31	A0

metric 1:1

The pin allocation shown correspond to the E.IPC-HC1X CPU modules. There will be slight difference in the pin allocation if other CPU modules are used, these will be depend on the CPU. Information regarding differences in pin allocation can be found in the appropriate CPU manuals.

The data in brackets indicates the allocation of the PC/XT bus which differs from that of the E.IPC bus. The different allocations concern only the supply voltages (B5, B7 and B9), DMA channel 1 (B17 and B18), the memory refresh at the PC/XT bus (B19) and the additional allocation of pin B8.

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The allocation of the memory addresses

Address range (hex.)	Module	Select number	Allocation
00000h-9FFFFh	E.IPC-HC1X	-	DOS working memory (640 KB)
A0000h-AFFFFh	E.IPC-HC1X	-	DOS working memory or VGA graphic controller
A0000h-AFFFFh	E.IPC-VM1X	-	DOS working memory or VGA graphic controller
B0000h-B7FFFh	-	-	Monochrome graphic controller
B8000h-BFFFFh	E.IPC-HC1X	-	CGA/LCD graphic controller
C0000h-C3FFFh	E.IPC-VM1X	-	VGA graphic controller (BIOS)
C4000h-C4FF0h	E.IPC-CP6X	1	Profibus / Festo bus controller
C8000h-CBFFFh	E.IPC-SC10	1	SCSI controller
C8000h-CBFFFh	E.IPC-CP1X	1	Ethernet controller (boot ROM)
C8000h-C8FF0h	E.IPC-CP40	1	Beckhoff bus controller
CC000h-CFFFFh	E.IPC-CP6X	2	Profibus / Festo bus
D0000h-DFFFFh	E.IPC-HC1X	-	EMS memory (option)
D0000h-D0FFFh	E.IPC-CP40	3	Beckhoff bus controller
D4000h-D4FFFh	E.IPC-CP6X	3	Profibus / Festo bus controller
D8000h-DBFFFh	E.IPC-SC10	3	SCSI controller
D8000h-DBFFFh	E.IPC-CP1X	3	Ethernet controller
D8000h-D8FFFh	E.IPC-CP40	3	Beckhoff bus controller
DC000h-DFFFFh	E.IPC-FC20	2	Floptical disk controller
DC000h-DCFFFh	E.IPC-CP6X	4	Profibus / Festo bus controller
DD000h-DDFFFh	E.IPC-CP	4	ISP bus controller
E0000h-FFFFFh			E.IPC system BIOS

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Allocation of the I/O addresses at the E.IPC bus

IO range	Module	KSW	Designation
0E0h-0EFh	-	-	PLC safety function
100h-10Fh	E.IPC-CP50	1	Interbus-S controller
110h-110h	E.IPC-OM70	1	6 changeover outputs
110h-111h	E.IPC-OM2X	1	8 digital inputs / 8 digital outputs
	E.IPC-IM1X	1	16 digital inputs
	E.IPC-OM1X	1	16 digital outputs
	E.IPC-OM40	1	16 digital outputs
	E.IPC-TM10	1	16 digital inputs / 16 digital outputs
110h-113h	E.IPC-AS12	1	32 LEDs
	E.IPC-AS13	1	16 switches
	E.IPC-AS14	1	32 LEDs
	E.IPC-OM50	1	32 digital outputs
112h-113h	E.IPC-IM1X	2	16 digital inputs
	E.IPC-OM1X	2	16 digital outputs
	E.IPC-OM2X	2	8 digital inputs / 8 digital outputs
118h-11Fh	E.IPC-IM20	1	Incremental encoder
120h-123h	E.IPC-AS11	1	8 LEDs / 8 buttons
120h-13Fh	E.IPC-IO1X	0	8 channel A/D converter
130h-133h	E.IPC-IO7X	1	2 analog outputs
130h-137h	E.IPC-IO6X	1	4 analog outputs
134h-137h	E.IPC-IO7X	2	2 analog outputs
140h-15Fh	E.IPC-IO1X	1	4 analog inputs
160h-16Fh	E.IPC-CP50	2	Interbus-S controller
170h-173h	E.IPC-AS12	4	32 LEDs
	E.IPC-AS13	4	16 switches
	E.IPC-AS14	4	32 LEDs
176h-17Fh	E.IPC-HD1X	1	Hard disk module
	E.IPC-ED1X	1	Hard disk module
186h-18Fh	E.IPC-HD1X	2	Hard disk module
	E.IPC-ED1X	2	Hard disk module
1A0h-1A3h	E.IPC-AS11	4	8 LEDs / 8 buttons
1A4h-1A5h	E.IPC-IO4X	1	4 channel A/D converter
1A6h-1A7h	E.IPC-IO4X	4	4 channel A/D converter
1B0h-137h	E.IPC-IO6X	1	4 analog outputs
1B0h-1B3h	E.IPC-IO7X	3	2 analog outputs

1B4h-1B7h	E.IPC-IO7X	4	2 analog outputs
1C0h-1DFh	E.IPC-IO1X	3	4 analoge inputs
1E0h-1E1h	E.IPC-AM10	1	Stepper motor module, 1 axis
1E2h-1E3h	E.IPC-AM10	2	Stepper motor module, 1 axis
1E4h-1E5h	E.IPC-AM10	3	Stepper motor module, 1 axis
1E6h-1E7h	E.IPC-AM10	4	Stepper motor module, 1 axis
1E8h-1E9h	E.IPC-AM10	5	Stepper motor module, 1 axis
1EAh-1EBh	E.IPC-AM10	6	Stepper motor module, 1 axis
1F0h-1F8h	-	-	Hard disk controller
1F8h-1FFh	-	-	PLC safety function
200h-20Fh	-	-	Game Port
210h-211h	E.IPC-OM10	3	Digital outputs
	E.IPC-OM20	3	8 digital inputs / 8 digital outputs
	E.IPC-IM10	3	16 digital inputs
210h-213h	E.IPC-AS14	2	32 LEDs
	E.IPC-AS12	2	32 LEDs
	E.IPC-AS13	2	16 switches
212h-213h	E.IPC-OM10	4	Digital outputs
	E.IPC-OM20	4	8 digital inputs / 8 digital outputs
	E.IPC-IM10	4	16 digital inputs
218h-21Fh	E.IPC-IM20	2	Incremental encoder
220h-223h	E.IPC-AS11	2	8 LEDs / 8 buttons
220h-23Fh	E.IPC-CP40	1	Beckhoff bus controller
230h-233h	E.IPC-IO7X	5	2 analog outputs
230h-237h	E.IPC-IO6X	2	4 analog outputs
234h.237h	E.IPC-IO7X	6	2 analog outputs
240h-25Fh	E.IPC-IO1X	2	4 analog inputs
	E.IPC-CP40	2	Beckhoff bus controller
270h-273h	E.IPC-AS12	5	32 LEDs
	E.IPC-AS13	5	16 switches
	E.IPC-AS14	5	32 LEDs
278h-27Fh	E.IPC-CP70	2	Printer LPT2
280h-29Fh	E.IPC-CP40	3	Beckhoff bus controller
2A0-2A3	E.IPC-AS11	5	8 LEDs / 8 buttons
2A0h-2A3h	E.IPC-AS11	5	8 LEDs / 8 buttons
2A0h-2BFh	E.IPC-CP40	4	Beckhoff bus controller
2A4h-2A5h	E.IPC-IO4X	2	4 channel A/D converter
2A6h-2A7h	E.IPC-IO4X	5	4 channel A/D converter
2B0h-2B7h	E.IPC-IO6X	4	4 analog outputs
2C0h-2DFh	E.IPC-IO1X	4	4 analog inputs

2E0h-2E3h	E.IPC-CP80	1	CAN bus controller
2E0h-2E7h	E.IPC-CP33	-	Serial interface COM5
52E8h-2EFh	E.IPC-CP3X	-	Serial interface COM4
2F0h-2F3h	E.IPC-CP80	2	CAN bus controller
2F8h-2FFh	E.IPC-CP3X	-	Serial interface COM2
300h-301h	E.IPC-IO4X	0	4 channel A/D converter
300h-303h	E.IPC-CP80	0	CAN bus controller
	E.IPC-IO7X	0	2 analog outputs
300h-307h	E.IPC-IO6X	0	4 analog outputs
300h-31Fh	E.IPC-CP1X	1	Ethernet controller
	E.IPC-CP40	5	Beckhoff bus controller
310h-311h	E.IPC-OM20	5	8 digital inputs / 8 digital outputs
	E.IPC-OM10	5	16 digital outputs
	E.IPC-IM10	5	16 digital inputs
310h-313h	E.IPC-AS12	3	32 LEDs
	E.IPC-AS13	3	16 switches
	E.IPC-AS14	3	32 LEDs
312h-313h	E.IPC-OM10	6	16 digital outputs
	E.IPC-OM20	6	8 digital inputs / 8 digital outputs
	E.IPC-IM10	6	16 digital inputs
318h-31Fh	E.IPC-IM20	3	Incremental encoder
320h-323h	E.IPC-AS11	3	8 LEDs / 8 buttons
320h-33Fh	E.IPC-CP1X	2	Ethernet controller
330h-33Fh	E.IPC-ED11	-	Flash disk
340h-35Fh	E.IPC-CP1X	1	Ethernet controller
360h-361h	E.IPC-IO4X	2	4 channel A/D converter
360h-37Fh	E.IPC-CP1X	4	Ethernet controller
378h-37Fh	E.IPC-CP70	1	Parallel printer LPT1
3A0h-3A3h	E.IPC-AS11	6	8 LEDs / 8 switches
3A4h-3A5h	E.IPC-IO4X	3	4 channel A/D converter
3A6h-3A7h	E.IPC-IO4X	6	4 channel A/D converter
3B0h-3DFh	E.IPC-VM10	-	VGA controller
3E0h-3E1h	E.IPC-MC1X	1	PCMCIA
3E0h-3E3h	E.IPC-CP80	3	CAN bus controller
3E8h-3EFh	E.IPC-CP3X	-	Serial interface COM3
3F0h-3F7h	E.IPC-FC10	-	Diskette controller
3F8h-3FFh	E.IPC-CP3X	-	Serial interface COM1

The I²C bus addresses

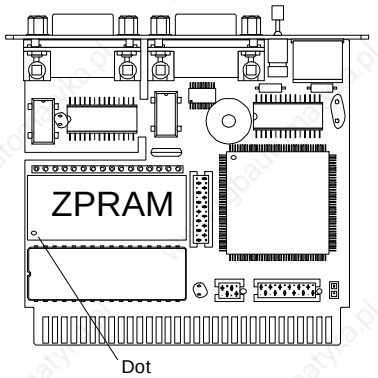
Address	Module	I²C module	Function
70h	DIS1/DIS2/BG20	SAA 1064	LED control
48h	DIS1/DIS2/BG20	PCF8574	Special functions
ACh/AEh	BG20	PCF8582	EEPROM
A0h	PS10/BP50	PCF8583	Real time clock
A2h	PS10/BP50	PCF8583	Real time clock
ACh/AEh	OMX1/IMX1/OM70	PCF8582	PLC function/EEPROM
C0h-DEh	BG10	PC16C74	LCD terminal

Maintenance

General notes regarding maintenance

As the CPU modules E.IPC-HC15, E.IPC-HC16 and E.IPC-HC17 are equipped with a ZPRAM, regular maintenance must according to the manufacturer of the ZPRAM be carried out regularly over a period of 10 years.

At the end of this period the ZPRAM module must be exchanged.



Exchanging the ZPRAM module

In order to exchange the ZPRAM module, the housing of the CPU module must be opened. The ZPRAM module should only be exchanged by trained personnel experienced in working with electronic components. Furthermore, the work must be carried out at an antistatic workplace.

Switch off all power to the E.IPC system before removing the CPU module from the E.IPC installation.

Using appropriate tools, remove the two retaining rings holding the fixing screws on the back of the module.

Now the fixing screws can be removed from the module housing and the printed circuit board taken from out of the module housing. Remove the module described on the diagram as ZPRAM by pushing a slotted screwdriver between the ZPRAM module and the socket and then carefully easing the ZPRAM module out.

Please ensure that the position of the dot marked on the module corresponds to that of the dot marked on the diagram when inserting the new ZPRAM module.

Do not forget the insulation foil when replacing the printed circuit board into the aluminium housing.

The housing can be closed again by placing the components onto the fixing screws in reverse order. Finally replace the retaining rings.

Once the module has been reassembled, it can be used as usual.

Solutions to problems

Instructions regarding fault-finding

Please, ensure that the installation instructions specified in the manual have been carried out correctly. Check that the E.IPC system has been connected with undamaged standard cables. Furthermore, it is vital to ensure that the E.IPC system is supplied with the correct voltage.

Programming

The allocation of the internal I/O addresses

From address	To address	Allocation
000h	01Fh	DMA controller (8237 compatible)
020h	03Fh	Interrupt controller (8237 compatible)
040h	05Fh	Timer (8259A compatible)
060h	062h	Keyboard interface (8255 compatible)
070h	071h	CMOS-RAM (AT compatible)
080h	08Fh	DMA page
090h	09Fh	External register
0E0h	0EFh	reserved for PLC safety functions
0F0h	0F7h	I²C bus controller
2F8h	2FFh	Internal COM2
3D8h	3DFh	Grafik controller (CGA)
3F8h	3FFh	Internal COM1

The allocation of the extension register

Address	Signal	Meaning	Active
90h	/FLCS	Switch Flash / option socket	low
91h	SWRES	Programmable bus reset	high
92h	RS232 SHDN	Deactivate SM11 module (ESD protection)	high
93h	CGA SHDN	Deactivate CGA video interface (ESD protection)	high
94h	KB SHDN	Deactivate keyboard interface (ESD protection)	high
95h	XTBUS B8	Programmable Pin B8 at PS1 bus	-
96h	SCLK CLR	Reset multiprocessor recognition (Flip-flop)	high
97h	JP1 Pin 8	Programmable pin at configuration plug JP1	
98h	-	free	
99h	/SLAVE	Slave operation	low
9Ah	/I²CRES	Reset for I²C controller	low
9Bh	LED1	Activate LED	low
9Ch	EN 36 V	Switch on +10 V ... +36 V at video connector	high
9Dh	EECS	Chip select for EEPROM	high
9Eh	EESC	Shift clock for EEPROM	high
9Fh	EEDI	Serial data for EEPROM	high

After a system start or a hardware reset, all outputs of the extension register are automatically set to low.

Note: To keep you software as compatible as possible with later CPU versions, the special function of the E.IPC-HC1X should not be programmed directly via the extension register but via the service interrupt.

The allocation of the interrupt channels

IRQ0	Reserved
IRQ1	Keyboard
IRQ2	COM4
IRQ3	COM2
IRQ4	COM1
IRQ5	COM3 / PS1-CP1X / LPT2
IRQ6	Diskette controller
IRQ7	LPT1 / shared interrupts / COM5

The allocation of the DMA channels

DMA0	Memory refresh
DMA1	I²C bus*
DMA2	Reserved for diskette controller
DMA3	free

*) The lines of the DMA channel 1 at the E.IPC bus are occupied by the I²C bus.

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Note

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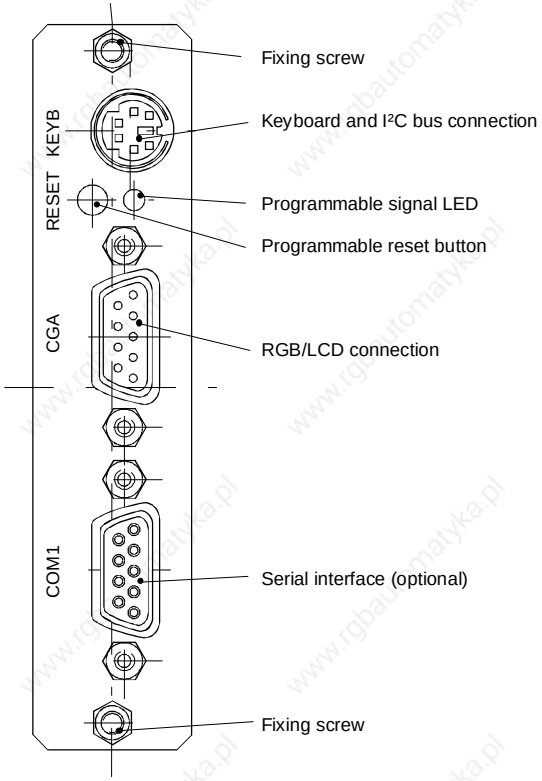
Data overview

Performance characteristics

- The computer unit of your FESTO IPC concept is software and socket compatible to the world-wide PC/XT standard, operating system MS-DOS 3.3-6.2, DR-DOS 6.0, Novell-DOS 7 or QNX 2.25
- High capacity C&T processor F8680 PC/CHIP (14 MHz, 3 MIPS, Landmark 19) with 16 bit memory access, 1 MB main memory (computing speed comparable to 386SX systems).
- CGA/LCD graphic adapter to connect to screen or LC display.
- Serial interface module (RS232, RS232 opto, RS422, RS485).
- Multiprocessor capable via software controlled decoupling from the PC/XT bus.
- ROM disk with up to 896 KB capacity or RAM/Flash disk with up to 512 KB.
- Secure attachment and high noise immunity thanks to screened electronics in an aluminium housing and electronics design conforming to EMC requirements.
- Any PC compatible computer with CGA, EGA or VGA graphics can be used as a development system.

Main details in brief

The CPU is the Heart of every FESTO IPC installation. The high-capacity E.IPC-HC1X CPU module is suitable both for control tasks and for simple visual applications thanks to its flexible PC technology. There is also the possibility of implementing low cost display and operating devices through the integrated CGA graphics interface. The SuperState BIOS and the hardware watchdog ensure that the CPU functions properly even under the most extreme operating conditions. As all configurations data is saved in an EEPROM, and batteries are therefore redundant, the E.IPC-HC1X CPU modules are absolutely maintenance-free.
Programming can be made in all common PC programming languages (Pascal, C, Basic, Assembler, etc.). Software with CGA, EGA or VGA compatible text output, or CGA compatible PC software usually runs without any modifications. Using the available PLC programming systems LogiCAD, Festo FST and PLC emulator, the CPU module can be programmed and used like a PLC.



Ratio 1:1

Physical data

- Cast aluminium housing
- Weight (g) . . . . . : 150
- Dimensions (mm) . . . . . : 75 x 21 x 96
- Max. current consumption (excl. ext. keyboard) . : max. 390 mA
- Power consumption . . . . . : 1,95 W
- Operating temperature range . . . . : 0 °C to 55 °C
- Relativy humidity (at 25 °C not condensing) . . : 10 % to 95 %
- Shock (when screwed on) . . . . : up to 15 G
- Vibration (when screwed on) . . . . : up to 2,5 G
- MTBF (at 35 °C) . . . . . : better than 100 000h

Executable operating systems, developement packages and help programs

- MS-DOS 3.3 to MS-DOS 6.2
- DR-DOS 6.0 / Novell-DOS 7
- QNX 2.25 (Real-Mode)
- Windows 3.0 (Real-Mode)
- Borland C 2.0, 3.0, 3.1*, 4.0
- Borland Pascal 5.5, 6.0, 7.0*
- MS QuickBasic 3.0, 4.5
- MS C 7.0*, MS Assembler 6.0
- Novell Netware (Workstation-Shell)
- Norton Utilities 7.0*, PCTools 8.0*
- PCAnywhere IV, Procomm Plus 2.0
- LapLink IV, Carbon Copy plus*

(* DOS versions in Real mode with CGA/EGA/VGA text mode or CGA graphics)