



<b>BASIC CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage		$V_{DD}$	2.6	3.0	3.6	V
Supply current <sup>(1)</sup>		$I_{DD}$	500	580	1000	$\mu\text{A}$
I <sup>2</sup> C signal input <sup>(1)</sup>	Logic high	$V_{IH}$	1.2	-	-	V
	Logic low	$V_{IL}$	-	-	0.4	
Peak sensitivity wavelength		$\lambda_{PC}$	-	590	-	nm
		$\lambda_{PR}$	-	610	-	
		$\lambda_{PG}$	-	560	-	
		$\lambda_{PB}$	-	470	-	
		$\lambda_{PIR}$	-	825	-	
Irradiance responsivity	520 nm LED <sup>(1)(2)</sup>	C	-	57	-	counts/( $\mu\text{W}/\text{cm}^2$ )
	850 nm LED <sup>(1)(2)</sup>	IR	-	25	-	
	643 nm LED <sup>(1)(2)</sup>	R	-	41	-	
	520 nm LED <sup>(1)(2)</sup>	G	-	39	-	
	460 nm LED <sup>(1)(2)</sup>	B	-	34	-	
Sensitivity	5000 K WLED <sup>(1)(3)</sup>	G	-	0.003	-	lx/count
Dark offset <sup>(1)(3)</sup>		R, G, B, C, IR	0	-	3	counts
Operating temperature range		$T_{amb}$	-40	-	+85	$^{\circ}\text{C}$
Shutdown current <sup>(1)</sup>	Light condition = dark	$I_{DD}$	0	800	1000	nA

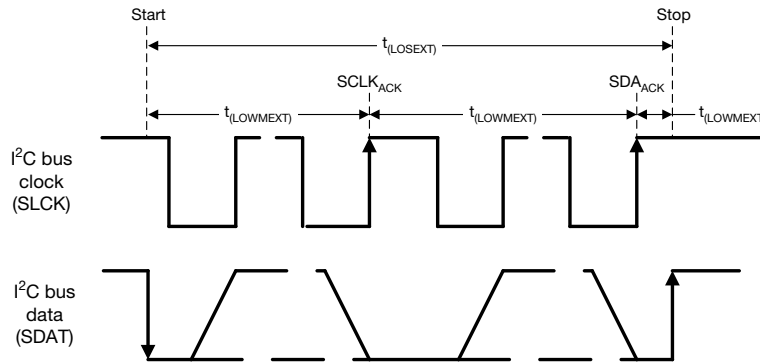
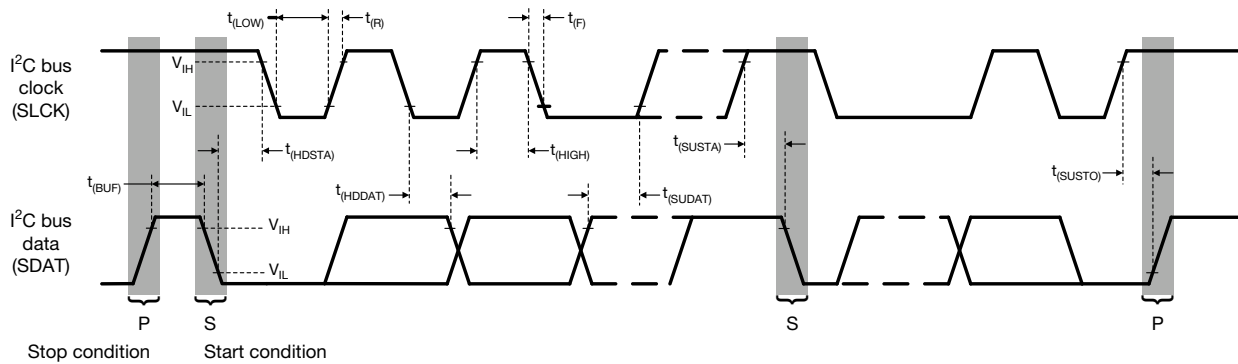
**Notes**

<sup>(2)</sup> Test condition:  $V_{DD} = 3\text{ V}$ , temperature:  $25\text{ }^{\circ}\text{C}$

<sup>(3)</sup> IT: 100 ms, SENS = (0) = x 1, DG = (0 : 0) = x 1, GAIN = (0 : 0) = x 1

<sup>(4)</sup> IT: 400 ms, SENS = (0) = x 1, DG = (1 : 0) = x 4, GAIN = (0 : 0) = x 4

<b>I<sup>2</sup>C BUS TIMING CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Clock frequency	$f_{(I2CCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	$\mu\text{s}$
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	$\mu\text{s}$
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	$\mu\text{s}$
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	$\mu\text{s}$
Data hold time	$t_{(HDDAT)}$	-	3450	-	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I <sup>2</sup> C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	$\mu\text{s}$
I <sup>2</sup> C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	$\mu\text{s}$
Clock / data fall time	$t_f$	-	300	-	300	ns
Clock / data rise time	$t_r$	-	1000	-	300	ns


 Fig. 1 - I<sup>2</sup>C Bus Timing Diagram