

International IOR Rectifier

SERIES IRK.136, .142, .162

**THYRISTOR/DIODE and
THYRISTOR/THYRISTOR**

NEW INT-A-pak Power Modules

Features

- High Voltage
- Electrically Isolated by DBC Ceramic (Al_2O_3)
- 3500 V_{RMS} Isolating Voltage
- Industrial Standard Package
- High Surge Capability
- Glass Passivated Chips
- Modules uses High Voltage Power thyristor/diodes in three Basic Configurations
- Simple Mounting
- UL E78996 approved 

135 A
140 A
160 A

Applications

- DC Motor Control and Drives
- Battery Charges
- Welders
- Power Converters
- Lighting Control
- Heat and Temperature Control

Major Ratings and Characteristics

Parameters	IRK.136..	IRK.142..	IRK.162..	Units	
$I_{T(AV)}$	135	140	160	A	
@ T_C	85	85	85	°C	
$I_{T(RMS)}$	300	310	355	A	
I_{TSM}	@ 50Hz	3200	4500	4870	A
	@ 60Hz	3360	4712	5100	A
I^2t	@ 50Hz	51.5	102	119	KA ² s
	@ 60Hz	47	92.5	108	KA ² s
$I^2\sqrt{t}$	515.5	1013	1190	KA ² √s	
V_{RRM}	400 to 1600			V	
T_J range	-40 to 125			°C	

CASE STYLE NEW INT-A-PAK



IRK.136, .142, .162 Series

Bulletin I27117 rev. C 03/02

International
IR Rectifier

Electrical Specifications

Voltage Ratings

Type number	Voltage Code	V_{RRM}/V_{DRM} , Maximum repetitive peak reverse voltage V	V_{RSM}/V_{DSM} , Maximum non-repetitive peak reverse voltage V	I_{RRM}/I_{DRM} @ 125°C mA
IRK.136	04	400	500	50
IRK.142	08	800	900	
IRK.162	12	1200	1300	
	14	1400	1500	
	16	1600	1700	

Forward Conduction

Parameter	IRK.136	IRK.142	IRK.162	Units	Conditions
$I_{T(AV)}$ Max. average on-state current @ Case temperature	135	140	160	A	180° conduction, half sine wave
	85	85	85	°C	
$I_{T(RMS)}$ Max. RMS on-state current	300	310	355	A	as AC switch
I_{TSM} Maximum peak, one-cycle on-state, non-repetitive surge current	3200	4500	4870	A	t = 10ms No voltage
	3360	4712	5100		t = 8.3ms reappplied
	2700	3785	4100		t = 10ms 100% V_{RRM}
	2800	3963	4300		t = 8.3ms reappplied
I^2t Maximum I^2t for fusing	51.5	102	119	KA ² s	t = 10ms No voltage
	47	92.5	108		t = 8.3ms reappplied
	36.5	71.6	84		t = 10ms 100% V_{RRM}
	33.3	65.4	76.7		t = 8.3ms reappplied
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	515.5	1013	1190	KA ² √s	t = 0.1 to 10ms, no voltage reappplied
$V_{T(TO)1}$ Low level value of threshold voltage	0.86	0.83	0.8	V	(16.7% × π × $I_{T(AV)}$) < I < π × $I_{T(AV)}$, @ T_J max.
$V_{T(TO)2}$ High level value of threshold voltage	1.05	1	0.98		(I > π × $I_{T(AV)}$), @ T_J max.
$r_{\theta 1}$ Low level value on-state slope resistance	2.02	1.78	1.67	mΩ	(16.7% × π × $I_{T(AV)}$) < I < π × $I_{T(AV)}$, @ T_J max.
$r_{\theta 2}$ High level value on-state slope resistance	1.65	1.43	1.38		(I > π × $I_{T(AV)}$), @ T_J max.
V_{TM} Maximum forward voltage drop	1.57	1.55	1.54	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = 25^\circ\text{C}$, 180° conduction
I_H Maximum holding current	200			mA	Anode supply = 6V initial $I_r = 30A$, $T_J = 25^\circ\text{C}$
I_L Maximum latching current	400			mA	Anode supply = 6V resistive load = 1Ω Gate pulse: 10V, 100μs, $T_J = 25^\circ\text{C}$

Switching

t_{gd} Typical delay time	1	μs	$T_J = 25^\circ\text{C}$	Gate Current=1A $dl/dt=1A/\mu s$
t_{gr} Typical rise time	2		$T_J = 25^\circ\text{C}$	$V_d=0,67\% V_{DRM}$
t_q Typical turn-off time	50 - 200		$I_{TM} = 300A$; $-di/dt = 15A/\mu s$; $T_J = T_J$ max $V_r = 50V$; $dV/dt = 20V/\mu s$; Gate 0V, 100Ω	

Blocking

I_{RRM}	Maximum peak reverse and off-state leakage current	50	mA	$T_J = 125^\circ\text{C}$
I_{DRM}				
V_{INS}	RMS isolation voltage	3500	V	50Hz, circuit to base, all terminals shorted, $t = 1\text{s}$
dV/dt	critical rate of rise of off-state voltage	1000	V/ μs	$T_J = T_{J\text{max.}}$, exponential to 67% rated V_{DRM}

Triggering

Parameter	IRK.136	IRK.142	IRK.162	Units	Conditions	
P_{GM}	Max. peak gate power			12	W	$t_p \leq 5\text{ms}$, $T_J = T_{J\text{max.}}$
$P_{G(AV)}$	Max. average gate power			3	W	$f = 50\text{Hz}$, $T_J = T_{J\text{max.}}$
I_{GM}	Max. peak gate current			3	A	$t_p \leq 5\text{ms}$, $T_J = T_{J\text{max.}}$
$-V_{GT}$	Max. peak negative gate voltage			10	V	
V_{GT}	Max. required DC gate voltage to trigger			4	V	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = T_{J\text{max.}}$ Anode supply = 6V, resistive load; $R_a = 1\Omega$
				2.5		
				1.7		
I_{GT}	Max. required DC gate current to trigger			270	mA	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = T_{J\text{max.}}$ Anode supply = 6V, resistive load; $R_a = 1\Omega$
				150		
				80		
V_{GD}	Max. gate voltage that will not trigger			0.3	V	@ $T_J = T_{J\text{max.}}$, rated V_{DRM} applied
I_{GD}	Max. gate current that will not trigger			10	mA	
di/dt	Max. rate of rise of turned-on current			300	A/ μs	@ $T_J = T_{J\text{max.}}$, $I_{TM} = 400\text{A}$ rated V_{DRM} applied

Thermal and Mechanical Specifications

Parameter	IRK.136	IRK.142	IRK.162	Units	Conditions	
T_J	Max. junction operating temperature range			-40 to 125	$^\circ\text{C}$	
T_{stg}	Max. storage temperature range			-40 to 150	$^\circ\text{C}$	
R_{thJC}	0.18	0.18	0.16	K/W	DC operation, per junction	
R_{thCS}	Max. thermal resistance, case to heatsink			0.05	K/W	Mounting surface smooth, flat and greased Per module
T	Mounting IAP to heatsink	4 to 6		Nm	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	
	torque $\pm 10\%$ busbar to IAP	4 to 6				
wt	Approximate weight			200 (7.1)	g(oz)	
	Case Style			New Int-A-Pak		

ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Devices	Sinusoidal conduction @ $T_J\text{max.}$					Rectangular conduction @ $T_J\text{max.}$					Units
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
IRK.136	0.007	0.01	0.013	0.0155	0.017	0.009	0.012	0.014	0.015	0.017	K/W
IRK.142	0.0019	0.0019	0.0020	0.0020	0.0021	0.0018	0.0022	0.0023	0.0023	0.0020	
IRK.162	0.0030	0.0031	0.0032	0.0033	0.0034	0.0029	0.0036	0.0039	0.0041	0.0040	

IRK.136, .142, .162 Series

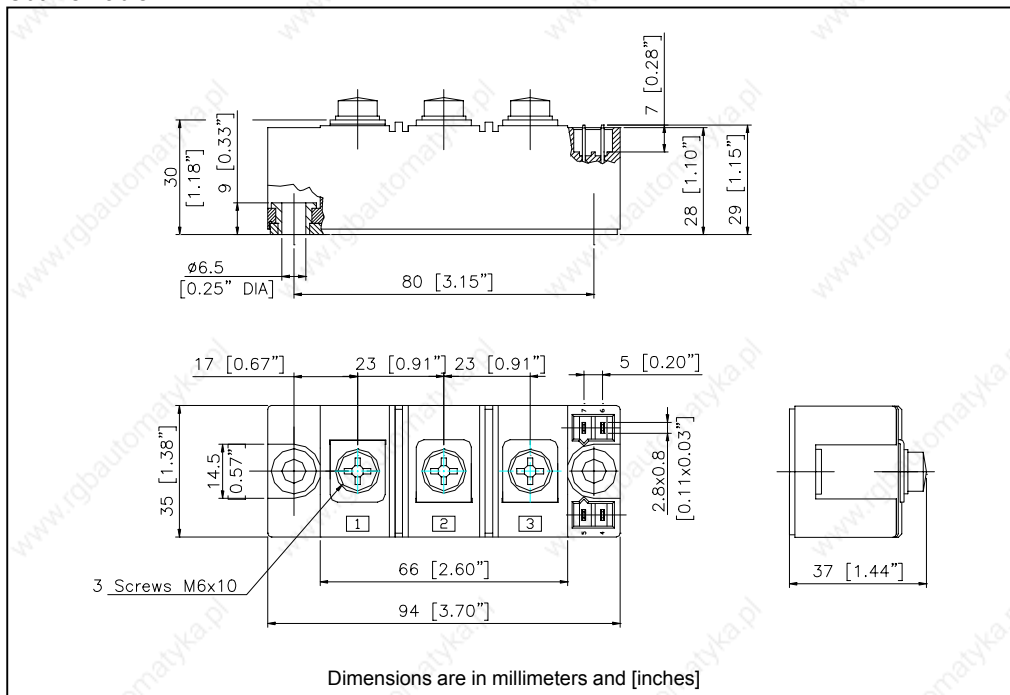
Bulletin I27117 rev. C 03/02

International
IOR Rectifier

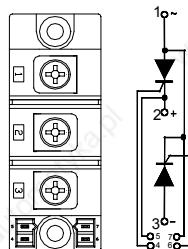
Ordering Information Table

Device Code				
1	2	3	4	
IRK	T	162	/	16
1	- Module Type			
2	- Circuit Configuration			
3	- Current Rating: $I_{T(AV)}$			
4	- Voltage Code: Code x 100 = V_{RRM}			

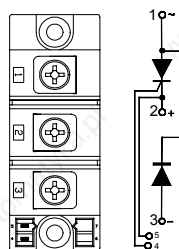
Outline Table



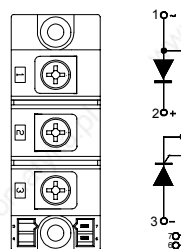
IRKT



IRKH



IRKL



NOTE: To order the Optional Hardware see Bulletin I27900

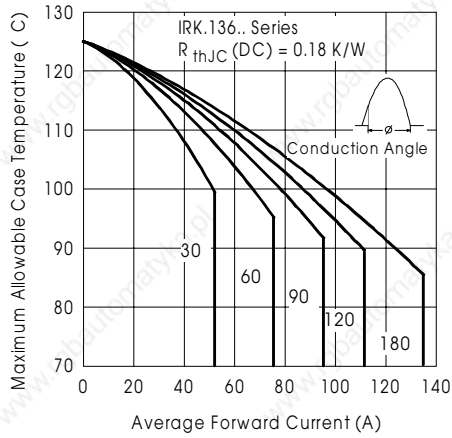


Fig. 1 - Current Ratings Characteristics

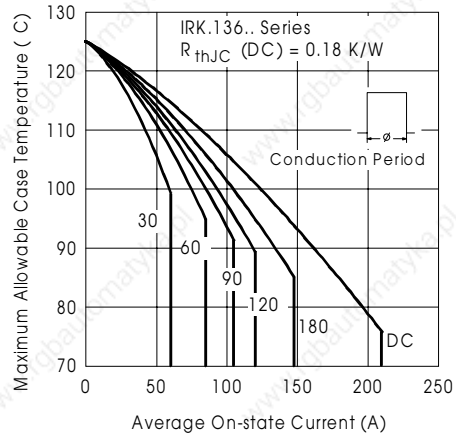


Fig. 2 - Current Ratings Characteristics

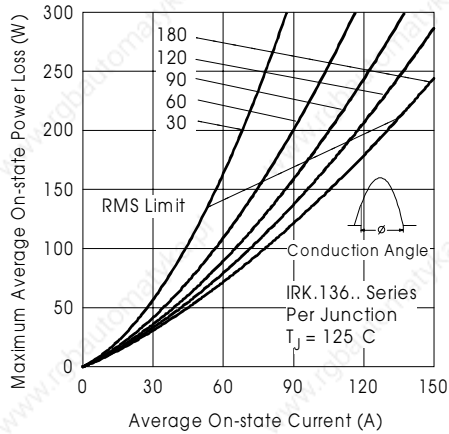


Fig. 3 - On-State Power Loss Characteristics

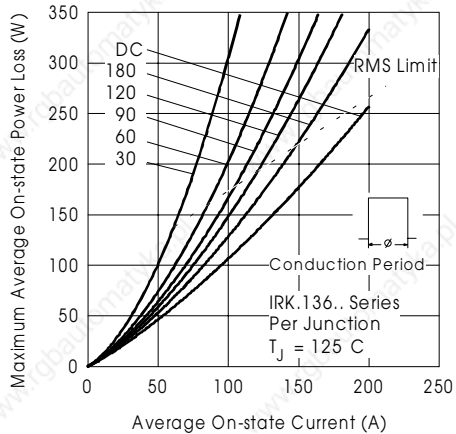


Fig. 4 - On-State Power Loss Characteristics

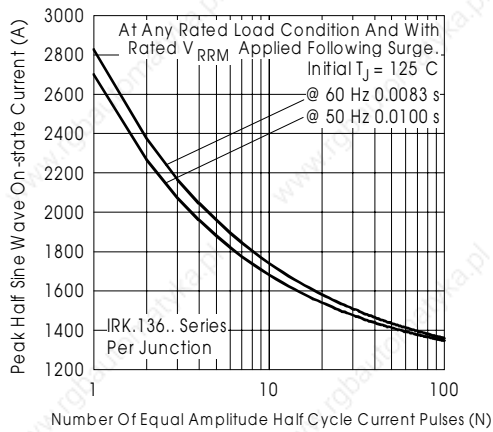


Fig. 5 - Maximum Non-Repetitive Surge Current

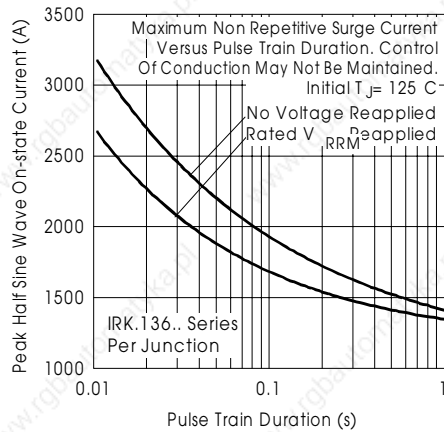


Fig. 6 - Maximum Non-Repetitive Surge Current

IRK.136, .142, .162 Series

Bulletin I27117 rev. C 03/02

International
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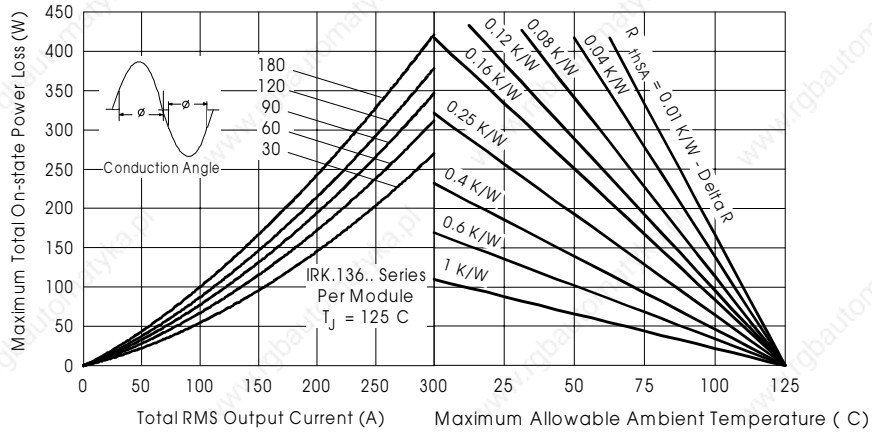


Fig.7 - On State Power Loss Characteristics

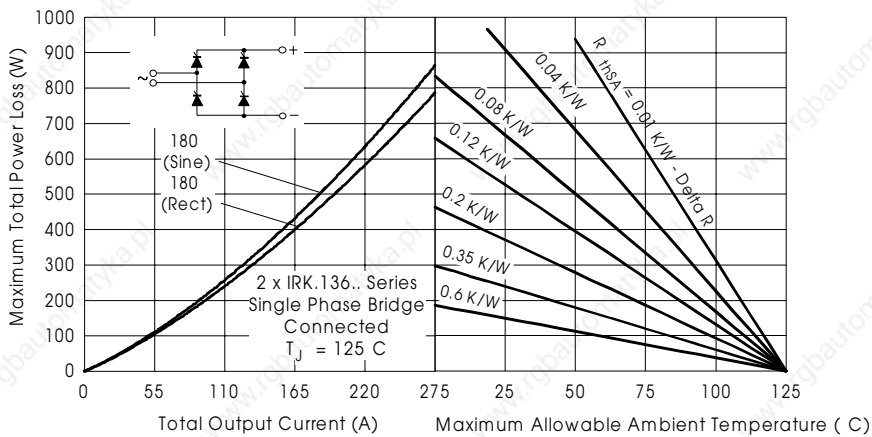


Fig.8 - On State Power Loss Characteristics

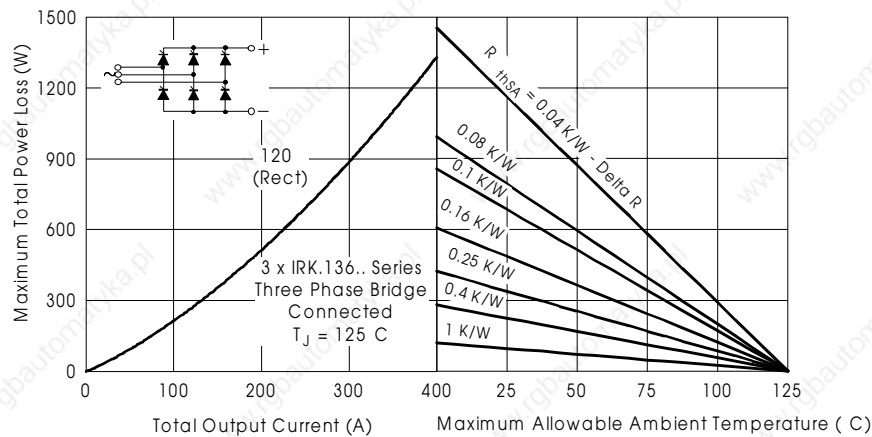


Fig.9 - On State Power Loss Characteristics

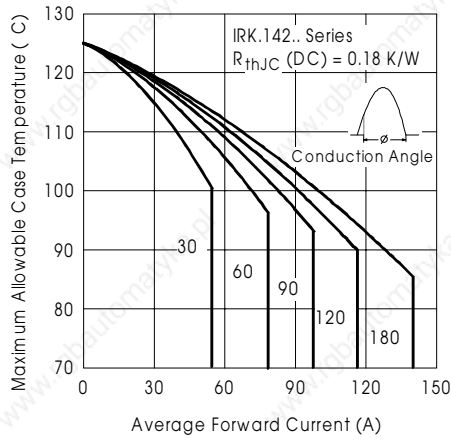


Fig. 10 - Current Ratings Characteristics

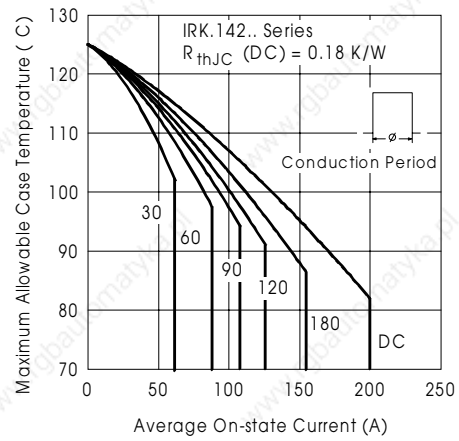


Fig. 11 - Current Ratings Characteristics

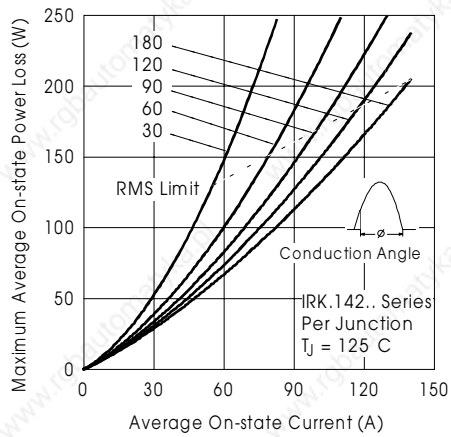


Fig. 12 - On-State Power Loss Characteristics

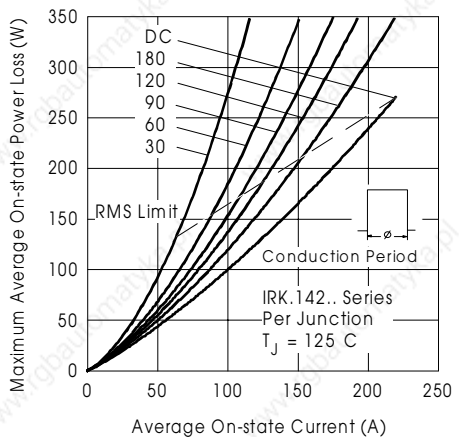


Fig. 13 - On-State Power Loss Characteristics

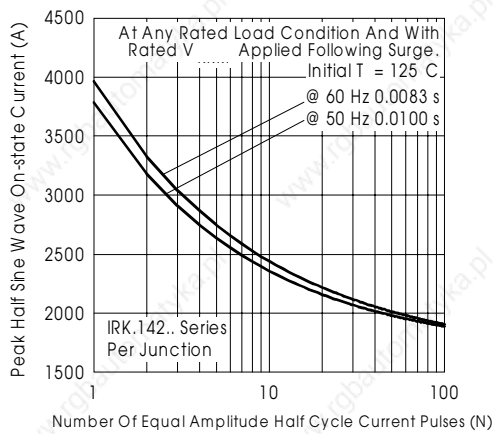


Fig. 14 - Maximum Non-Repetitive Surge Current

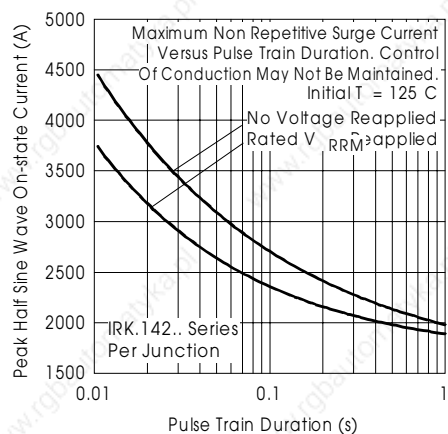


Fig. 15 - Maximum Non-Repetitive Surge Current

IRK.136, .142, .162 Series

Bulletin I27117 rev. C 03/02

International
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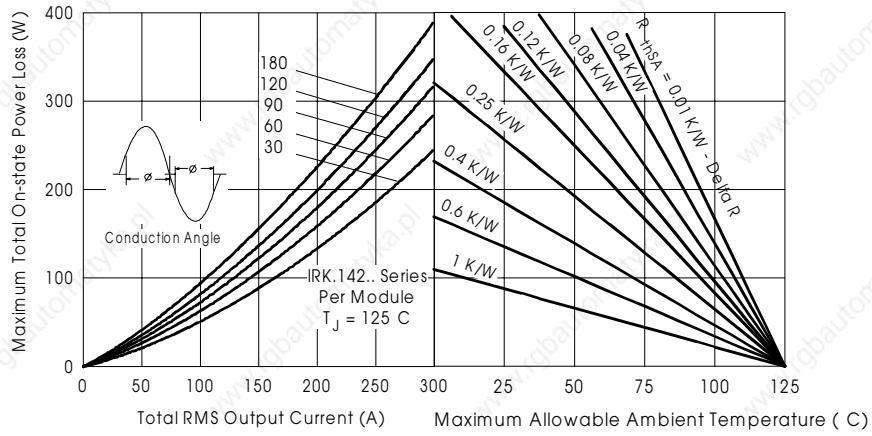


Fig.16 - On State Power Loss Characteristics

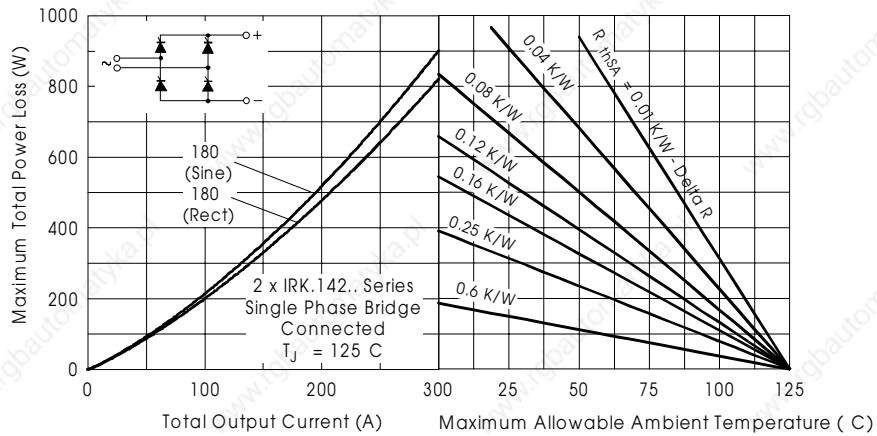


Fig.17 - On State Power Loss Characteristics

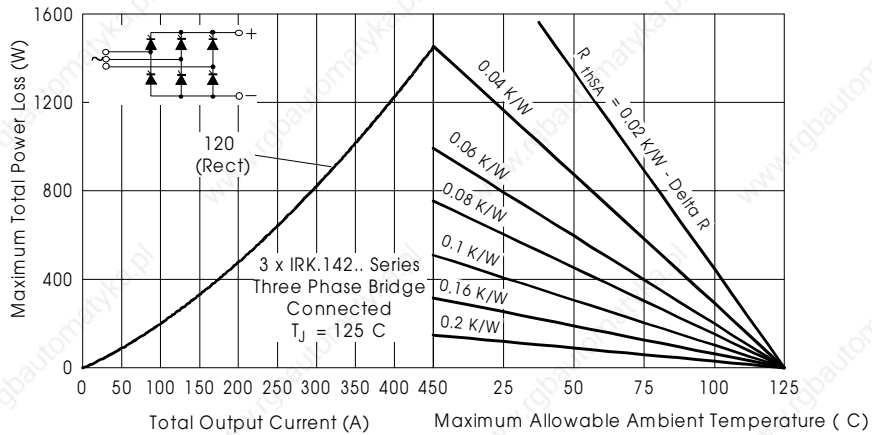


Fig.18 - On State Power Loss Characteristics

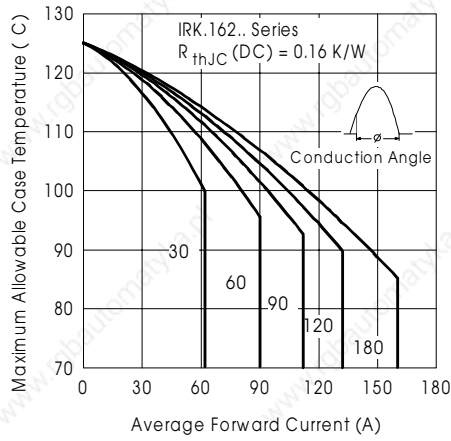


Fig. 19 - Current Ratings Characteristics

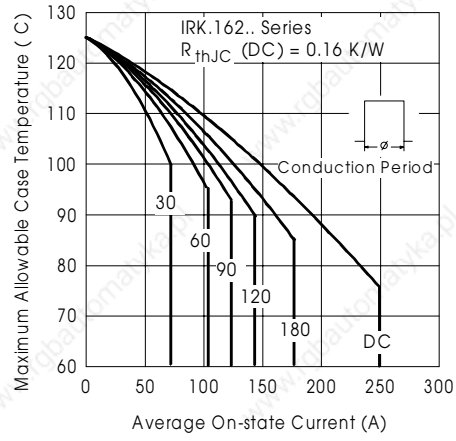


Fig. 20 - Current Ratings Characteristics

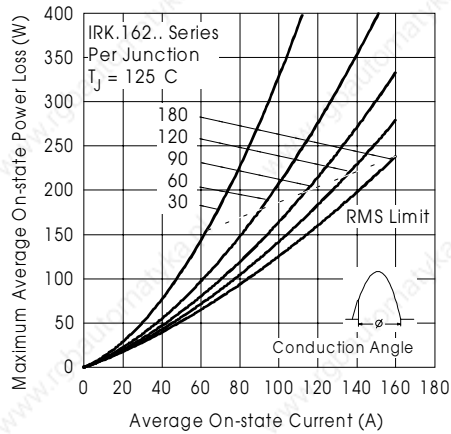


Fig. 21 - On-State Power Loss Characteristics

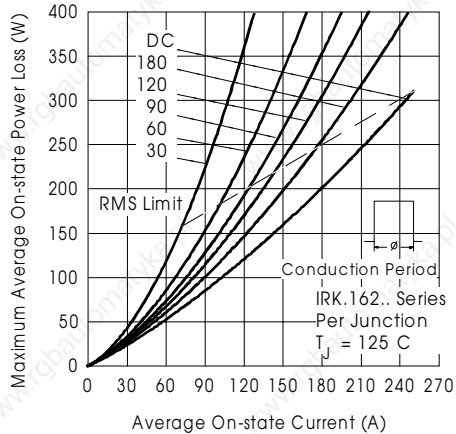


Fig. 22 - On-State Power Loss Characteristics

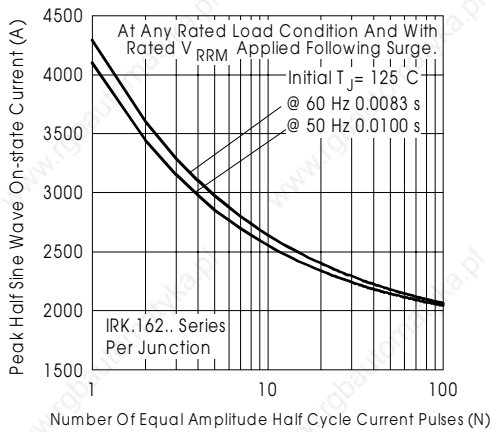


Fig. 23 - Maximum Non-Repetitive Surge Current

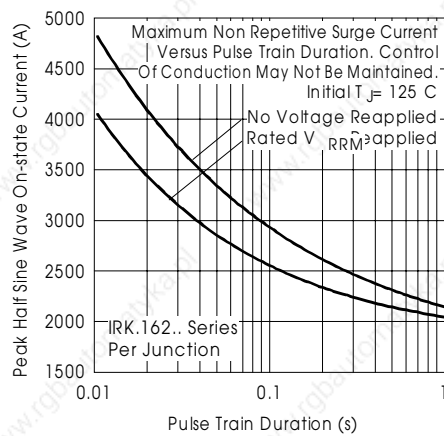


Fig. 24 - Maximum Non-Repetitive Surge Current

IRK.136, .142, .162 Series

Bulletin I27117 rev. C 03/02

International
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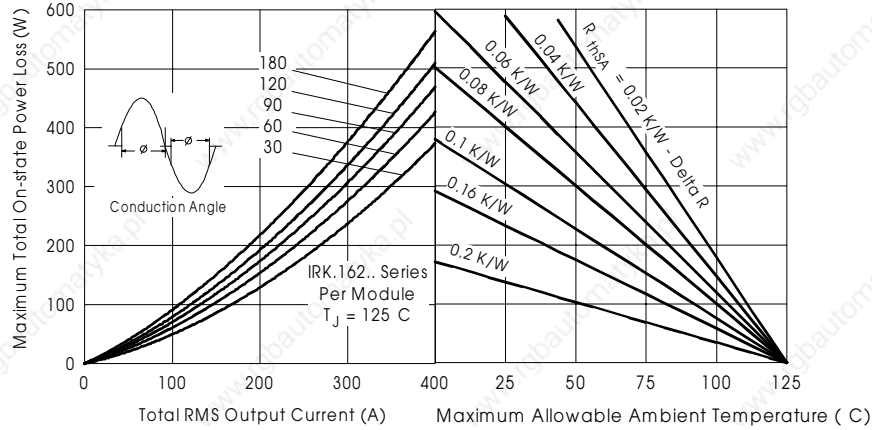


Fig.25 - On State Power Loss Characteristics

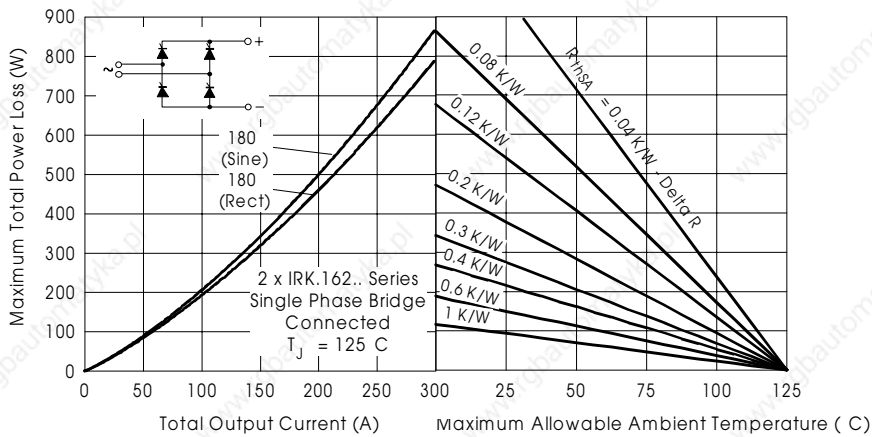


Fig.26 - On State Power Loss Characteristics

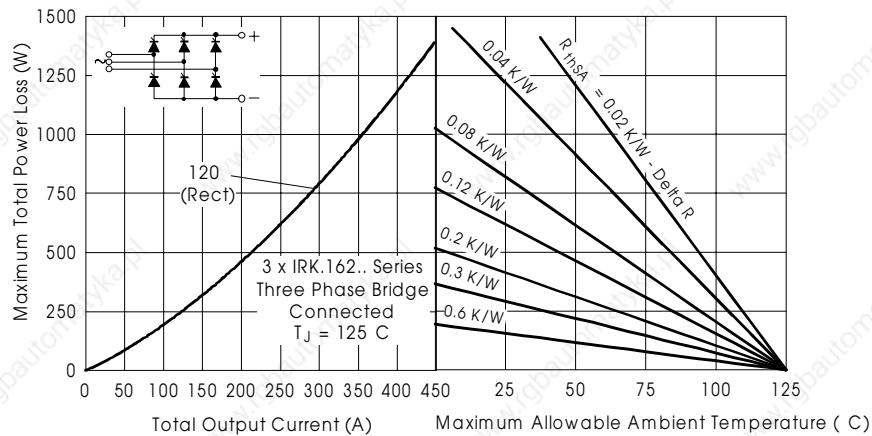


Fig.27 - On State Power Loss Characteristics

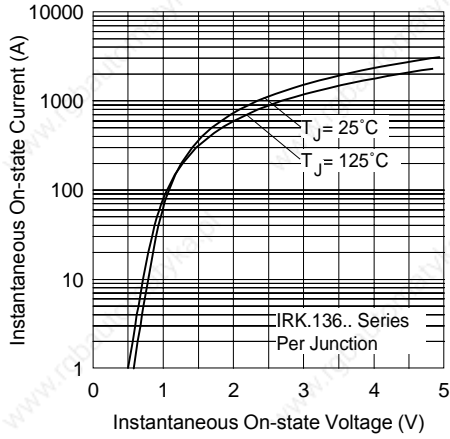


Fig.28 - On State Voltage Drop Characteristics

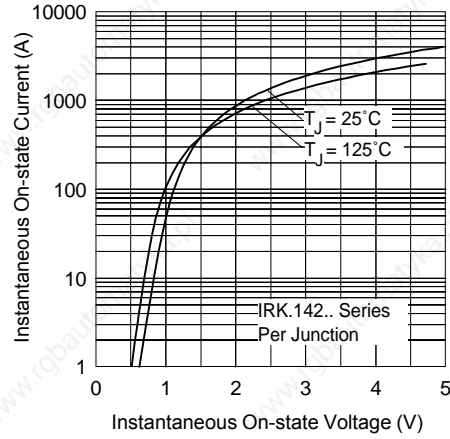


Fig.29 - On State Voltage Drop Characteristics

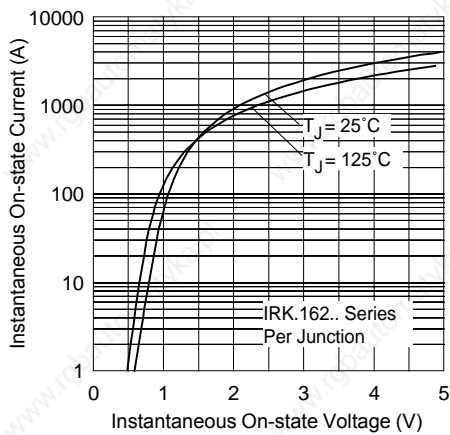


Fig.30 - On State Voltage Drop Characteristics

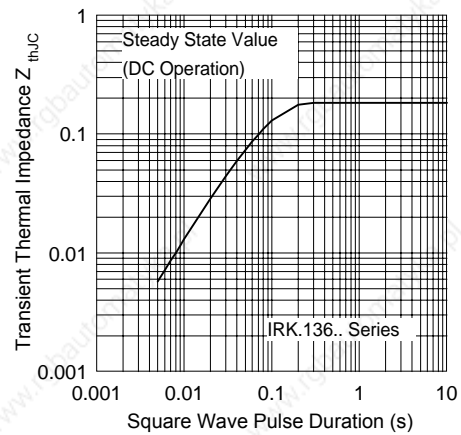


Fig.31 - Thermal Impedance ZthJC Characteristics

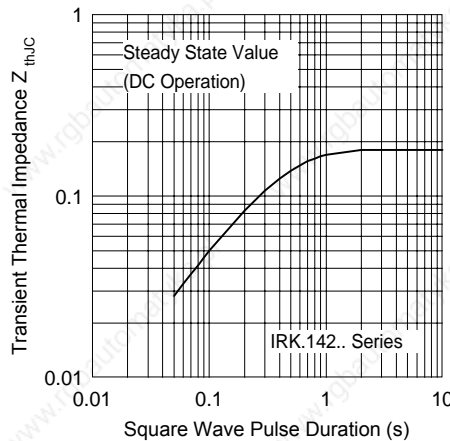


Fig.32 - Thermal Impedance ZthJC Characteristics

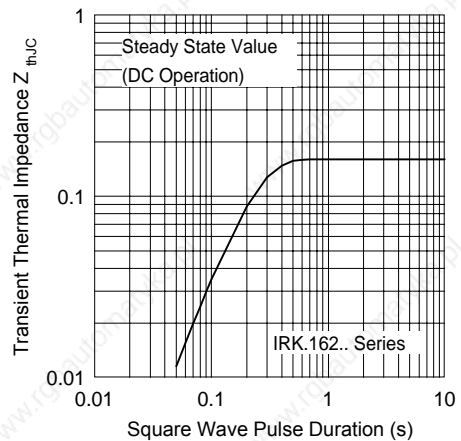


Fig.33 - Thermal Impedance ZthJC Characteristics

IRK.136, .142, .162 Series

Bulletin I27117 rev. C 03/02

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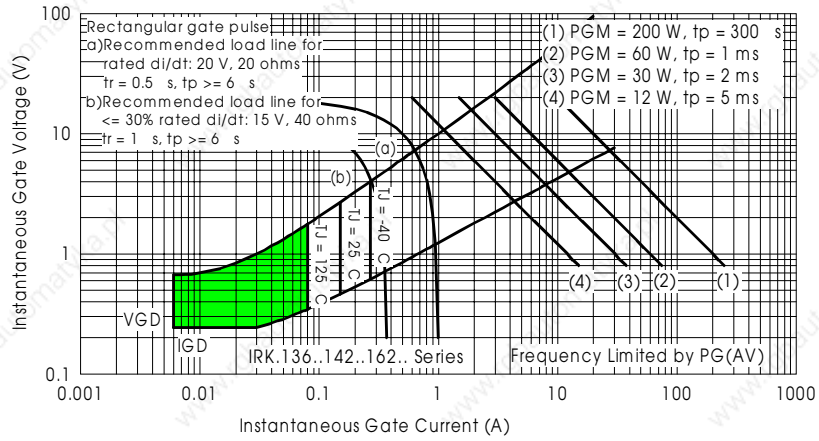


Fig. 34 - Gate Characteristics

Data and specifications subject to change without notice.
 This product has been designed and qualified for Multiple Level.
 Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7309
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