

KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

T-4623-12

8K x 8 Bit Static RAM

FEATURES

- Fast Access Time: 70,100,120 ns (max.)
- Low Power Dissipation
Standby (CMOS): 10 μ W (typ.) L-Version
5 μ W (typ.) LL-Version
- Operating: 220mW (max.)
- Single 5V \pm 10% Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
—No clock or refresh required
- Three State Output
- Low Data Retention Voltage: 2V (min.)
- JEDEC Standard pin Configuration
KM6264A/AL/AL-L: 28-pin DIP (600 mil.)
KM6264AG/ALG/ALG-L: 28-pin SOP (330 mil.)

GENERAL DESCRIPTION

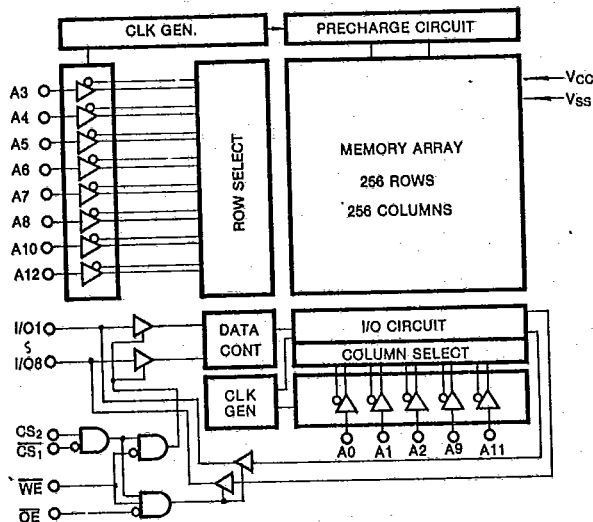
The KM6264A/AL/AL-L is a 65,536-bit high-speed Static Random Access Memory organized as 8,192 words by 8 bit.

The device is fabricated using Samsung's advanced CMOS process.

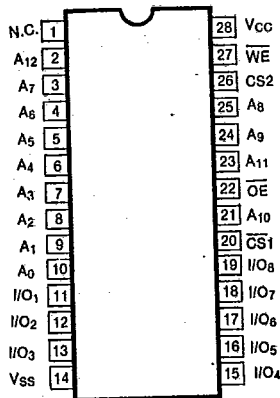
The KM6264A/AL/AL-L has an output enable input for precise control of the data outputs. It also has chip select inputs for the minimum current power down mode.

The KM6264A/AL/AL-L has been designed for high speed and low power applications. It is particularly well suited for battery back-up nonvolatile memory applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



Pin Name	Pin Function
A ₀ -A ₁₂	Address Inputs
WE	Write Enable
CS ₁ , CS ₂	Chip Select
OE	Output Enable
I/O ₁ -I/O ₈	Data Inputs/Outputs
V _{CC}	Power (+ 5V)
V _{SS}	Ground
N.C.	No Connection

KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

T-46-23-12

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.5 to 7.0	V
Power Dissipation	P _D	1.0	W
Storage Temperature	T _{stg}	-65 to +150	°C
Operating Temperature	T _A	0 to 70	°C
Soldering Temperature and Time	T _{solder}	260°C, 10 sec (Lead only)	—

*Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5*	—	0.8	V

* V_{IL}(min.) = -3.0V for ≤50ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V ± 10%, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ*	Max	Unit
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{CC}	-2		2	μA
Output Leakage Current	I _{LO}	CS1 = V _{IH} or CS2 = V _{IL} or WE = V _{IL} V _{IO} = V _{SS} to V _{CC}	-2		2	μA
Operating Power Supply Current	I _{CC1}	V _{IN} = V _{IH} or V _{IL} CS1 = V _{IL} , CS2 = V _{IH} , I _{IO} = 0mA			40	mA
Average Operating Current	I _{CC2}	Min Cycle, 100% Duty CS1 = V _{IL} , CS2 = V _{IH} , I _{IO} = 0mA		35	70	mA
Standby Power Supply Current	I _{SB}	CS1 = V _{IH} or CS2 = V _{IL}			3	mA
					1	mA
	I _{SB1}	CS1 ≥ V _{CC} - 0.2V, CS2 ≤ 0.2V or CS2 ≥ V _{CC} - 0.2V	L	2	100	μA
			LL	1	30	μA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA			0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4			V

* Typ.: V_{CC}=5V, T_A=25°C

KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

T-46-23-12

CAPACITANCE (f = 1MHz, T_A = 25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
Input/Output Capacitance	C _{IO}	V _{IO} = 0V	—	8	pF

* Note: Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS

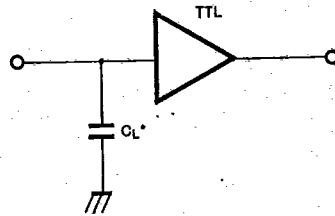
TEST CONDITIONS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 100*pF + 1 TTL Load



* C_L = 30pF for KM6264A/AL-7/7L

TEST CIRCUIT



* Including Scope and Jlg Capacitance

READ CYCLE

Parameter	Symbol	KM6264A-7 KM6264AL-7 KM6264AL-7L		KM6264A-10 KM6264AL-10 KM6264AL-10L		KM6264A-12 KM6264AL-12 KM6264AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	70		100		120		ns
Address Access Time	t _{AA}		70		100		120	ns
Chip Select to Output	t _{CO1} , t _{CO2}		70		100		120	ns
Output Enable to Valid Output	t _{OE}		35		50		60	ns
Chip Enable to Low-Z Output	t _{LZ1} , t _{LZ2}	5		10		10		ns
Output Enable to Low-Z Output	t _{OLZ}	5		5		5		ns
Chip Disable to High-Z Output	t _{HZ1} , t _{HZ2}	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t _{OHz}	0	30	0	35	0	40	ns
Output Hold from Address Change	t _{OH}	10		10		10		ns

KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

T-46-23-12

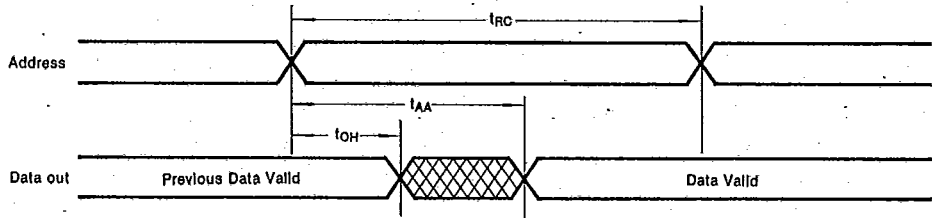
WRITE CYCLE

Parameter	Symbol	KM6264A-7 KM6264AL-7 KM6264AL-7L		KM6264A-10 KM6264AL-10 KM6264AL-10L		KM6264A-12 KM6264AL-12 KM6264AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		100		120		ns
Chip Select to End of Write	t_{CW}	60		80		85		ns
Address Set-Up Time	t_{AS}	0		0		0		ns
Address Valid to End of Write	t_{AW}	60		80		85		ns
Write Pulse Width	t_{WP}	40		60		70		ns
Write Recovery Time	t_{WR}	0		0		0		ns
Write to Output High-Z	t_{WHZ}	0	30	0	30	0	30	ns
Data to Write Time Overlap	t_{DW}	30		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	5		5		10		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE NO. 1

(CS1 = $\overline{OE} = V_{IL}$, CS2 = $\overline{WE} = V_{IH}$)

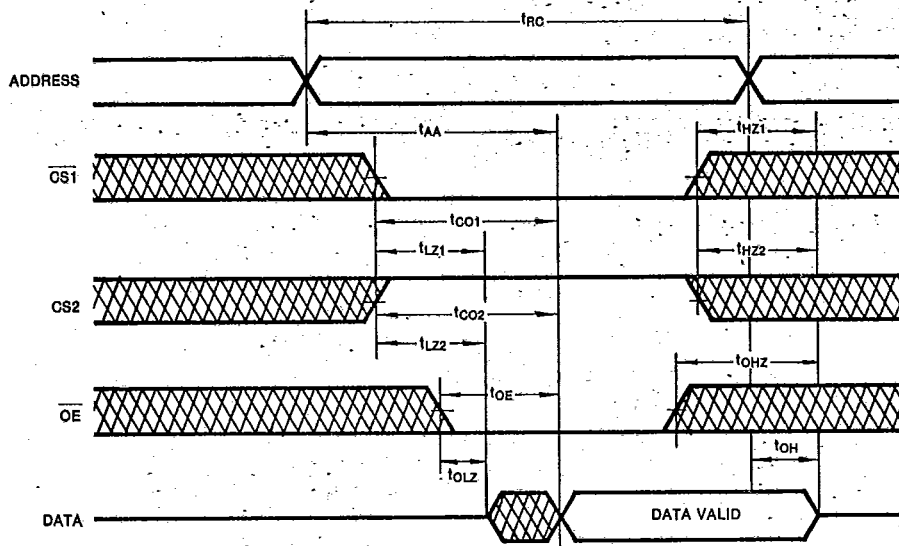


KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{WE} = V_{IH}$)

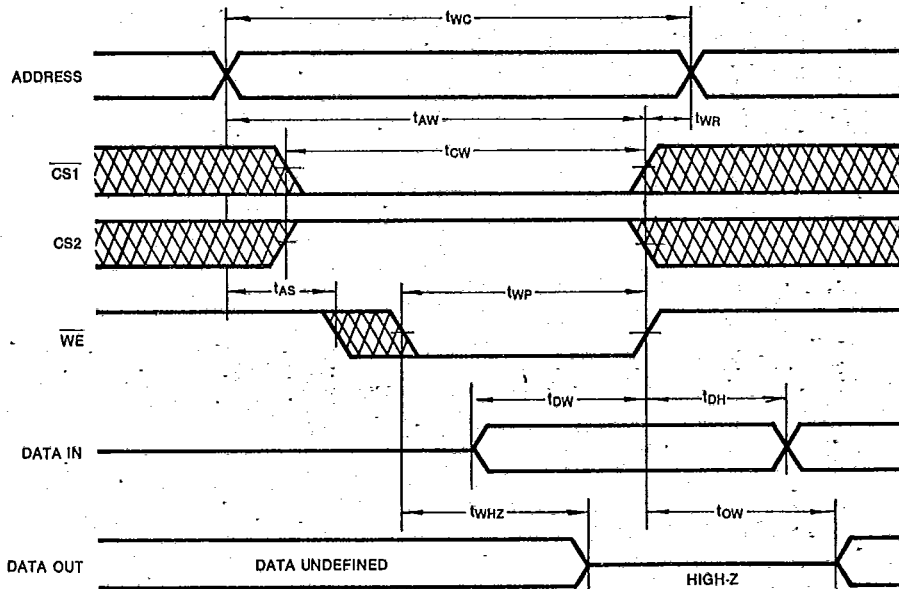
T-46-23-12



Note (READ CYCLE)

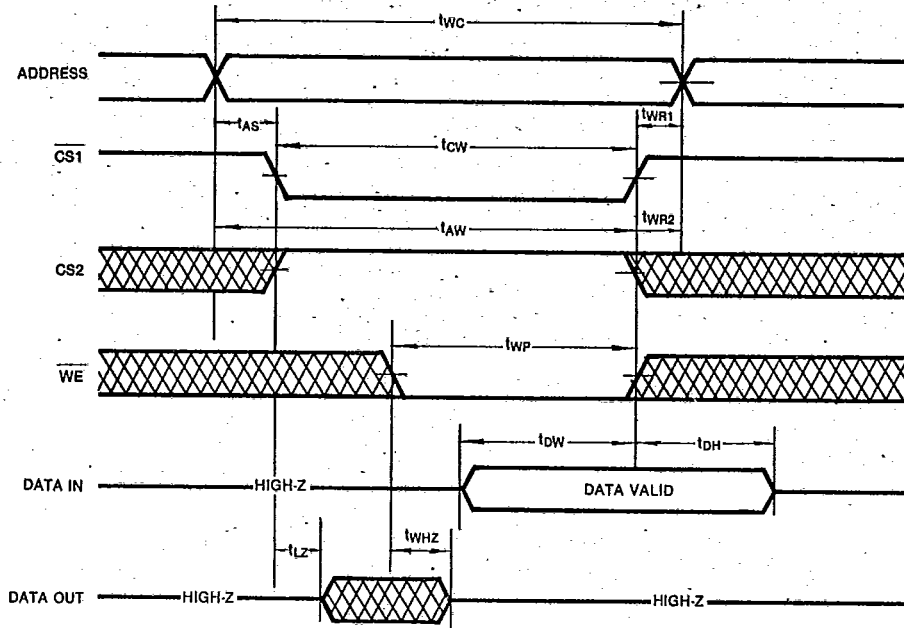
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
2. At any given temperature and voltage condition, $t_{HZ}(\max)$ is less than $t_{LZ}(\min)$ both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (\overline{WE} Controlled)

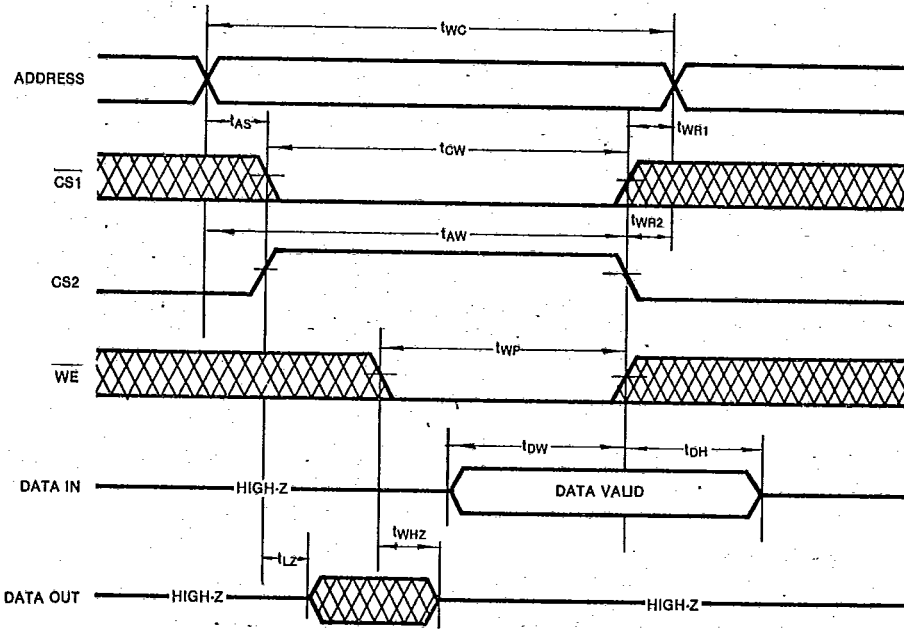


TIMING WAVEFORM OF WRITE CYCLE (CS1 Controlled)

T-46-23-12



TIMING WAVEFORM OF WRITE CYCLE (CS2 Controlled)



KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

T-46-2312

Notes (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, $CS2$ going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or $CS2$ going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as $\overline{CS1}$, or \overline{WE} going high, t_{WR2} applied in case a write ends at $CS2$ going low.
5. If \overline{OE} , $CS2$ and \overline{WE} are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
7. D_{OUT} is the read data of the new address.
8. When $\overline{CS1}$ is low and $CS2$ is high; I/O pins are in the output state. The input signals in the opposite phase leading to the outputs should not be applied.



FUNCTIONAL DESCRIPTION

$\overline{CS1}$	$CS2$	\overline{WE}	\overline{OE}	Mode	I/O Pin	V_{CC} Current
H	X	X	X	Power Down	High-Z	I_{SA}
X*	L	X	X	Power Down	High-Z	I_{SA}
L	H	H	H	Output Disable	High-Z	I_{CC}
L	H	H	L	Read	D_{OUT}	I_{CC}
L	H	L	X	Write	D_{IN}	I_{CC}

* Note: X means Don't Care.

KM6264A/KM6264AL/KM6264AL-L

CMOS SRAM

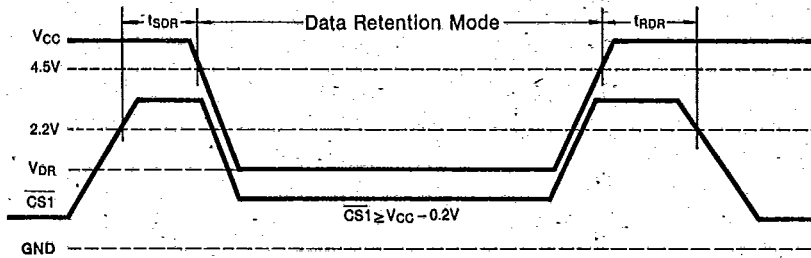
T-46-23-12

DATA RETENTION CHARACTERISTICS (T_A = 0 to 70°C)

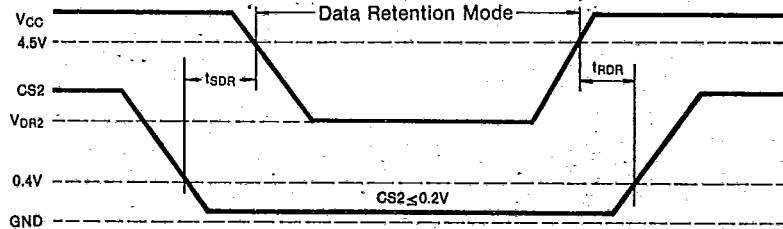
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V _{CC} for Data Retention	V _{DR}	CS1 ≥ V _{CC} - 0.2V ⁽¹⁾	2.0		5.5	V
Data Retention Current	I _{DR}	V _{CC} = 3V CS1 ≥ V _{CC} - 0.2V, CS2 ≥ V _{CC} - 0.2V or CS2 ≤ 0.2V	L	1	50	μA
			LL	0.5	10 ⁽²⁾	μA
Data Retention Set-up Time	t _{SDR}	See Data Retention Wave forms (below)	0			ns
Recovery Time	t _{RDR}		t _{RC} ⁽³⁾			ns

- (1) CS1 ≥ V_{CC} - 0.2V, CS2 ≥ V_{CC} - 0.2V (CS1 Controlled) or CS2 ≤ 0.2V (CS2 Controlled)
- (2) 1μA (max.) at 0°C ~ 40°C
- (3) t_{RC} = Read cycle time

DATA RETENTION WAVEFORM (1) (CS1 Controlled)



DATA RETENTION WAVEFORM (2) (CS2 Controlled)



KM6264A/KM6264AL/KM6264AL-L

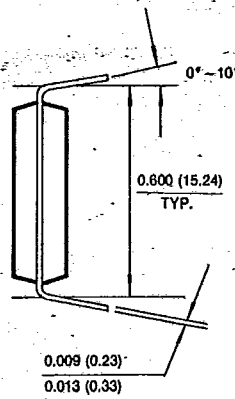
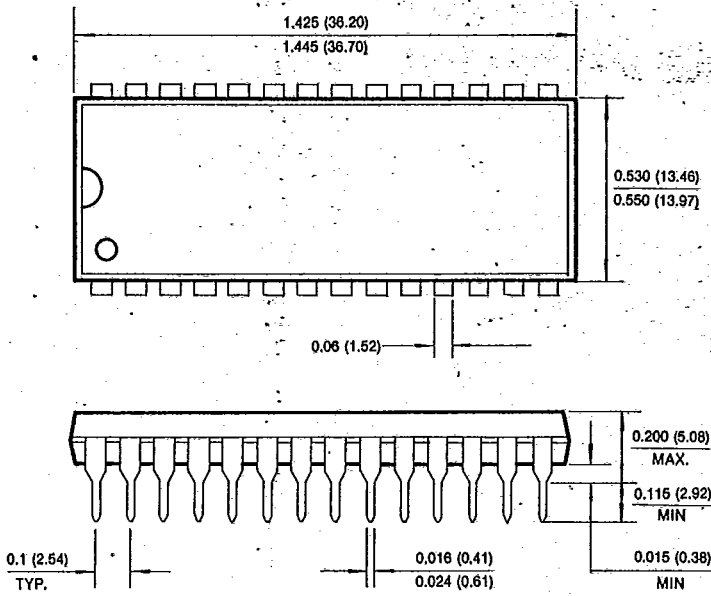
CMOS SRAM

PACKAGE DIMENSIONS

28 PIN PLASTIC DUAL IN LINE PACKAGE

T-46-23-12

Unit: Inches (Millimeters)



28 PIN PLASTIC SMALL OUT LINE PACKAGE

