

## Description

The μPD43256A is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43256A a high-speed device that requires very low power and no clock or refreshing.

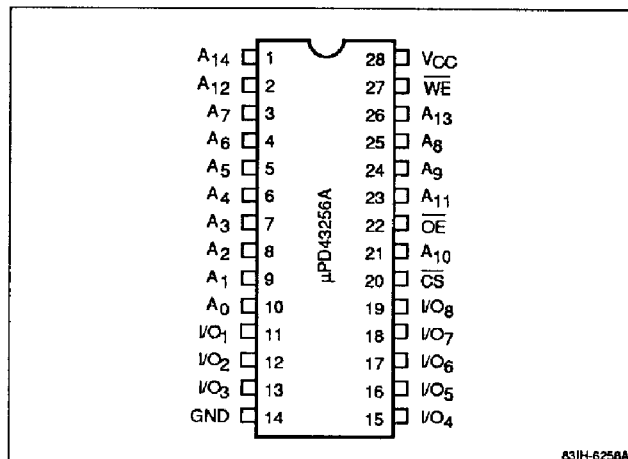
Minimum standby power is drawn when  $\overline{CS}$  is high, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256A is available in standard 28-pin plastic DIP, 28-pin plastic miniflat, or 32-pin plastic TSOP packaging.

## Features

- Single +5-volt power supply
- Fully static operation—no clock or refreshing required
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One  $\overline{CS}$  pin and one  $\overline{OE}$  pin for easy application
- Data retention of 2 V minimum
- Standard 28-pin plastic DIP and miniflat packaging
- Standard 32-pin plastic TSOP packaging (with either normal or reverse bent leads)

## Pin Configurations

### 28-Pin Plastic DIP or Miniflat



631H-6256A

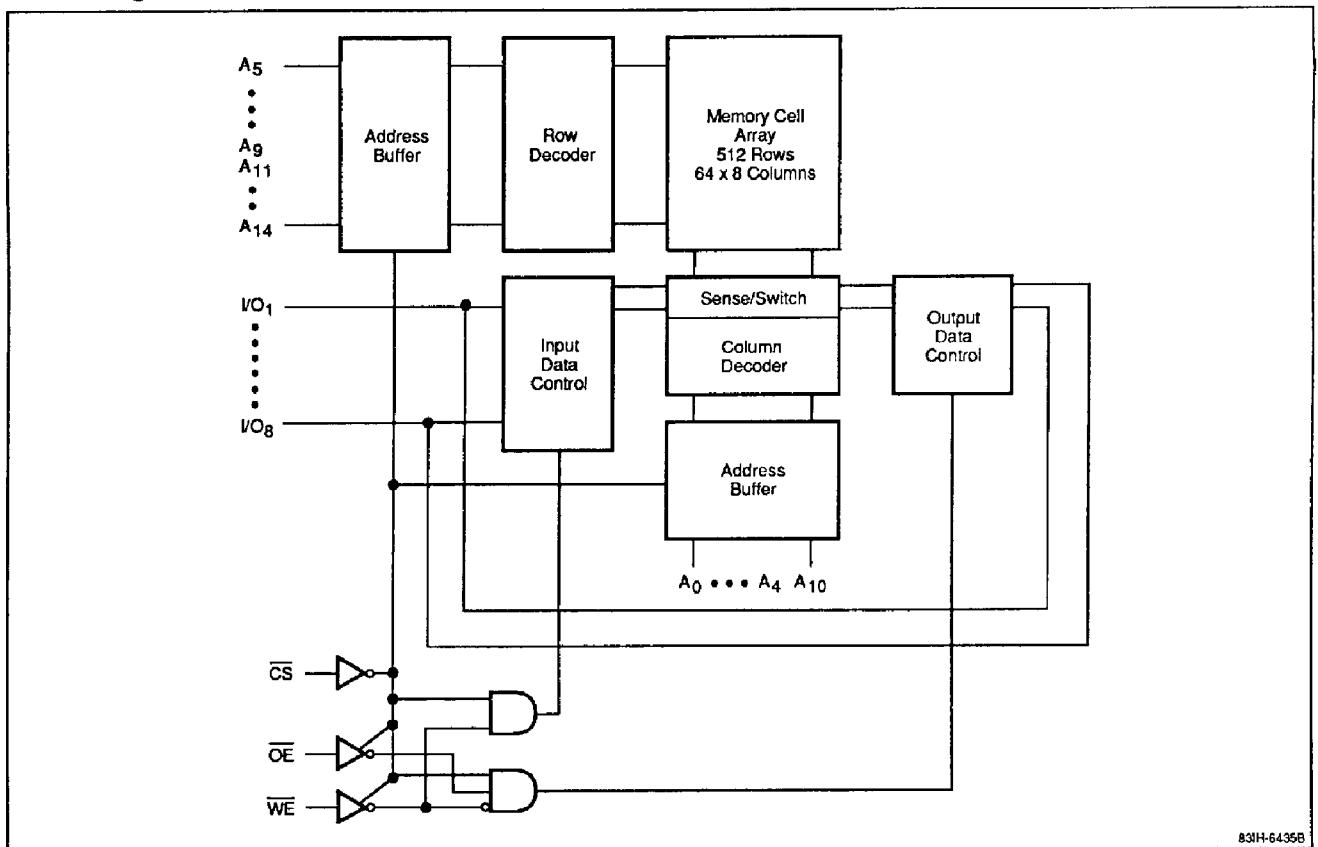
## Pin Identification

Symbol	Function
A <sub>0</sub> - A <sub>14</sub>	Address inputs
I/O <sub>1</sub> - I/O <sub>8</sub>	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V <sub>CC</sub>	+5-volt power supply
NC	No connection

### Ordering Information

Catalog Part Number	Access Time (max)	Data Retention Current (max) T <sub>A</sub> = 0 to 70°C(max)	Package
μPD43256AC-85L	85 ns	50 μA	28-pin plastic DIP(600 mil)
C-10L	100 ns		
C-12L	120 ns		
C-15L	150 ns		
μPD43256AC-85LL	85 ns	20 μA	28-pin plastic DIP(600 mil)
C-10LL	100 ns		
C-12LL	120 ns		
C-15LL	150 ns		
μPD43256AGU-85L	85 ns	50 μA	28-pin plastic miniflat
GU-10L	100 ns		
GU-12L	120 ns		
GU-15L	150 ns		
μPD43256AGU-85LL	85 ns	20 μA	28-pin plastic miniflat
GU-10LL	100 ns		
GU-12LL	120 ns		
GU-15LL	150 ns		
μPD43256AGX-10L	100 ns	50 μA	32-pin plastic TSOP (normal pinouts)
GX-12L	1200 ns		
μPD43256AGX-10LL	100 ns	20 μA	
GX-12LL	120 ns		
μPD43256AGXM-10L	100 ns	50 μA	32-pin plastic TSOP (reverse pinouts)
GXM-12L	1200 ns		
μPD43256AGXM-10LL	100 ns	20 μA	
GXM-12LL	120 ns		

# Block Diagram



83IH-6435B

### Absolute Maximum Ratings

Supply voltage, $V_{CC}$ (Note 1)	-0.5 to +7.0 V
Input voltage, $V_{IN}$ (Note 1)	-0.5 to $V_{CC} + 0.5$ V
Output voltage, $V_{IO}$ (Note 1)	-0.5 to $V_{CC} + 0.5$ V
Operating temperature, $T_{OPR}$	0 to +70°C
Storage temperature, $T_{STG}$	-55 to +125°C
Power dissipation, $P_D$	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

#### Notes:

(1) -3.0 V minimum (pulse width = 50 ns).

### Capacitance

$T_A = +25^\circ\text{C}$ ;  $f = 1$  MHz;  $V_{IN}$  and  $V_{OUT} = 0$  V

Parameter	Symbol	Min	Max	Unit
Input capacitance	$C_I$		5	pF
Input/output capacitance	$C_{IO}$		8	pF

#### Notes:

(1) This parameter is sampled and not 100% tested.

### DC Characteristics

$T_A = 0$  to +70°C;  $V_{CC} = +5.0$  V  $\pm 10\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	$I_{LI}$	-1		1	μA	$V_{IN} = 0$ V to $V_{CC}$
I/O leakage current	$I_{LO}$	-1		1	μA	$V_{IO} = 0$ V to $V_{CC}$ ; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	$I_{CCA1}$			45	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{IO} = 0$ V (Note 1)
	$I_{CCA2}$			10	mA	$\overline{CS} = V_{IL}$ ; $I_{IO} = 0$ V
	$I_{CCA3}$			10	mA	$\overline{CS} \leq 0.2$ V; $f = 1$ MHz; $I_{IO} = 0$ V; $V_{IL} \leq 0.2$ V; $V_{IH} \geq V_{CC} - 0.2$ V
Standby supply current	$I_{SB}$			3	mA	$\overline{CS} \geq V_{IH}$
	$I_{SB1}$		0.002	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2$ V (Note 2)
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 2.1$ mA
Output voltage, high	$V_{OH1}$	2.4			V	$I_{OH} = -1.0$ mA
	$V_{OH2}$	$V_{CC} - 0.5$			V	$I_{OH} = -0.1$ mA

#### Notes:

(1) μPD43256A-10L/-10LL/-12L/-12LL = 40 mA (max).

μPD43256A-15L/-15LL = 35 mA (max).

(2) μPD43256AGX-10LL/-12LL = 50 μA (max).

### Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	$I_{CC}$
H	X	X	Not selected	High-Z	Standby
L	H	H	Not selected	High-Z	Active
L	L	H	Read	$D_{OUT}$	Active
L	X	L	Write	$D_{IN}$	Active

#### Notes:

(1) X = don't care.

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
Input voltage, low (Note 1)	$V_{IL}$	-0.3		0.8	V
Input voltage, high	$V_{IH}$	2.2		$V_{CC} + 0.5$	V
Ambient temperature	$T_A$	0		70	°C

#### Notes:

(1) -3.0 V minimum (pulse width = 50 ns).

**AC Characteristics (for L and LL Versions)**

$T_A = 0 \text{ to } +70^\circ\text{C}$ ;  $V_{CC} = +5.0 \text{ V} \pm 10\%$

$V_A = 0 \text{ to } +7.0 \text{ V}$ , $V_{CC} = +3.0 \text{ V} \pm 10\%$											
Parameter	Symbol	$\mu\text{PD43256A-85}$		$\mu\text{PD43256A-10}$		$\mu\text{PD43256A-12}$		$\mu\text{PD43256A-15}$		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
<b>Read Operation</b>											
Read cycle time	$t_{RC}$	85		100		120		150		ns	
Address access time	$t_{AA}$		85		100		120		150	ns	(Note 2)
Chip select access time	$t_{ACS}$		85		100		120		150	ns	(Note 2)
Output enable to output valid	$t_{OE}$		40		50		60		70	ns	(Note 2)
Output hold from address change	$t_{OH}$	10		10		10		10		ns	
Chip select to output in low-Z	$t_{CLZ}$	10		10		10		10		ns	(Note 3)
Output enable to output in low-Z	$t_{OLZ}$	5		5		5		5		ns	(Note 3)
Chip select to output in high-Z	$t_{CHZ}$		30		35		40		50	ns	(Note 3)
Output enable to output in high-Z	$t_{OHZ}$		30		35		40		50	ns	(Note 3)
<b>Write Operation</b>											
Write cycle time	$t_{WC}$	85		100		120		150		ns	
Chip select to end of write	$t_{CW}$	70		80		85		100		ns	
Address valid to end of write	$t_{AW}$	70		80		85		100		ns	
Address setup time	$t_{AS}$	0		0		0		0		ns	
Write pulse width	$t_{WP}$	65		70		70		90		ns	
Write recovery time	$t_{WR}$	5		5		5		5		ns	
Data valid to end of write	$t_{DW}$	35		40		50		60		ns	
Data hold time	$t_{DH}$	0		0		0		0		ns	
Write enable to output in high-Z	$t_{WHZ}$		30		35		40		50	ns	(Note 3)
Output active from end of write	$t_{OW}$	10		10		10		10		ns	(Note 3)

**Notes:**

- (1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.
- (2) See figure 1 for output load.
- (3) See figure 2 for output load.

### Low $V_{CC}$ Data Retention Characteristics

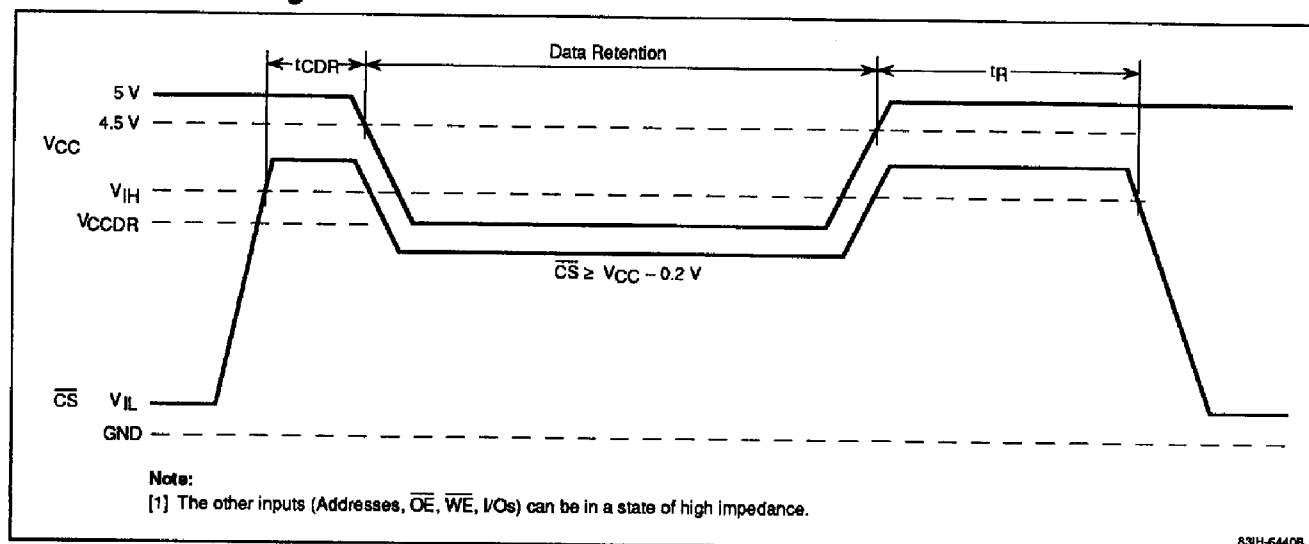
$T_A = 0$  to  $70^\circ\text{C}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	$V_{CCDR}$	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2\text{ V}$
Data retention supply current	$I_{CCDR}$		1	50	$\mu\text{A}$	$V_{CC} = 3.0\text{ V}$ ; $\overline{CS} \geq V_{CC} - 0.2\text{ V}$ (Notes 1, 2)
Chip deselection to data retention	$t_{CDR}$	0			ns	
Operation recovery time	$t_R$	$t_{RC}$			ns	

#### Notes:

- (1) For  $\mu\text{PD43256A-LL}$ ,  $I_{CCDR} = 20\text{ }\mu\text{A}$  (max) at  $T_A = 0$  to  $70^\circ\text{C}$  and  $3\text{ }\mu\text{A}$  (max) at  $T_A = 0$  to  $40^\circ\text{C}$ .
- (2) For  $\mu\text{PD43256A-L}$ ,  $I_{CCDR} = 15\text{ }\mu\text{A}$  (max) at  $T_A = 0$  to  $40^\circ\text{C}$ .

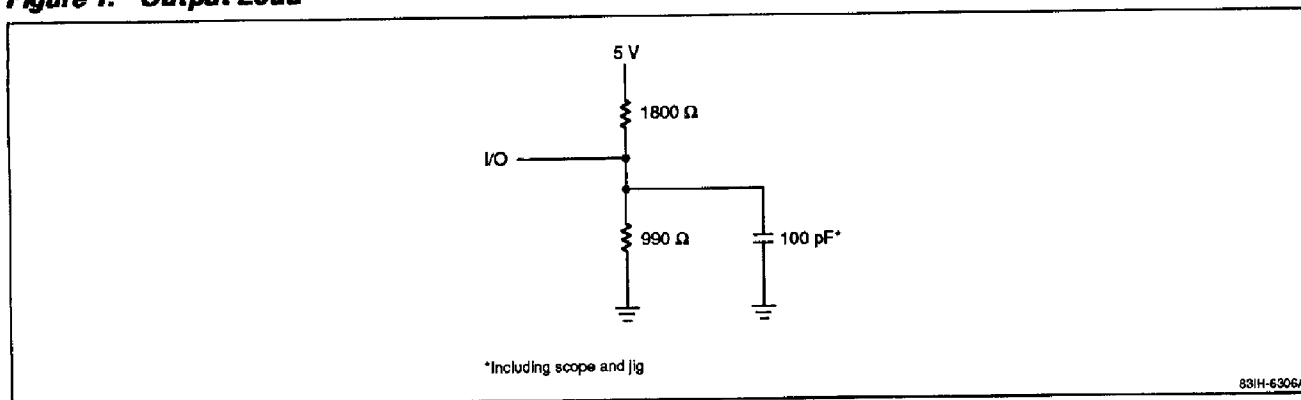
### Data Retention Timing



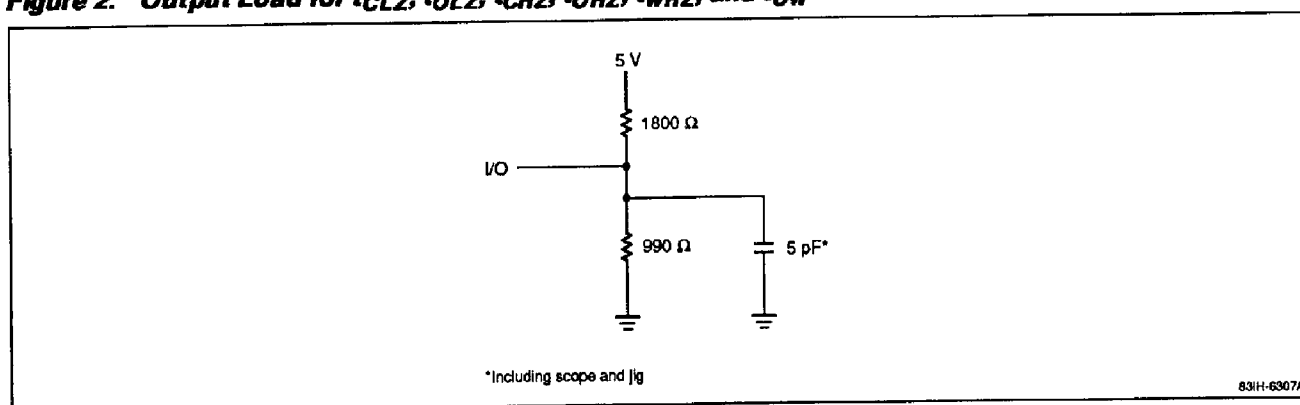
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**$\mu$ PD43256A**

**Figure 1. Output Load**

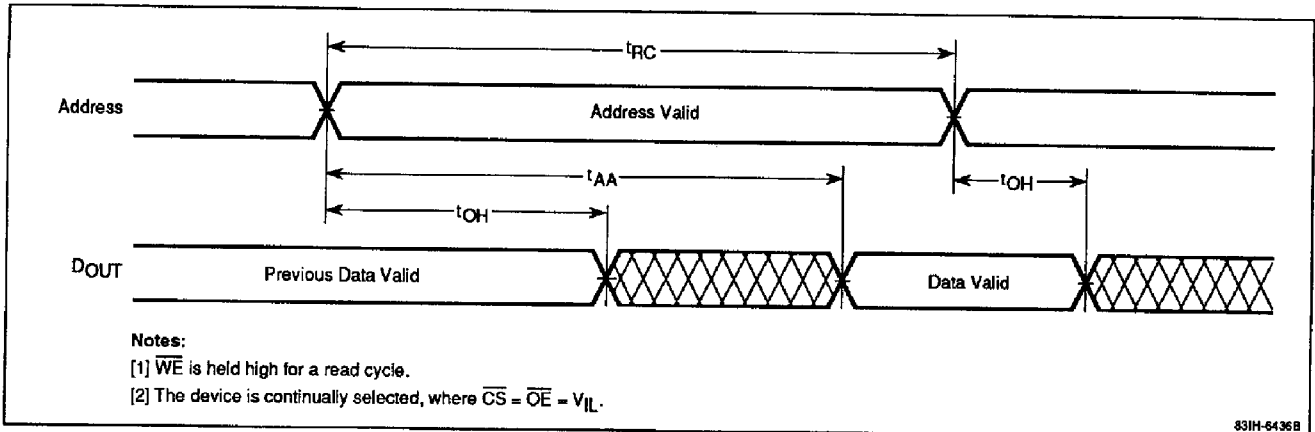


**Figure 2. Output Load for  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$ , and  $t_{OW}$**

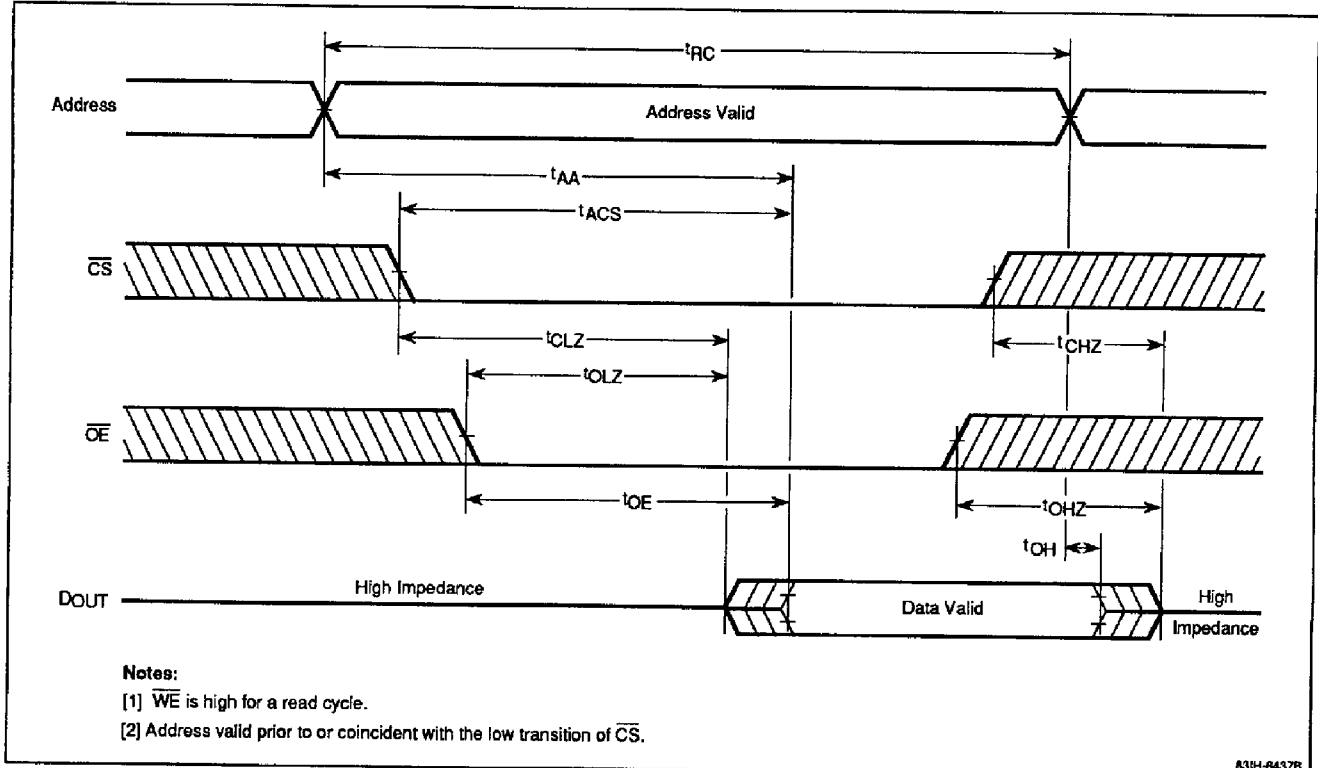


## Timing Waveforms

### Address Access Cycle



### Chip Select Access Cycle





**Timing Waveforms (cont)**

***WE-Controlled Write Cycle***

