

# 4Byte 4Mx36 SIMM

(4Mx4 & 16M Quad  $\overline{\text{CAS}}$  base)

Revision 0.1

Nov. 1997

**Revision History**

**Version 0.1 (Nov. 1997)**

- Changed the mode of parity check component from EDO to FP, refer to *PACKAGE DIMENSIONS* and *GENERAL DISCRPTION*.

**DRAM MODULE**

**KMM5364003CK/CKG & KMM5364103CK/CKG with Fast Page Mode**  
 4M x 36 DRAM SIMM using 4Mx4 and 16M Quad CAS, 4K/2K Refresh, 5V

**GENERAL DESCRIPTION**

The Samsung KMM53640(1)03CK is a 4Mx36bits Dynamic RAM high density memory module. The Samsung KMM53640(1)03CK consists of eight CMOS 4Mx4bits DRAMs in 24-pin SOJ package and one CMOS 4Mx4 bit Quad CAS DRAM in 28-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM53640(1)03CK is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

**PERFORMANCE RANGE**

| Speed | t <sub>TRAC</sub> | t <sub>CAC</sub> | t <sub>RC</sub> |
|-------|-------------------|------------------|-----------------|
| -5    | 50ns              | 13ns             | 90ns            |
| -6    | 60ns              | 15ns             | 110ns           |

**FEATURES**

- Part Identification
  - KMM5364003CK(4096 cycles/64ms Ref, SOJ, Solder)
  - KMM5364003CKG(4096 cycles/64ms Ref, SOJ, Gold)
  - KMM5364103CK(2048 cycles/32ms Ref, SOJ, Solder)
  - KMM5364103CKG(2048 cycles/32ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- PCB : Height(1000mil), single sided component

**PIN CONFIGURATIONS**

| Pin | Symbol                          | Pin | Symbol                          |
|-----|---------------------------------|-----|---------------------------------|
| 1   | V <sub>ss</sub>                 | 37  | DQ17                            |
| 2   | DQ0                             | 38  | DQ35                            |
| 3   | DQ18                            | 39  | V <sub>ss</sub>                 |
| 4   | DQ1                             | 40  | $\overline{\text{CAS0}}$        |
| 5   | DQ19                            | 41  | $\overline{\text{CAS2}}$        |
| 6   | DQ2                             | 42  | $\overline{\text{CAS3}}$        |
| 7   | DQ20                            | 43  | $\overline{\text{CAS1}}$        |
| 8   | DQ3                             | 44  | $\overline{\text{RAS0}}$        |
| 9   | DQ21                            | 45  | Res( $\overline{\text{RAS1}}$ ) |
| 10  | V <sub>cc</sub>                 | 46  | NC                              |
| 11  | NC                              | 47  | W                               |
| 12  | A0                              | 48  | NC                              |
| 13  | A1                              | 49  | DQ9                             |
| 14  | A2                              | 50  | DQ27                            |
| 15  | A3                              | 51  | DQ10                            |
| 16  | A4                              | 52  | DQ28                            |
| 17  | A5                              | 53  | DQ11                            |
| 18  | A6                              | 54  | DQ29                            |
| 19  | A10                             | 55  | DQ12                            |
| 20  | DQ4                             | 56  | DQ30                            |
| 21  | DQ22                            | 57  | DQ13                            |
| 22  | DQ5                             | 58  | DQ31                            |
| 23  | DQ23                            | 59  | V <sub>cc</sub>                 |
| 24  | DQ6                             | 60  | DQ32                            |
| 25  | DQ24                            | 61  | DQ14                            |
| 26  | DQ7                             | 62  | DQ33                            |
| 27  | DQ25                            | 63  | DQ15                            |
| 28  | A7                              | 64  | DQ34                            |
| 29  | A11                             | 65  | DQ16                            |
| 30  | V <sub>cc</sub>                 | 66  | NC                              |
| 31  | A8                              | 67  | PD1                             |
| 32  | A9                              | 68  | PD2                             |
| 33  | Res( $\overline{\text{RAS1}}$ ) | 69  | PD3                             |
| 34  | $\overline{\text{RAS0}}$        | 70  | PD4                             |
| 35  | DQ26                            | 71  | NC                              |
| 36  | DQ8                             | 72  | V <sub>ss</sub>                 |

**PIN NAMES**

| Pin Name  | Function               |
|---|------------------------|
| A0 - A11  | Address Inputs(4K Ref) |
| A0 - A10  | Address Inputs(2K Ref) |
| DQ0 - DQ35  | Data In/Out            |
| $\overline{\text{W}}$                               | Read/Write Enable      |
| $\overline{\text{RAS0}}$                            | Row Address Strobe     |
| $\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$ | Column Address Strobe  |
| PD1 -PD4  | Presence Detect        |
| V <sub>cc</sub>                                     | Power(+5V)             |
| V <sub>ss</sub>                                     | Ground                 |
| NC  | No Connection          |

**PRESENCE DETECT PINS (Optional)**

| Pin | 50NS            | 60NS            |
|-----|-----------------|-----------------|
| PD1 | V <sub>ss</sub> | V <sub>ss</sub> |
| PD2 | NC              | NC              |
| PD3 | V <sub>ss</sub> | NC              |
| PD4 | V <sub>ss</sub> | NC              |

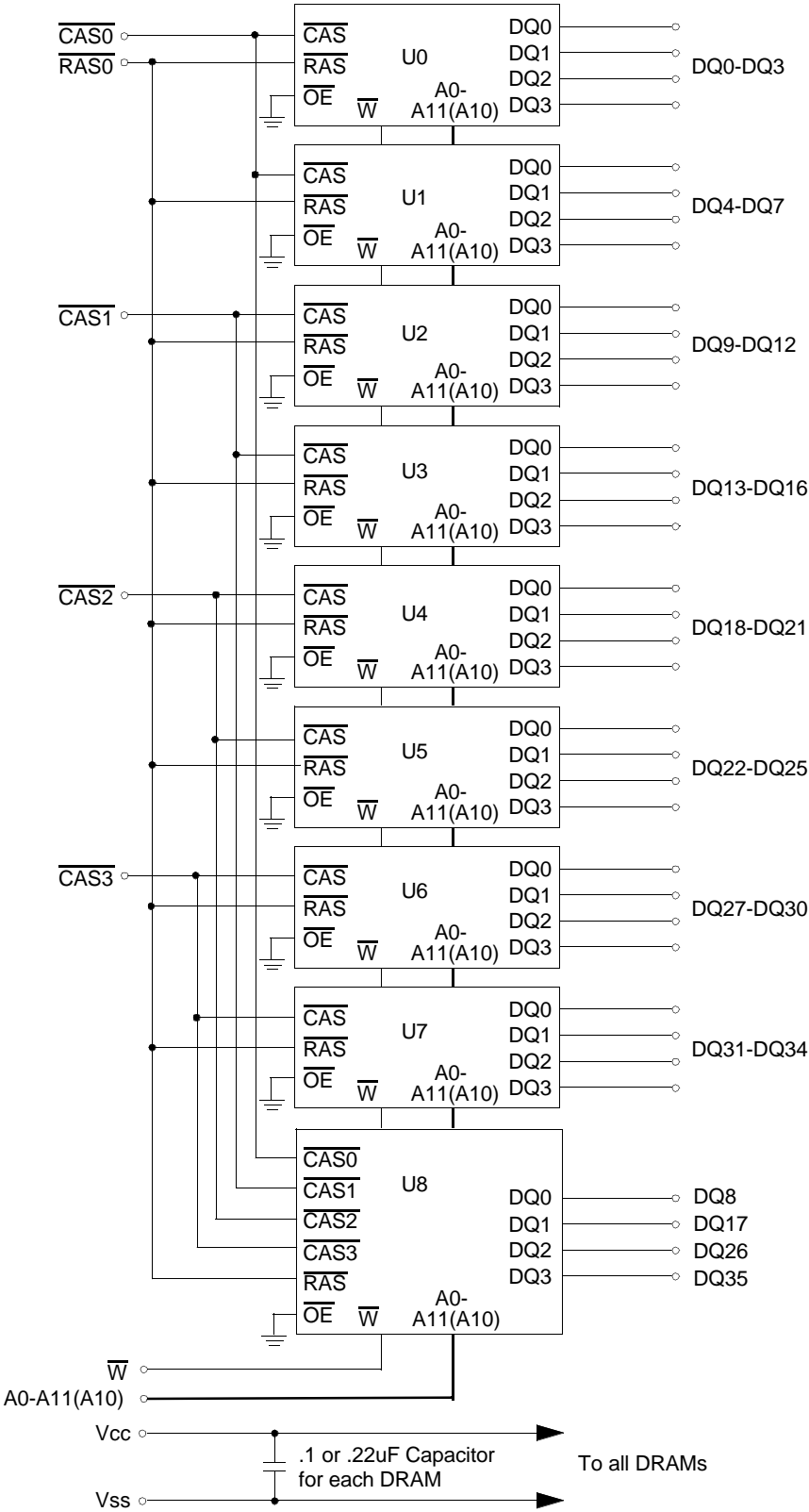
\* Pin connection changing available

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\* NOTE : A11 is used for only KMM5364003CK/CKG (4K ref.)

**DRAM MODULE**

**FUNCTIONAL BLOCK DIAGRAM**



**DRAM MODULE**

**ABSOLUTE MAXIMUM RATINGS \***

| Item  | Symbol                             | Rating      | Unit |
|---|------------------------------------|-------------|------|
| Voltage on any pin relative to V <sub>SS</sub>                | V <sub>IN</sub> , V <sub>OUT</sub> | -1 to +7.0  | V    |
| Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub> | V <sub>CC</sub>                    | -1 to +7.0  | V    |
| Storage Temperature   | T <sub>stg</sub>                   | -55 to +150 | °C   |
| Power Dissipation   | P <sub>d</sub>                     | 9           | W    |
| Short Circuit Output Current                                  | I <sub>OS</sub>                    | 50          | mA   |

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to V<sub>SS</sub>, T<sub>A</sub> = 0 to 70°C)

| Item               | Symbol          | Min                | Typ | Max                              | Unit |
|--------------------|-----------------|--------------------|-----|----------------------------------|------|
| Supply Voltage     | V <sub>CC</sub> | 4.5                | 5.0 | 5.5                              | V    |
| Ground             | V <sub>SS</sub> | 0                  | 0   | 0                                | V    |
| Input High Voltage | V <sub>IH</sub> | 2.4                | -   | V <sub>CC</sub> +1 <sup>*1</sup> | V    |
| Input Low Voltage  | V <sub>IL</sub> | -1.0 <sup>*2</sup> | -   | 0.8                              | V    |

\*1 : V<sub>CC</sub>+2.0V/20ns, Pulse width is measured at V<sub>CC</sub>.

\*2 : -2.0V/20ns, Pulse width is measured at V<sub>SS</sub>.

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted)

| Symbol            | Speed      | KMM5364003CK/CKG |     | KMM5364103CK/CKG |     | Unit |
|-------------------|------------|------------------|-----|------------------|-----|------|
|                   |            | Min              | Max | Min              | Max |      |
| I <sub>CC1</sub>  | -5         | -                | 810 | -                | 990 | mA   |
|                   | -6         | -                | 720 | -                | 900 | mA   |
| I <sub>CC2</sub>  | Don't care | -                | 18  | -                | 18  | mA   |
| I <sub>CC3</sub>  | -5         | -                | 810 | -                | 990 | mA   |
|                   | -6         | -                | 720 | -                | 900 | mA   |
| I <sub>CC4</sub>  | -5         | -                | 720 | -                | 810 | mA   |
|                   | -6         | -                | 630 | -                | 720 | mA   |
| I <sub>CC5</sub>  | Don't care | -                | 9   | -                | 9   | mA   |
| I <sub>CC6</sub>  | -5         | -                | 810 | -                | 990 | mA   |
|                   | -6         | -                | 720 | -                | 900 | mA   |
| I <sub>I(L)</sub> | Don't care | -45              | 45  | -45              | 45  | uA   |
| I <sub>O(L)</sub> | Don't care | -5               | 5   | -5               | 5   | uA   |
| V <sub>OH</sub>   | Don't care | 2.4              | -   | 2.4              | -   | V    |
| V <sub>OL</sub>   | Don't care | -                | 0.4 | -                | 0.4 | V    |

I<sub>CC1</sub> : Operating Current \* (  $\overline{RAS}$ ,  $\overline{CAS}$ , Address cycling @ t<sub>RC</sub>=min)

I<sub>CC2</sub> : Standby Current (  $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub> :  $\overline{RAS}$  Only Refresh Current \* (  $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$  cycling @ t<sub>RC</sub>=min)

I<sub>CC4</sub> : Fast Page Mode Current \* (  $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$  Address cycling : t<sub>PC</sub>=min)

I<sub>CC5</sub> : Standby Current (  $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub> :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current \* (  $\overline{RAS}$  and  $\overline{CAS}$  cycling @ t<sub>RC</sub>=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input 0 ≤ V<sub>IN</sub> ≤ V<sub>CC</sub>+0.5V, all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled, 0V ≤ V<sub>OUT</sub> ≤ V<sub>CC</sub>)

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one page mode cycle, t<sub>PC</sub>.

**DRAM MODULE**

**CAPACITANCE** (TA = 25°C, VCC=5V, f = 1MHz)

| Item   | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Input capacitance[A0-A11(A10)]                             | CIN1   | -   | 65  | pF   |
| Input capacitance[ $\overline{W}$ ]                        | CIN2   | -   | 80  | pF   |
| Input capacitance[ $\overline{RAS0}$ ]                     | CIN3   | -   | 80  | pF   |
| Input capacitance[ $\overline{CAS0}$ - $\overline{CAS3}$ ] | CIN4   | -   | 40  | pF   |
| Input/Output capacitance[DQ0-35]                           | CDQ    | -   | 25  | pF   |

**AC CHARACTERISTICS** (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, Output loading CL=100pF

| Parameter  | Symbol | -5  |     | -6  |     | Unit | Note  |
|--|--------|-----|-----|-----|-----|------|-------|
|  |        | Min | Max | Min | Max |      |       |
| Random read or write cycle time  | tRC    | 90  |     | 110 |     | ns   |       |
| Access time from $\overline{RAS}$  | tRAC   |     | 50  |     | 60  | ns   | 3,4   |
| Access time from $\overline{CAS}$  | tCAC   |     | 13  |     | 15  | ns   | 3,4,5 |
| Access time from column address  | tAA    |     | 25  |     | 30  | ns   | 3,10  |
| $\overline{CAS}$ to output in Low-Z  | tCLZ   | 0   |     | 0   |     | ns   | 3     |
| Output buffer turn-off delay   | tOFF   | 0   | 13  | 0   | 15  | ns   | 6     |
| Transition time(rise and fall)   | tT     | 3   | 50  | 3   | 50  | ns   | 2     |
| $\overline{RAS}$ precharge time  | tRP    | 30  |     | 40  |     | ns   |       |
| $\overline{RAS}$ pulse width   | tRAS   | 50  | 10K | 60  | 10K | ns   |       |
| $\overline{RAS}$ hold time   | tRSH   | 13  |     | 15  |     | ns   |       |
| $\overline{CAS}$ hold time   | tCSH   | 50  |     | 60  |     | ns   |       |
| $\overline{CAS}$ pulse width   | tCAS   | 13  | 10K | 15  | 10K | ns   |       |
| $\overline{RAS}$ to $\overline{CAS}$ delay time                                  | tRCD   | 20  | 37  | 20  | 45  | ns   | 4     |
| $\overline{RAS}$ to column address delay time                                    | tRAD   | 15  | 25  | 15  | 30  | ns   | 10    |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time                              | tCRP   | 5   |     | 5   |     | ns   |       |
| Row address set-up time  | tASR   | 0   |     | 0   |     | ns   |       |
| Row address hold time  | tRAH   | 10  |     | 10  |     | ns   |       |
| Column address set-up time   | tASC   | 0   |     | 0   |     | ns   |       |
| Column address hold time   | tCAH   | 10  |     | 10  |     | ns   |       |
| Column address to $\overline{RAS}$ lead time                                     | tRAL   | 25  |     | 30  |     | ns   |       |
| Read command set-up time   | tRCS   | 0   |     | 0   |     | ns   |       |
| Read command hold time referenced to $\overline{CAS}$                            | tRCH   | 0   |     | 0   |     | ns   | 8     |
| Read command hold time referenced to $\overline{RAS}$                            | tRRH   | 0   |     | 0   |     | ns   | 8     |
| Write command hold time  | tWCH   | 10  |     | 10  |     | ns   |       |
| Write command pulse width  | tWP    | 10  |     | 10  |     | ns   |       |
| Write command to $\overline{RAS}$ lead time                                      | tRWL   | 13  |     | 15  |     | ns   |       |
| Write command to $\overline{CAS}$ lead time                                      | tCWL   | 13  |     | 15  |     | ns   |       |
| Data-in set-up time  | tDS    | 0   |     | 0   |     | ns   | 9     |
| Data-in hold time  | tDH    | 10  |     | 15  |     | ns   | 9     |
| Refresh period (4K Ref)  | tREF   |     | 64  |     | 64  | ms   |       |
| Refresh period (2K Ref)  | tREF   |     | 32  |     | 32  | ms   |       |
| Write command set-up time  | tWCS   | 0   |     | 0   |     | ns   | 7     |
| $\overline{CAS}$ setup time( $\overline{CAS}$ -before- $\overline{RAS}$ refresh) | tCSR   | 5   |     | 5   |     | ns   |       |
| $\overline{CAS}$ hold time( $\overline{CAS}$ -before- $\overline{RAS}$ refresh)  | tCHR   | 10  |     | 10  |     | ns   |       |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time                         | tRPC   | 5   |     | 5   |     | ns   |       |



**DRAM MODULE**

**AC CHARACTERISTICS** (0°C≤T<sub>A</sub>≤70°C, V<sub>CC</sub>=5.0V±10%. See notes 1,2.)

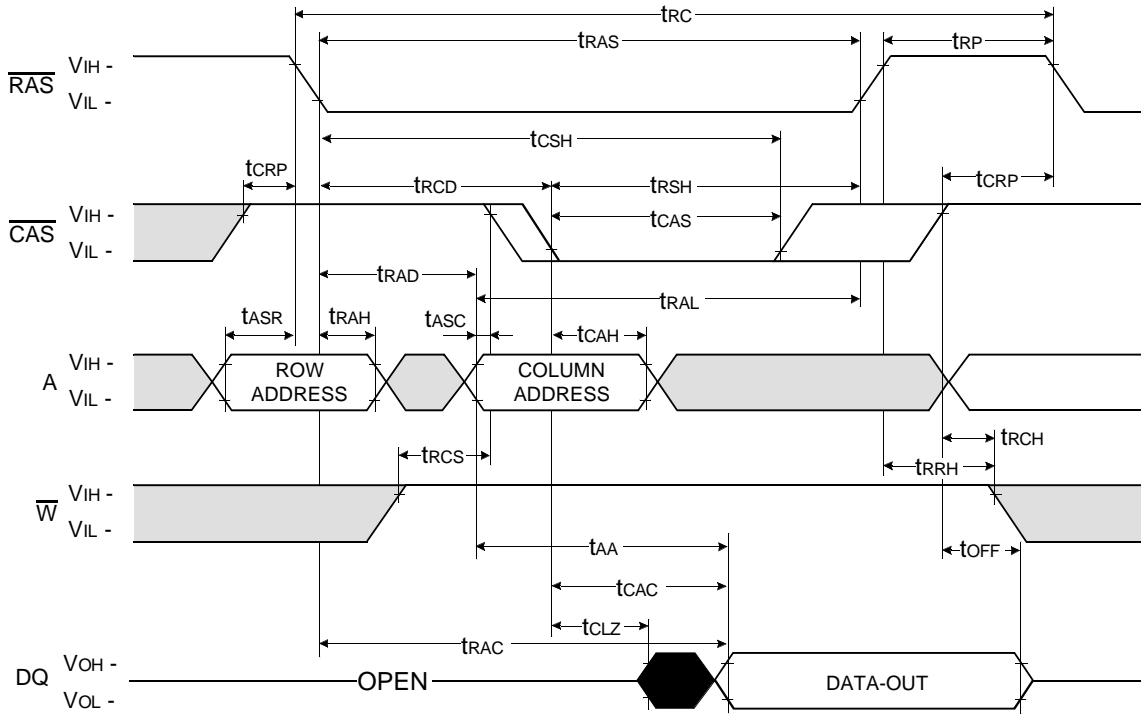
Test condition : V<sub>IH</sub>/V<sub>IL</sub>=2.4/0.8V, V<sub>OH</sub>/V<sub>OL</sub>=2.4/0.4V, Output loading CL=100pF

| Parameter  | Symbol | -5  |      | -6  |      | Unit | Note |
|--|--------|-----|------|-----|------|------|------|
|  |        | Min | Max  | Min | Max  |      |      |
| Access time from $\overline{\text{CAS}}$ precharge                             | tCPA   |     | 30   |     | 35   | ns   | 3    |
| Fast page mode cycle time  | tPC    | 35  |      | 40  |      | ns   |      |
| $\overline{\text{CAS}}$ precharge time(Fast page cycle)                        | tCP    | 10  |      | 10  |      | ns   |      |
| $\overline{\text{RAS}}$ pulse width(Fast page cycle)                           | tRASP  | 50  | 200K | 60  | 200K | ns   |      |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time(C-B-R refresh) | tWRP   | 10  |      | 10  |      | ns   |      |
| $\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time(C-B-R refresh)      | tWRH   | 10  |      | 10  |      | ns   |      |
| Hold time $\overline{\text{CAS}}$ low to $\overline{\text{CAS}}$ high          | tCLCH  | 5   |      | 5   |      | ns   | 11   |

**NOTES**

- An initial pause of 200us is required after power-up followed by any 8  $\overline{\text{RAS}}$ -only or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles before proper device operation is achieved.
- V<sub>IH</sub>(min) and V<sub>IL</sub>(max) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub>(min) and V<sub>IL</sub>(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t<sub>RC</sub>D(max) limit insures that t<sub>RA</sub>C(max) can be met. t<sub>RC</sub>D(max) is specified as a reference point only. If t<sub>RC</sub>D is greater than the specified t<sub>RC</sub>D(max) limit, then access time is controlled exclusively by t<sub>CA</sub>C.
- Assumes that t<sub>RC</sub>D≥t<sub>RC</sub>D(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
- t<sub>WC</sub>S is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t<sub>WC</sub>S≥t<sub>WC</sub>S(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t<sub>RC</sub>H or t<sub>RR</sub>H must be satisfied for a read cycle.
- These parameter are referenced to the  $\overline{\text{CAS}}$  leading edge in early write cycles.
- Operation within the t<sub>RA</sub>D(max) limit insures that t<sub>RA</sub>C(max) can be met. t<sub>RA</sub>D(max) is specified as reference point only. If t<sub>RA</sub>D is greater than the specified t<sub>RA</sub>D(max) limit, then access time is controlled by t<sub>AA</sub>.
- In order to hold the address latched by the first  $\overline{\text{CAS}}$  going low, the parameter t<sub>CL</sub>CH must be met.

**READ CYCLE**

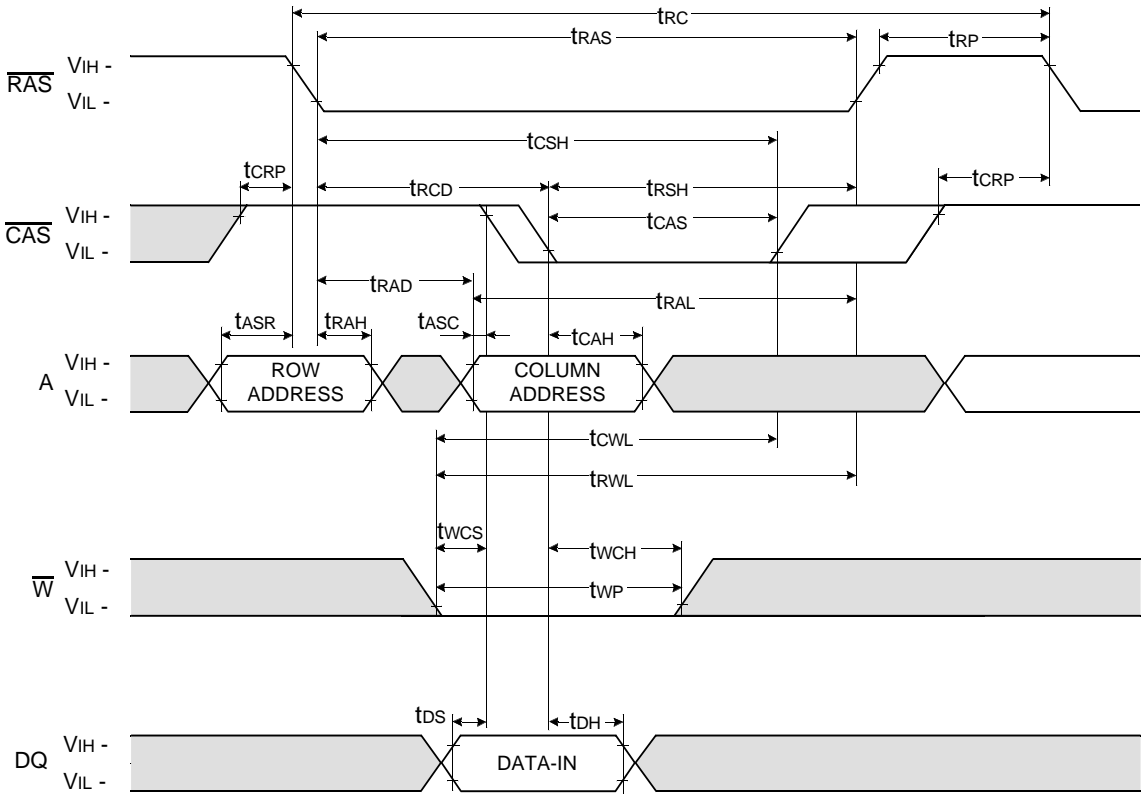




DRAM MODULE

WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

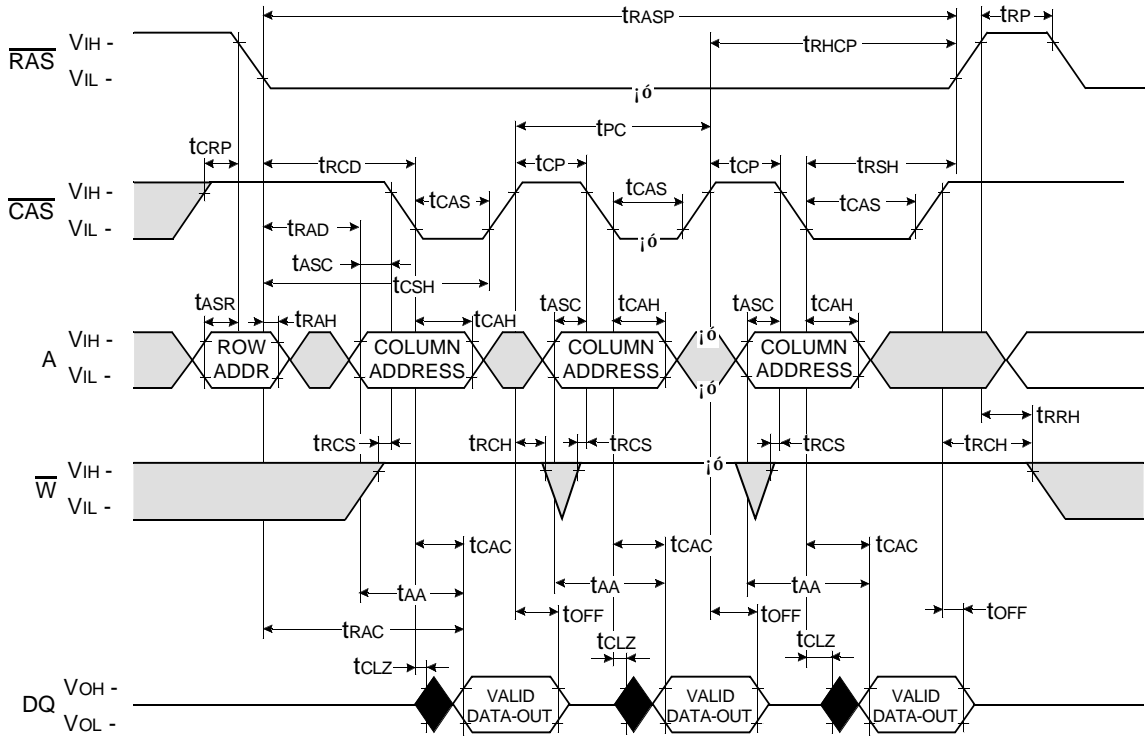


□ Don't care  
■ Undefined

DRAM MODULE

FAST PAGE READ CYCLE

NOTE : DOUT = OPEN

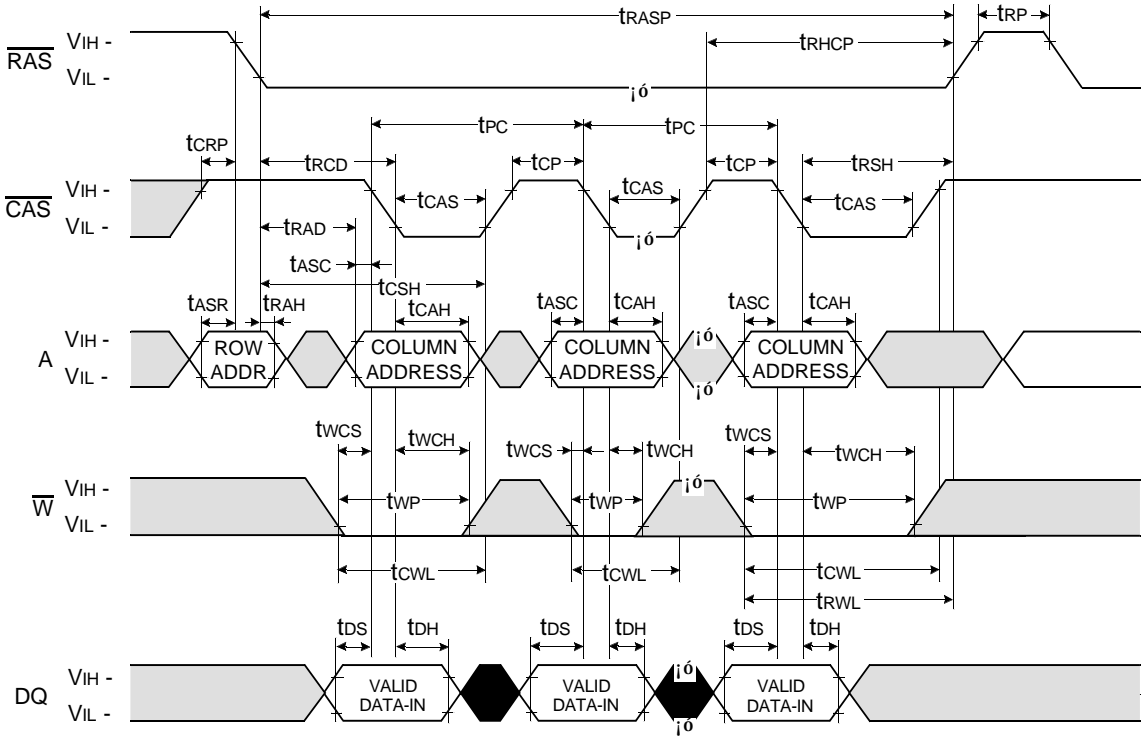


Don't care  
Undefined

DRAM MODULE

FAST PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN

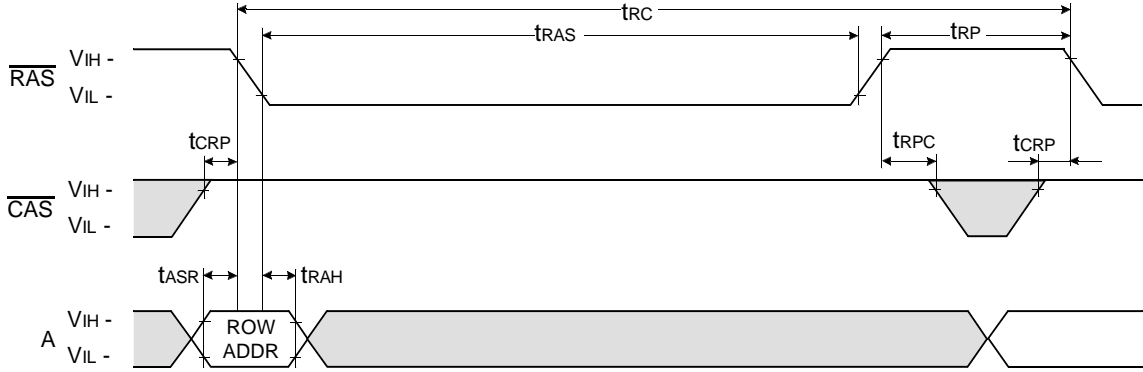


**DRAM MODULE**

**$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE**

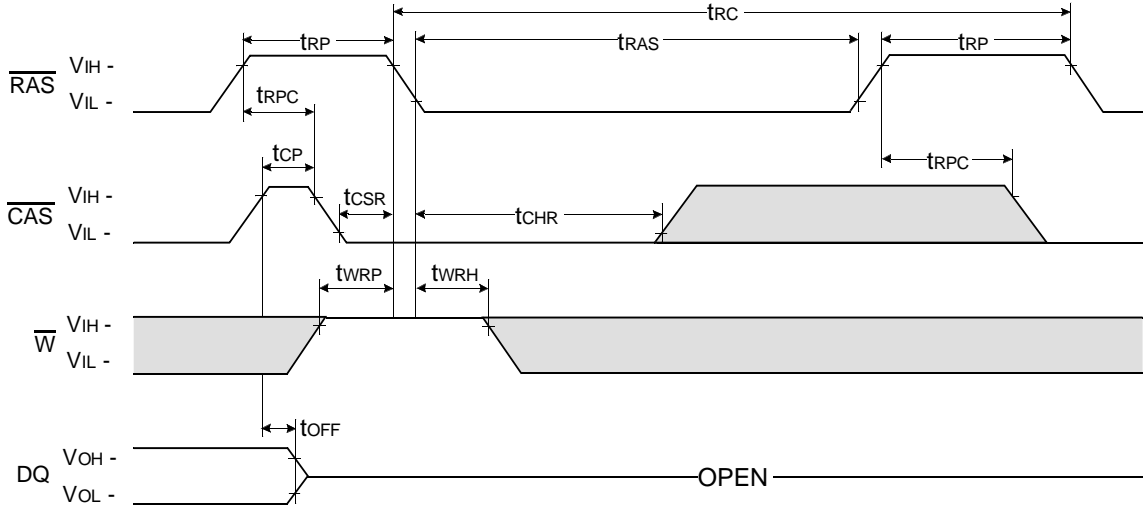
NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ , DIN = Don't care

DOUT = OPEN



**$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**

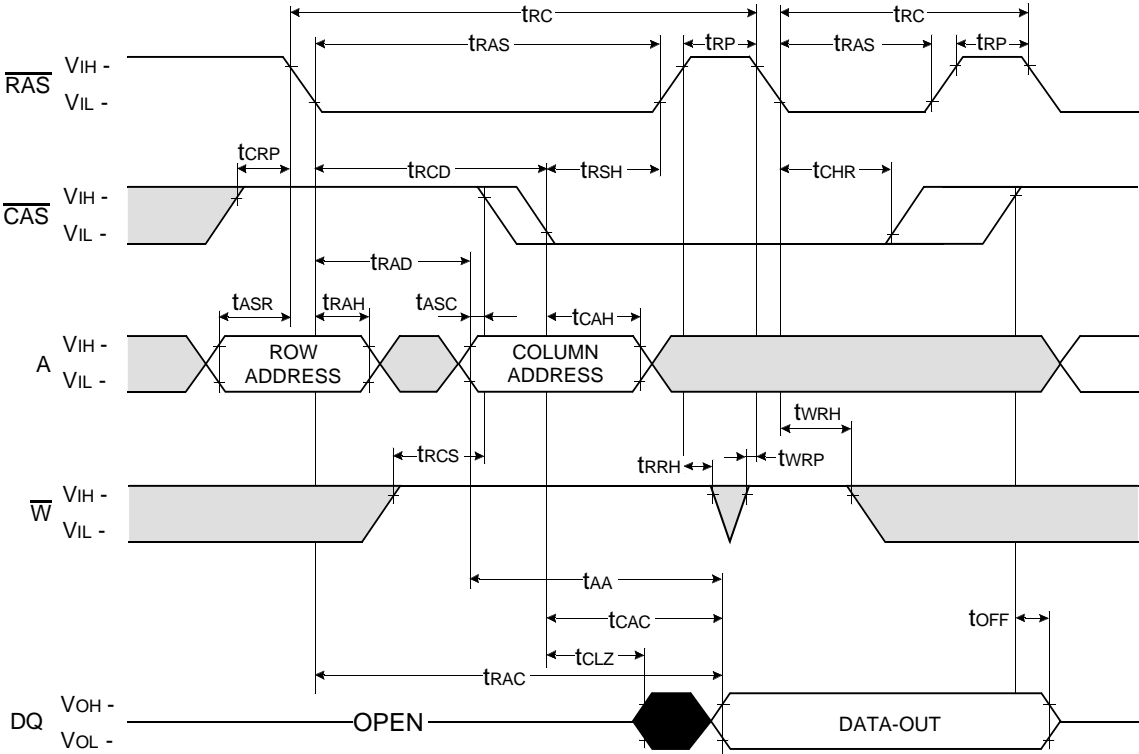
NOTE :  $\overline{\text{OE}}$ , A = Don't care



□ Don't care  
■ Undefined

DRAM MODULE

HIDDEN REFRESH CYCLE ( READ )

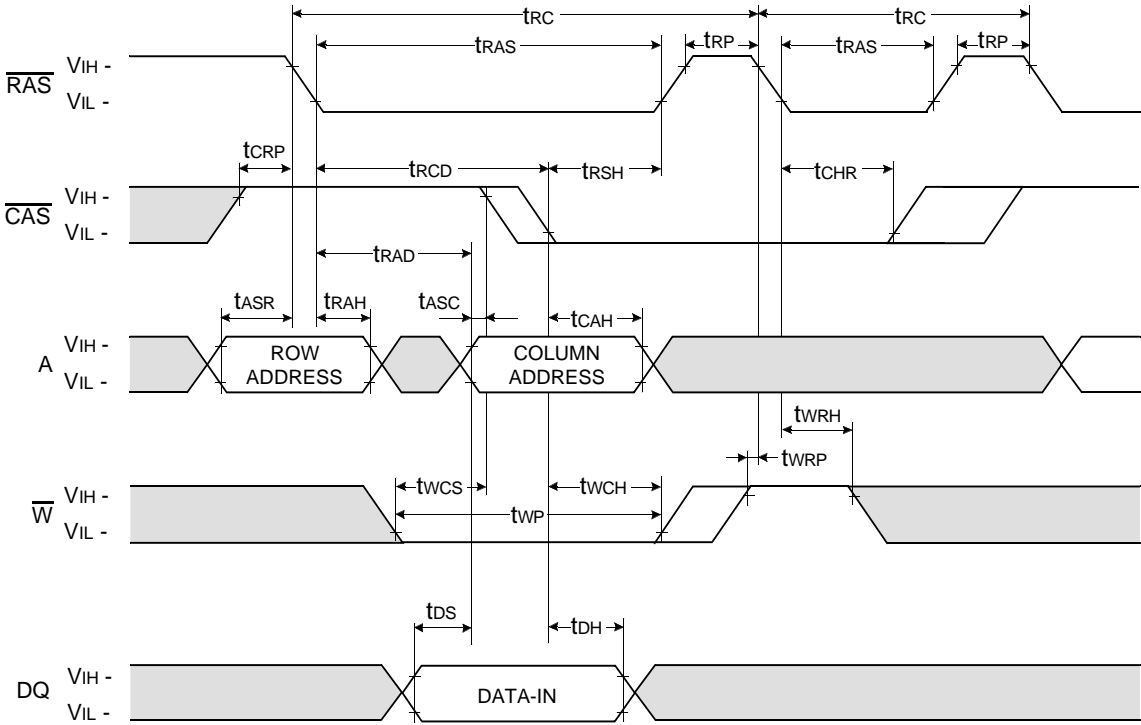


Don't care  
 Undefined

DRAM MODULE

HIDDEN REFRESH CYCLE ( WRITE )

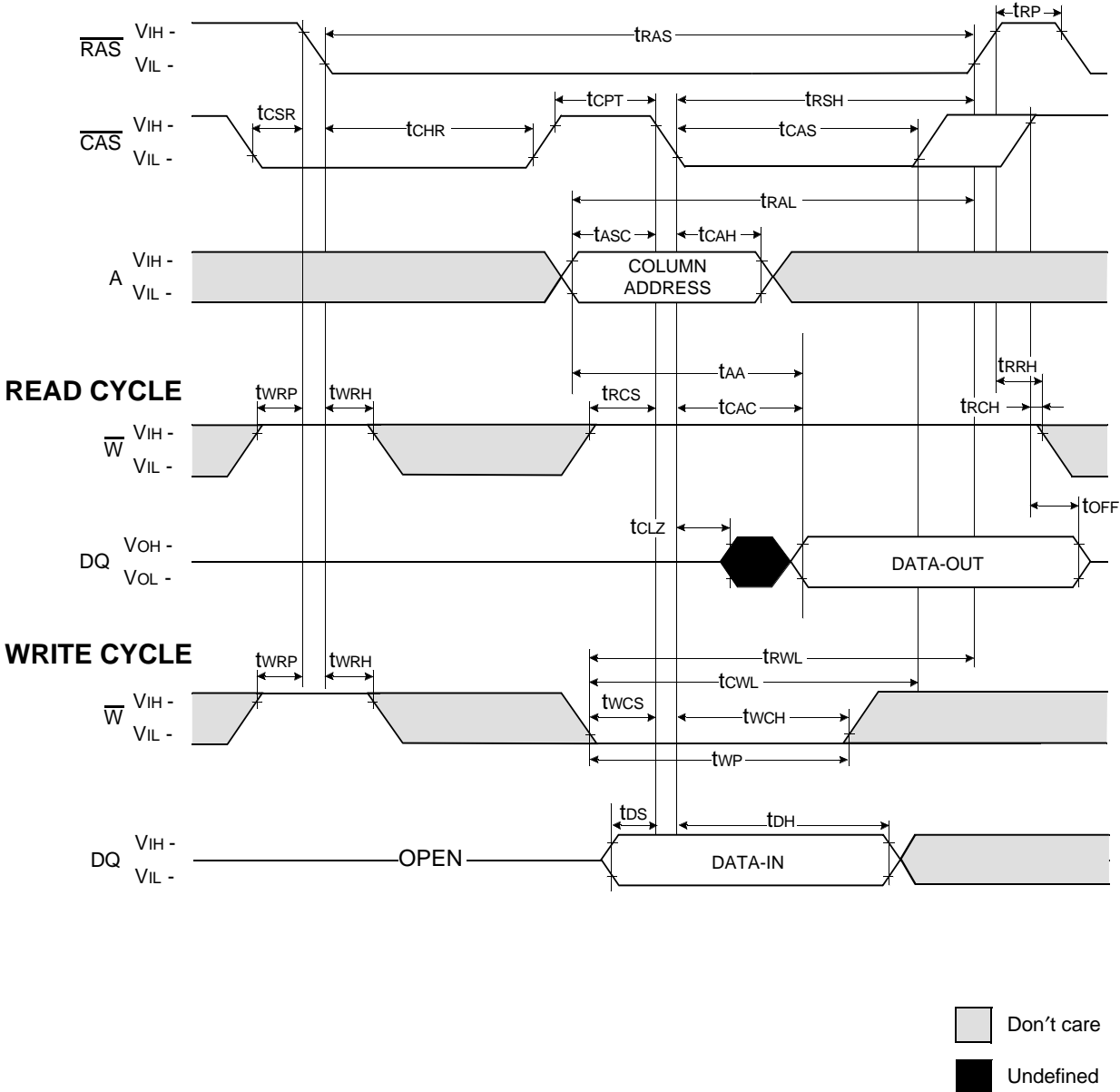
NOTE : DOUT = OPEN



□ Don't care  
■ Undefined

DRAM MODULE

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

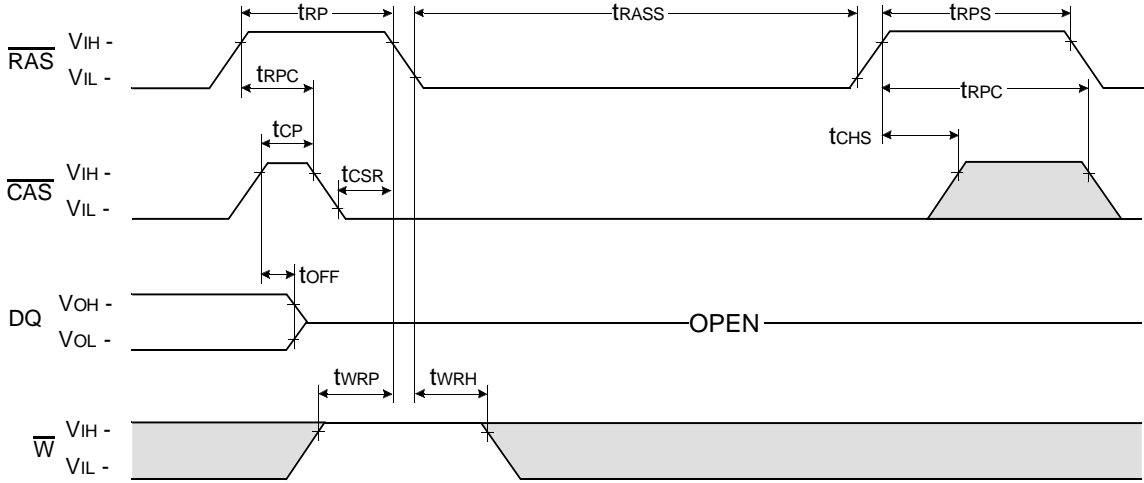


NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

DRAM MODULE

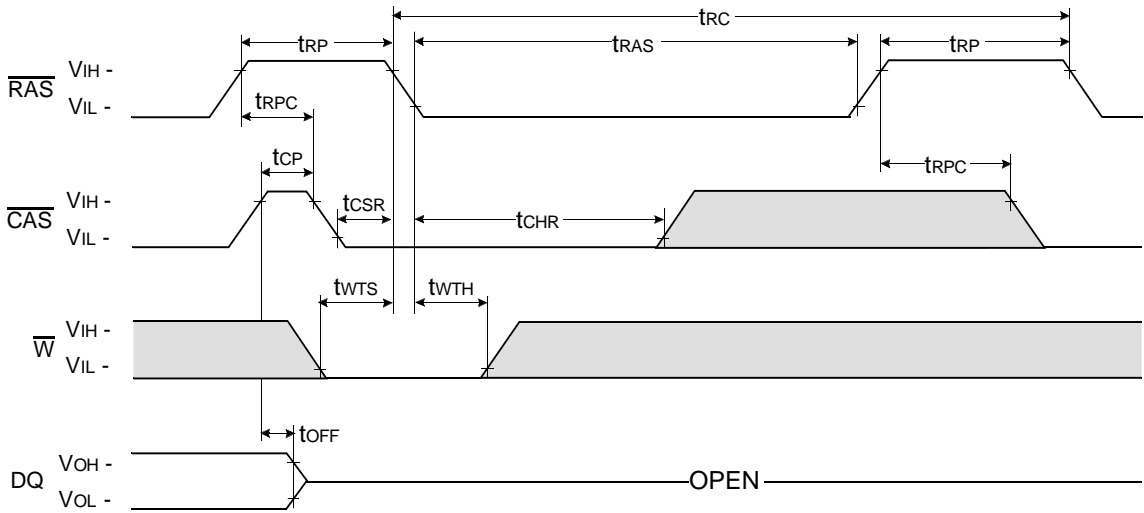
**CAS - BEFORE - RAS SELF REFRESH CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



**TEST MODE IN CYCLE**

NOTE :  $\overline{OE}$ , A = Don't care



□ Don't care  
■ Undefined

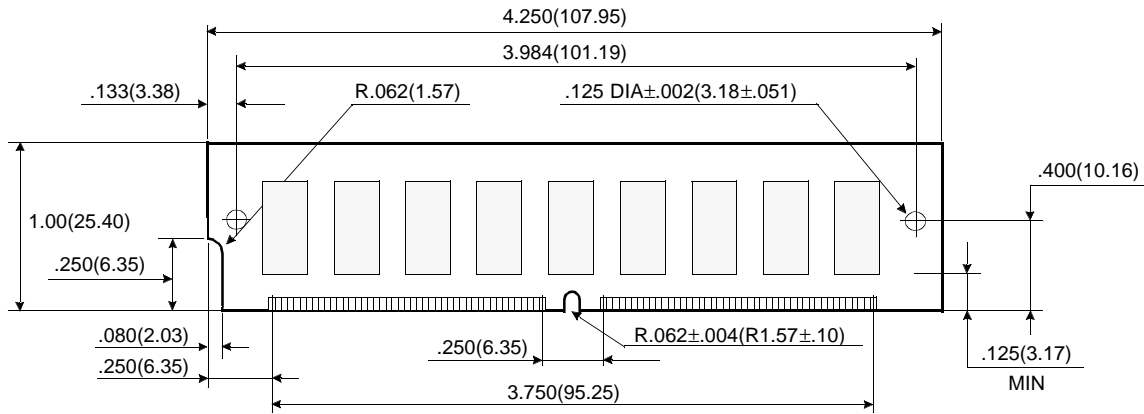


# DRAM MODULE

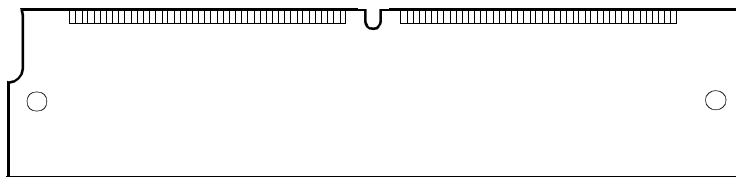
**KMM5364003CK/CKG**  
**KMM5364103CK/CKG**

## PACKAGE DIMENSIONS

Units : Inches (millimeters)

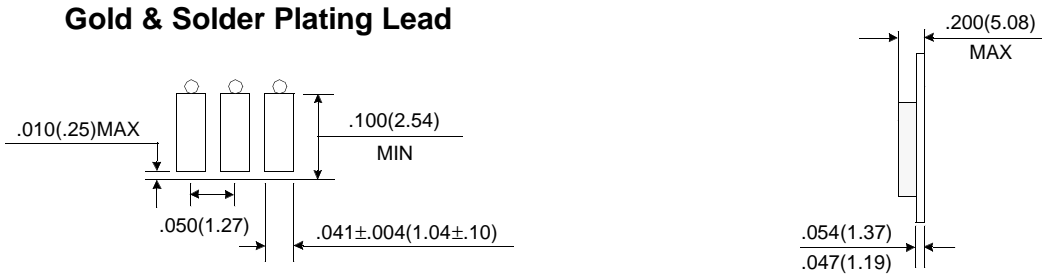


( Front view )



( Back view )

### Gold & Solder Plating Lead



Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device are 4Mx4 FP DRAM (SOJ & 300mil) & 4Mx4 Quad CAS with FP DRAM (SOJ & 300mil)

DRAM Part No. : KMM5364003CK/CKG -- KM44C4000CK (300 mil) & KM44C4003CK (300mil)  
 KMM5364103CK/CKG -- KM44C4100CK (300 mil) & KM44C4103CK (300mil)

Revision History  
 Rev 0.1 : Nov. 1997