1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

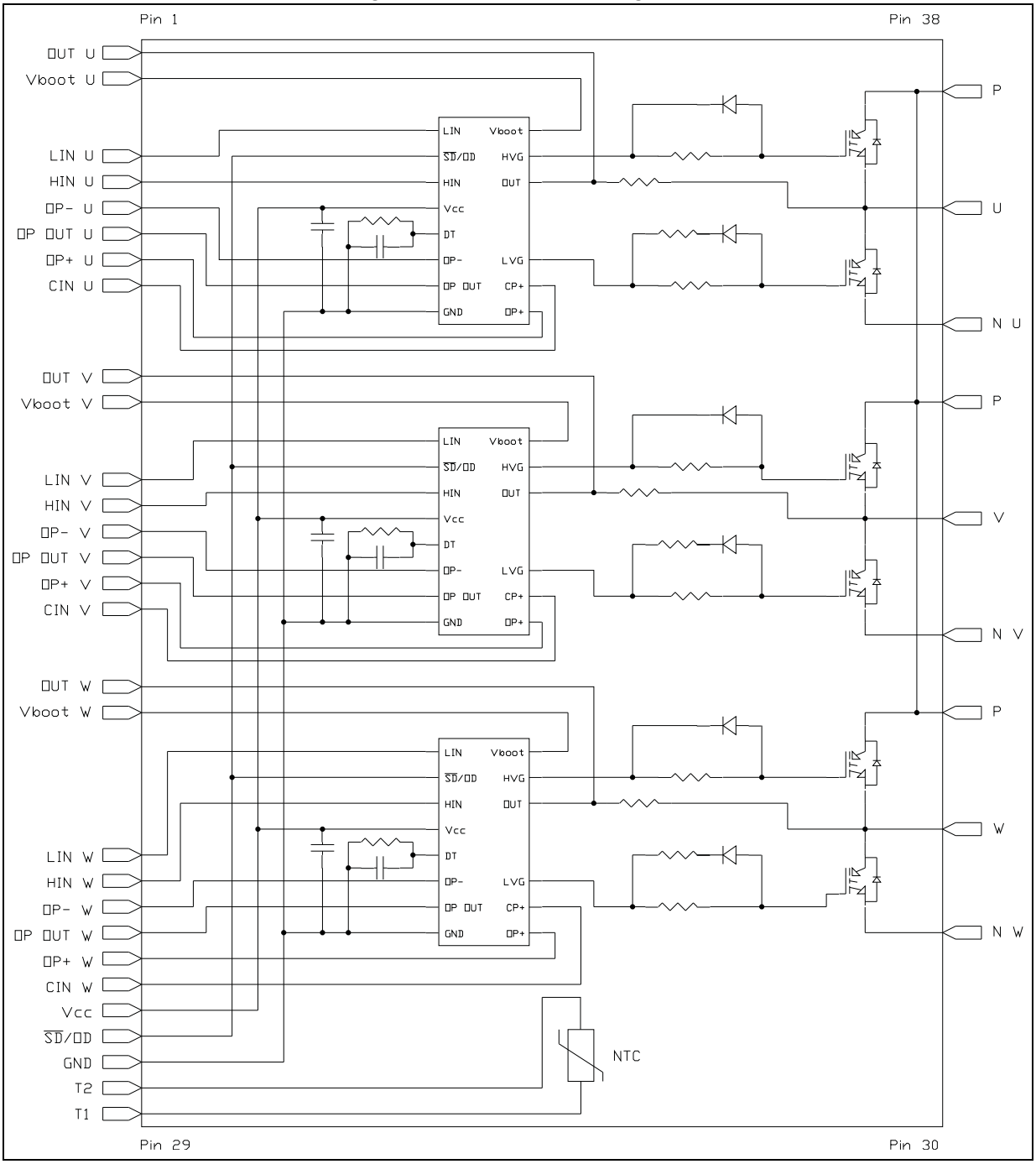

Table 2. Pin description

Pin	Symbol	Description
1	OUT_U	High side reference output for U phase
2	$V_{boot\ U}$	Bootstrap voltage for U phase
3	LIN_U	Low side logic input for U phase
4	HIN_U	High side logic input for U phase
5	$OP\text{-}_U$	Op amp inverting input for U phase
6	$OP_{OUT\ U}$	Op amp output for U phase
7	$OP+_U$	Op amp non inverting input for U phase
8	CIN_U	Comparator input for U phase
9	OUT_V	High side reference output for V phase
10	$V_{boot\ V}$	Bootstrap voltage for V phase
11	LIN_V	Low side logic input for V phase
12	HIN_V	High side logic input for V phase
13	$OP\text{-}_V$	Op amp inverting input for V phase
14	$OP_{OUT\ V}$	Op amp output for V phase
15	$OP+_V$	Op amp non inverting input for V phase
16	CIN_V	Comparator input for V phase
17	OUT_W	High side reference output for W phase
18	$V_{boot\ W}$	Bootstrap voltage for W phase
19	LIN_W	Low side logic input for W phase
20	HIN_W	High side logic input for W phase
21	$OP\text{-}_W$	Op amp inverting input for W phase
22	$OP_{OUT\ W}$	Op amp output for W phase
23	$OP+_W$	Op amp non inverting input for W phase
24	CIN_W	Comparator input for W phase
25	V_{CC}	Low voltage power supply
26	$\overline{SD}$ / OD	Shut down logic input (active low) / open drain (comparator output)
27	GND	Ground
28	T_2	NTC thermistor terminal 2
29	T_1	NTC thermistor terminal 1
30	N_W	Negative DC input for W phase
31	W	W phase output
32	P	Positive DC input
33	N_V	Negative DC input for V phase
34	V	V phase output