65540 / 545

High Performance
Flat Panel / CRT
VGA Controllers

Data Sheet
Revision 1.2

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CHIPS®

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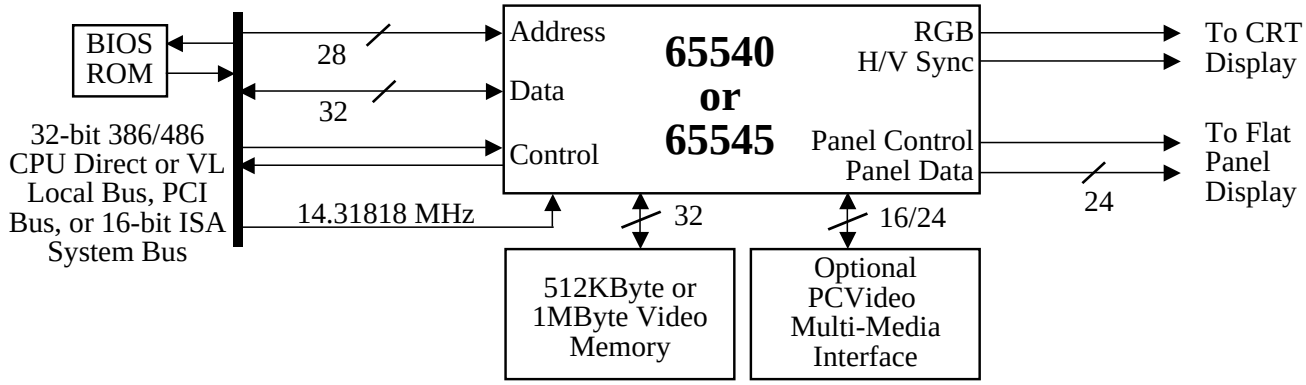
65540 / 545
High Performance
Flat Panel / CRT VGA Controller

- Highly integrated design (flat panel / CRT VGA controller, RAMDAC, clock synthesizer)
- Multiple Bus Architecture Integrated Interface
  - Local Bus (32-bit CPU Direct and VL)
  - EISA/ISA (PC/AT) 16-bit Bus
  - PCI Bus (65545)
- Flexible display memory configurations
  - One 256Kx16 DRAM (512KB)
  - Four 256Kx4 DRAMs (512KB)
  - Two 256Kx16 DRAMs (1MB)
- Advanced frame buffer architecture uses available display memory, maximizing integration and minimizing chip count
- Integrated programmable linear address feature accelerates GUI performance
- Hardware windows acceleration (65545)
  - 32-bit graphics engine
    - System-to-screen and screen-to-screen BitBLT
    - 3 operand ROP's
    - Color expansion
    - Optimized for Windows™ BitBLT format
  - Hardware line drawing
  - 64x64x2 hardware cursor
- Hardware pop-up icon (65545)
  - 64x64 pixels by 4 colors
  - 128x128 pixels by 2 colors
- High performance resulting from zero wait-state writes (write buffer) and minimum wait-state reads (internal asynchronous FIFO design)
- Mixed 3.3V ±0.3V / 5.0V ±10% Operation
- Interface to CHIPS' PC Video to display "live" video on flat panel displays
- Supports panel resolutions up to 1280 x 1024 resolution including 800x600 and 1024x768
- Supports non-interlaced CRT monitors with resolutions up to 1024 x 768 / 256 colors
- True-color and Hi-color display capability with flat panels and CRT monitors up to 640x480 resolution
- Direct interface to Color and Monochrome Dual Drive (DD) and Single Drive (SS) panels (supports 8, 9, 12, 15, 16, 18 and 24-bit data interfaces)
- Advanced power management features minimize power consumption during:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- Flexible on-board Activity Timer facilitates ordered shut-down of the display system
- Power Sequencing control outputs regulate application of Bias voltage, +5V to the panel and +12 V to the inverter for backlight operation
- SMARTMAP™ intelligent color to gray scale conversion enhances text legibility
- Text enhancement feature improves white text contrast on flat panel displays
- Fully Compatible with IBM™ VGA
- EIAJ-standard 208-pin plastic flat pack



System Diagram

Revision History

Revision	Date	By	Comment
1.1	9/94	DH	Added note: Refer to Electrical Specs for maximum clock frequencies in 'Supported Video Modes' table Added note: Not all above resolutions can be supported at 3.3V and/or 5V Changed Mode 50 in Supported Video Modes-Extended Resolution Table from 16 to 16M Reset column in Reset/Setup/Test/Standby/Panel-Off Mode table was incorrect. Now reads: "RESET#/Low/–/–/High/High" Changed note for Pin List-Bus Interface: from "Drive=5V low drive and 3V high drive" to "IOL and IOH drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)" Changed pin description: pin 25 LDEV# pin type "Out/OC" to "Out" Changed Config Reg XR01 bits 2-1 VL-Bus description for pin 23=CRESET should read pin 23=RDYRTN# Changed Ext Reg XR2D and XR2E to (CMPR Enabled) and (CMPR Disabled) and added note: "For DD panels without frame acceleration, the programmed value should be doubled" Updated tables for "No FRC" and "2-Frame FRC" Updated Flat Panel Timing "CD: 010" should read "CD: 001" Updated Programming: FLM delay programmed in XR2C should be equal to: CRT blank time – FLM front porch – FLM width XR2D LP Delay (CMPR enabled) & XR2E LP Delay (CMPR disabled) Added note: "Can use external 14.31818 MHz oscillator into XTALI (203) with XTALO (204) as no connect" Updated Elec Specs: changed "Max" under "Normal Operating Conditions" from 90 to 100; "memory clock is assumed to be 68 MHz not 65 MHz;" and "VL-Bus timing is compatible with VL-Bus Specification 2.0" Added timing for VL-Bus LDEV#, 14.31818 MHz, DRAM R/M/W and PC-Video and modified timing for PCI Bus Frame Clarified function of ACTI output.
1.2	7/95	BB/MP	Updated Supported Video Modes table Updated I/O Map section Added 64310 to CHIPS VGA Product Family in Register Summary Updated Extension Registers table Updated XR33, XR6C, XR6F in the Extension Registers section Added Rset formula to CRT Panel Interface Circuit Updated Interface-Optrex DMF-50351NC-FW (640x480 Color STN-DD) LCD Panel Interface example Updated 65540/545 DC Characteristics in timing section Updated Local Bus Input Setup & Hold, Local Bus Output Valid, Local Bus Output Float Delay, VL-Bus LDEV#, CRT Output, Panel Output Timing diagrams Added 65545B2 specifications

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Introduction / Overview

The 65540 / 545 High Performance Flat Panel / CRT Controllers initiate a family of 208-pin, high performance solutions for full-featured notebook / sub-notebook and other portable applications that require the highest graphics performance available. The 65545 is pin-to-pin compatible with the 65540 and adds a sophisticated graphics hardware engine for Bit Block Transfer (BitBLT), line drawing, hardware cursor, and other functions intensively used in Graphical User Interfaces (GUIs) such as Microsoft Windows™. The 65540 and 65545 also use the same video BIOS, offering the system manufacturer a wide range of price / performance points while minimizing overhead for system integration and improving time-to-market. The following table indicates feature differences between the 65540 and 65545:

Features	65540	65545
Support for all flat panels	✓	✓
VESA Local Bus / 16-bit ISA Bus	✓	✓
32-bit PCI Bus	—	✓
Linear Addressing	✓	✓
Hardware Accelerator	—	✓
Hardware Cursor	—	✓
Pin Compatible	✓	✓
BIOS Compatible	✓	✓

The 65540 / 545 family achieves superior performance through direct connection to system processor buses up to 32-bits in width. When combined with CHIPS' advanced linear acceleration software driver technology, these devices exhibit exceptional performance compared with devices of similar architecture. The 65540 / 545 architecture provides a fast throughput to video memory, maximizing the capability of today's powerful microprocessors to manipulate graphics operations. Based on the architecture of the 65540, the 65545 adds a powerful 32-bit graphics engine to offload graphics processing from the microprocessor for maximum performance.

Minimum chip-count, low-power graphics subsystem implementations are enabled through the high integration level of the 65540 / 545 family. These devices integrate the VGA-compatible graphics controller, true color RAMDAC, and dual PLL clock synthesizers. The entire graphics sub-system can be implemented with a single 256Kx16 DRAM. The 32-bit local bus interface of the 65540 / 545 family eliminates external buffers.

For maximum performance, the 65540 / 545 supports an additional 256Kx16 DRAM, which provides a 32-bit video memory bus and additional display memory to support resolutions up to 1024x768 with 256 colors, 800x600 with 256 colors, and 640x480 with 16M colors. In addition, the 65540 / 545 family can support PC Video multi-media features while interfacing to a 32-bit local bus and one MByte of video memory.

The 65540 / 545 family supports a wide variety of monochrome and color Single-Panel, Single-Drive (SS) and Dual-Panel, Dual Drive (DD) passive STN and active matrix TFT / MIM LCD, EL, and plasma panels. The 65540 / 545 family supports panel resolutions of 800x600, 1024x768, and 1280x1024. For monochrome panels, up to 64 gray scales are supported. Up to 226,981 different colors can be displayed on passive STN LCDs and up to 16M colors on 24-bit active matrix LCDs using the 65540 / 545 controllers.

The 65540 / 545 family offers a variety of programmable features to optimize display quality. For text modes which do not fill all 480 lines of a standard VGA panel, the 65540 / 545 provides tall font stretching in the hardware. Fast vertical centering and programmable vertical stretching in graphics modes offer more options for handling modes with less than 480 lines. Three selectable color-to-grayscale reduction techniques and SMARTMAP™ are available for improving the viewability of color applications on monochrome panels. CHIPS' polynomial FRC algorithm reduces panel flicker on a wider range of panel types with a single setting for a particular panel type.

The 65540 / 545 employs a variety of advanced power management features to reduce power consumption of the display subsystem and extend battery life. The 65540 / 545's internal logic, memory interface, bus interface, and flat panel interfaces can be independently configured to operate at either 3.3 V or 5.0 V. The 65540 / 545 is optimized for minimum power consumption during normal operation and provides two power-saving modes - Panel Off and Standby. During Panel Off mode, the 65540 / 545 turns off the flat panel while

the VGA subsystem remains active. The palette may also be automatically shut off during Panel Off mode to further reduce power consumption. During Standby mode, the 65540 / 545 suspends all CPU, memory and display activities. In this mode, the 65540 / 545 places the DRAM in self-refresh mode and the 65540 / 545 reference input clock can be turned off. The 65540 / 545 also provides a programmable activity timer which monitors VGA activity. After all display activity ceases, the timer will automatically shut down the panel by either disabling the backlight or putting the 65540 / 545 in Panel Off mode.

The 65540 / 545 is fully compatible with the VGA graphics standard at the register, gate, and BIOS levels. The 65540 / 545 provides full backwards compatibility with the EGA and CGA graphics standards without using NMIs. CHIPS and third-party vendors supply fully VGA-compatible BIOS, end-user utilities and drivers for common application programs (e.g., Microsoft Windows™, OS/2, WordPerfect, Lotus, etc.). CHIPS' drivers for Windows include a Big Cursor (to increase the cursor's legibility on monochrome flat panels) and panning / scrolling capability (to increase performance).

MINIMUM CHIP COUNT / BOARD SPACE

The 65540 / 545 provides a minimum chip count / board space, yet highly flexible VGA subsystem. The 65540 / 545 integrates a high-performance VGA flat panel / CRT controller, industry-standard RAMDAC, clock synthesizer, monitor sense circuitry and an activity timer in a 208-pin plastic flat pack package. In its minimum configuration, the 65540 / 545 requires only a single 256Kx16 DRAM, such that a complete VGA subsystem for motherboard applications can be implemented with just two ICs. This configuration consumes less than 2 square inches (1290 sq mm) of board space and is capable of supporting simultaneous flat panel / CRT display requirements while directly interfacing to a 32-bit local bus. As an option, a second memory chip may be implemented to increase performance (via a 32-bit data path to display memory) and support graphics modes which require more than 512 KBytes of display memory. No external buffers or glue logic are required for the 65540 / 545's bus interface, memory interface, or panel interface. The 65540 / 545 employs separate address and data buses with sufficient drive capability such that the bus can be driven directly. The 65540 / 545 also provides up to 24 bits of panel data with sufficient drive capability such that virtually all flat panels can be driven directly.

DISPLAY MEMORY INTERFACE

The 65540 / 545 supports multiple display memory configurations, providing the OEM with the flexibility to use the same VGA controller in several designs with differing cost, power consumption and performance criteria. The 65540 / 545 supports the following display memory configurations:

- One 256Kx16 DRAM (512 KBytes)
- Two 256Kx16 DRAMs (1 MBytes)
- Four 256Kx4 DRAMs (512 KBytes)

Performance is significantly improved when the 65540 / 545 is configured with a 32-bit data path to display memory, which is accomplished by using two 256Kx16 DRAMs. Two 256Kx16 DRAMs support all standard, Super, and Extended VGA resolutions up to 1024x768 256 colors as well as "high" 16bpp color and "true" 24bpp color modes. The table on the following page summarizes the display capabilities of the 65540 / 545.

Display memory control signals are derived from the integrated clock synthesizer's memory clock. The 65540 / 545 serves as a DRAM controller for the system's display memory. It handles DRAM refresh, fetches data from display memory for display refresh, interfaces the CPU to display memory, and supplies all necessary DRAM control signals.

The 65540 / 545 supports 'two-CAS / one-WE' and 'one-CAS / two-WE' 256Kx16 DRAMs. The 65540 / 545 supports the self-refresh features of 256Kx16 DRAMs and certain 256Kx4 DRAMs during Standby mode, enabling the 65540 / 545 to be powered down completely during suspend/resume operation.

65540 / 545 Display Capabilities

CRT Mode Resolution	CRT Mode Color[4]	Mono LCD Gray Scales [4]	DD STN LCD Colors [2, 3, 4]	9-Bit TFT LCD Colors [1, 2, 3, 4]	Video Memory	Simultaneous Display
320x200	256 / 256K†	61 / 61	256 / 226,981	256 / 185,193	512KB	Yes
640x480	16 / 256K†	16 / 61	16 / 226,981	16 / 185,193	512KB	Yes
640x480	256 / 256K†	61 / 61	256 / 226,981	256 / 185,193	512KB	Yes
800x600	16 / 256K†	16 / 61	16 / 226,981	16 / 185,193	512KB	Yes with 1MB
800x600	256 / 256K†	61 / 61	256 / 226,981	256 / 185,193	512KB	Yes with 1MB
1024x768	16 / 256K†	16 / 61	16 / 226,981	16 / 185,193	512KB	Yes with 1MB
1024x768	256 / 256K†	61 / 61	256 / 226,981	256 / 185,193	1MB	Yes
1280x1024	16 / 256K†	16 / 61	n/a	n/a	1MB	n/a

Notes:

1 Larger color palettes and simultaneous colors can be displayed on 12-bit, 18-bit, and 24-bit TFT panels via the 65540 / 545 video input port

2 Includes dithering

3 Includes frame rate control

4 Colors are described as number of simultaneous on-screen colors and number of unique colors available in the color palette

† 256K colors assumes DAC output mode is set to 6 bits of R, G, & B. If DAC is set to 8-bit output mode, the number of available colors is 16M

CPU BUS INTERFACE

The 65540 / 545 provides a direct interface to:

- 32-bit VL-Bus
- 32-Bit 386/486 CPU local bus
- EISA/ISA (PC/AT) 16-bit bus
- PCI Bus (65545 only)

Strap options allow the user to configure the chip for the type of interface desired. Control signals for all interface types are integrated on chip. All operations necessary to ensure proper functioning in these various environments are handled in a fashion transparent to the CPU. These include internal decoding of all memory and I/O addresses, bus width translations, and generation of necessary control signals.

HIGH PERFORMANCE FEATURES

The 65540 / 545 includes a number of performance enhancement techniques including:

- Direct 32-bit local bus CPU support
- 32-bit interface to video memory
- Linearly addressable display memory
- 32-bit graphics hardware engine (65545 only)
- 64x64x2 hardware cursor (65545 only)

The 65540 /545 provides an optimized 32-bit path from 32-bit CPUs direct to the video memory. Running the 32-bit local bus of the 65540 / 545 at CPU speeds up to 33 MHz maximizes data throughput and drawing speed for today's powerful CPU architectures. Addressing pixels linearly maximizes the efficiency of software drivers, enabling the CPU to make the most use of the full 32-bit path through the 65540 / 545 controller. Software drivers optimized for linear addressing are available from CHIPS and improve performance up to 80% over standard software methods.

65545 ACCELERATION

Several functions traditionally performed by software have been implemented in hardware in the 65545 to off load the CPU and further improve performance. Three-Operand BitBLT logic supports all 256 logical combinations of Source, Destination, and Pattern. All BitBLTs are executed up to 32-bits per cycle, maximizing the efficiency of memory accesses. A 32-bit color expansion engine allows the host CPU to transfer monochrome "maps" of color images over the system bus at high speeds to the 65545, which decodes the monochrome images into their color form. Line drawing is also accelerated with hardware assistance.

65545 HARDWARE CURSOR

A programmable-size hardware cursor frees software from continuously generating the cursor image on the display. The 65545 supports four types of cursors:

32 x 32	x 2bpp	(and/xor)
64 x 64	x 2bpp	(and/xor)
64 x 64	x 2bpp	(4-color)
128 x 128	x 1bpp	(2-color)

The first two hardware cursor types indicated as 'and/xor' above follow the MS Windows™ AND/XOR cursor data plane structure which provides for two colors plus 'transparent' (background color) and 'inverted' (background color inverted). The last two types in the list above are also referred to as 'Pop-Ups' because they are typically used to implement pop-up menu capabilities. Hardware cursor / pop-up data is stored in display memory, allowing multiple cursor values to be stored and selected rapidly. The two or four colors specified by the values in the hardware cursor data arrays are stored in on-chip registers as high-color (5-6-5) values independent of the on-chip color lookup tables.

The hardware cursor can overlay either graphics or video data on a pixel by pixel basis. It may be positioned anywhere within screen resolutions up to 2048x2048 pixels. 64x64 'and/xor' cursors may also be optionally doubled in size to 128 pixels either horizontally and/or vertically by pixel replication.

Hardware cursor screen position, type, color, and base address of the cursor data array in display memory may be controlled via the 32-bit 'DR' extension registers.

PC VIDEO / OVERLAY SUPPORT

The 65540 / 545 allows up to 24 bits of external RGB video data to be input and merged with the internal VGA data stream. The 65540 / 545 supports two forms of video windowing: (i) color key input and (ii) X-Y window keying. The X-Y window key input can be used to position the live video window coordinates. The 65540 / 545 can be used in conjunction with Chips and Technologies, Inc. PC Video products to provide portable multi-media solutions.

DISPLAY INTERFACE

The 65540 / 545 is designed to support a wide range of flat panel and CRT displays of all different types and resolutions.

Flat Panel Displays

The 65540 / 545 supports all flat panel display technologies including plasma, electroluminescent (EL) and liquid crystal displays (LCD). LCD panel interfaces are provided for single panel-single drive (SS) and dual panel-dual drive (DD) configurations. A single panel sequences data similar to a CRT (i.e., sequentially from one area of video memory). In contrast, a dual panel requires video data to be provided alternating from two separate areas of video memory. In addition, a dual drive panel requires the data from the two areas to be provided to the panel simultaneously. Due to its integrated frame buffer and 24-data-line panel interface, the 65540 / 545 supports all panels directly. Support for LCD-DD panels does not require external hardware such as a frame buffer. Support for high-resolution, 'high color' flat panels also does not require additional components. The 65540 / 545 handles display data sequencing transparently to applications software, providing full compatibility on both CRT and flat panel displays.

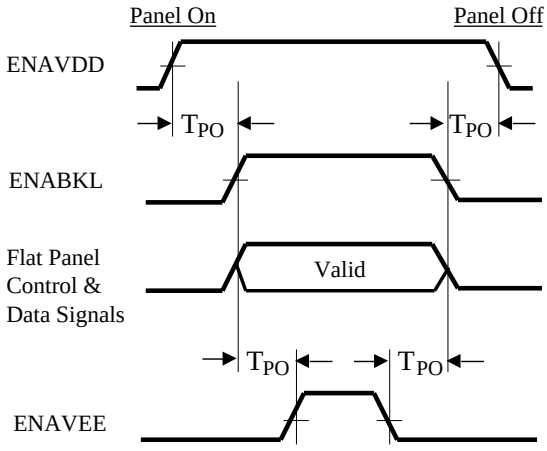
9-bit '512-Color'	12-bit '4096-Color'	Dither	FRC
512 (8^3)	4096 (16^3)	No	No
3,375 (15^3)	29,791 (31^3)	No	Yes
24,389 (29^3)	226,981 (61^3)	Yes	No
185,193 (57^3)	1,771,561 (121^3)	Yes	Yes

There is currently no standard interface for flat panel displays. Interface signals and timing requirements vary between panel technologies and suppliers. The 65540 / 545 provides register programmable features to allow interfacing to the widest possible range of flat panel displays. The 65540 / 545 provides a direct interface to panels from vendors such as Sharp, Sanyo, Epson, Seiko Instruments, Oki, Toshiba, Hitachi, Fujitsu, NEC, Matsushita/Panasonic, and Planar.

PANEL POWER SEQUENCING

Flat panel displays are extremely sensitive to conditions where full biasing voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel. This results in severe damage to the panel and may disable the panel permanently. The 65540 / 545 provides a simple and elegant method to sequence power to the flat panel display during various modes of operation to conserve power and provide safe operation to the flat panel. The 65540 / 545 provides three pins called ENAVEE, ENAVDD and ENABKL to regulate the LCD Bias Voltage (VEE), the driver electronics logic voltage (VDD), and the backlight voltage (BKL) to provide intelligent power sequencing to the panel. The timing diagram below illustrates the power sequencing cycle. In the 65540 / 545, the power on/off delay time (T_{PO}) is programmable (with a default of 32 mS).

The 65540 / 545 initiates a 'panel off' sequence if the STNDBY# input is asserted (low), or if XR52 bit-4 is set to a '1' putting the chip into STNDBY mode. The 65540 / 545 also initiates a 'panel off' sequence if the chip is programmed to enter 'panel off' mode (by setting extension register XR52 bit-3=1), or if the 'Display Type' is programmed to 'CRT' (extension register XR51 bit-2 transitions from '1' to '0'). The 65540 / 545 initiates a 'panel on' sequence if the STNDBY# input is high and the chip is programmed to 'panel on' (XR52 bit-3 transitions from a '1' to '0') and 'flat panel display' (XR51 bit-2 is set to '1').



Panel Power Sequencing

CRT Displays

The 65540 / 545 supports high resolution fixed frequency and variable frequency analog monitors in interlaced and non-interlaced modes of operation. Digital monitor support is also built in.

The 65540 / 545 supports resolutions up to 1024x768 256 colors, 800x600 256 colors or 640x480 16,777,216 colors in 1 MByte display memory configurations, 1024x768 16 colors, 800x600 256 colors in 512 KBytes display memory configurations. The tables starting on the following page list all 65540 / 545 CRT monitor video modes.

Supported Video Modes - VGA Standard

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz) †	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
0, 1	Text	16	40 x 25	8x8	360x400	28.322	31.5	70	256 KB	A,B,C
0*, 1*			40 x 25	8x14	320x350	25.175				
0+, 1+			40 x 25	8x8	320x200	25.175				
2, 3	Text	16	80 x 25	9x16	720x400	28.322	31.5	70	256 KB	A,B,C
2*, 3*			80 x 25	8x14	640x350	25.175				
2+, 3+			80 x 25	8x8	640x200	25.175				
4	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70	256 KB	A,B,C
5	Graphics	4	40 x 25	8x8	320x200	25.175	31.5	70	256 KB	A,B,C
6	Graphics	2	80 x 25	8x8	640x200	25.175	31.5	70	256 KB	A,B,C
7	Text	Mono	80 x 25	9x16	720x400	28.322	31.5	70	256 KB	A,B,C
7+			80 x 25	9x14	720x350					
D	Planar	16	40 x 25	8x8	320x200	25.175	31.5	70	256 KB	A,B,C
E	Planar	16	80 x 25	8x8	640x200	25.175	31.5	70	256 KB	A,B,C
F	Planar	Mono	80 x 25	8x14	640x350	25.175	31.5	70	256 KB	A,B,C
10	Planar	16	80 x 25	8x14	640x350	25.175	31.5	70	256 KB	A,B,C
11	Planar	2	80 x 30	8x16	640x480	25.175	31.5	60	256 KB	A,B,C
12	Planar	16	80 x 30	8x16	640x480	25.175	31.5	60	256 KB	A,B,C
13	Packed Pixel	256	40 x 25	8x8	320x200	25.175	31.5	70	256 KB	A,B,C

Note:
- All of the above VGA standard modes are supported directly in the 65548 BIOS (both 32K and 40K BIOS versions).
- All of the above VGA standard modes are supported at both 3.3V and 5V.
- All VGA modes using 25.175 MHz and 28.322 MHz can also be supported using 32 MHz and 36 MHz respectively. In this case, the horizontal frequency becomes 40.000 KHz and the vertical frequency becomes 89 Hz. (see XR33 bit-7 "ISO Mode Control" for selection of VGA dot clock frequencies)

Note: Not **all** above resolutions can be supported at both 3.3V and 5V.

† Refer to Electrical Specifications section for maximum clock frequencies for 5V and 3.3V operation.

CRT Codes:

A PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 35.5 KHz Horizontal Frequency Specification)

B Multi-Frequency CRT monitor (37.5 KHz Minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)

C Multi-Frequency High-Performance CRT Monitor (48.5 KHz Min H Freq Specification) (Nanao Flexscan 9070s, MultiSync 5D, or equivalent)

Supported Video Modes - Extended Resolution

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz) †	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
20	4 bit Linear	16	80 x 30	8x16	640x480	25.175	31.5	60	512 KB	A,B,C
22	4 bit Linear	16	100 x 37	8x16	800x600	40.000	37.5	60	512 KB	B,C
24	4 bit Linear	16	128 x 48	8x16	1024x768	65.000	48.5	60	512 KB	C
24 I	4 bit Linear	16	128 x 48	8x16	1024x768	44.900	35.5	**43**	512 KB	B,C
28I	4 bit Linear	16	128 x 48	8x16	1280x1024	65.000	42.5	39	1 MB	C
30	8 bit Linear	256	80 x 30	8x16	640x480	25.175	31.5	60	512 KB	A,B,C
32	8 bit Linear	256	100 x 37	8x16	800x600	40.000	37.5	60	512 KB	B,C
34	8 bit Linear	256	128 x 48	8x16	1024x768	65.000	48.5	60	1 MB	C
34 I	8 bit Linear	256	128 x 48	8x16	1024x768	44.900	35.5	**43**	1 MB	B,C
40	15bit Linear	32K	80 x 30	8x16	640x480	50.350	31.5	60	1 MB	A,B,C
41	16bit Linear	64K	80 x 30	8x16	640x480	50.350	31.5	60	1 MB	A,B,C
50	24bit Linear	16M	80 x 30	8x16	640x480	65.000	27.1	51.6	1 MB	B,C
60	Text	16	132 x 25	8x16	1056x400	40.000	30.5	68	256 KB	A,B,C
61	Text	16	132 x 50	8x16	1056x400	40.000	30.5	68	256 KB	A,B,C
6A, 70	Planar	16	100 x 37	8x16	800x600	40.000	38.0	60	256 KB	B,C
72,75	Planar	16	128 x 48	8x16	1024x768	65.000	48.5	60	512 KB	C
72, 75I	Planar	16	128 x 48	8x16	1024x768	44.900	35.5	**43**	512 KB	B,C
78	Packed Pixel	16	80 x 25	8x16	640x400	25.175	31.5	70	256 KB	A,B,C
79	Packed Pixel	256	80 x 30	8x16	640x480	25.175	31.5	60	512 KB	A,B,C
7C	Packed Pixel	256	100 x 37	8x16	800x600	40.000	37.5	60	512 KB	B,C
7E	Packed Pixel	256	128 x 48	8x16	1024x768	65.000	48.5	60	1 MB	C
7E I	Packed Pixel	256	128 x 48	8x16	1024x768	44.900	35.5	**43**	1 MB	B,C
76 I	4 bit Planar	16	128 x 48	8x16	1280x1024	65.000	42.5	39	1 MB	C

Note: Support for the modes in the above table is included directly in the BIOS (both 32K and 40K versions).
The "I" in the mode # column indicates "Interlaced".

Supported Video Modes - High Refresh

Mode# (Hex)	Display Mode	Colors	Text Display	Font Size	Pixel Resolution	DotClock (MHz) †	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Video Memory	CRT
12*	Planar	16	80 x 30	8x16	640x480	31.500	37.5	75	256 KB	B,C
30	8 bit Linear	256	80 x 30	8x16	640x480	31.500	37.5	75	256 KB	C
79	Packed Pixel	256	80 x 30	8x16	640x480	31.500	37.5	75	512 KB	C
6A, 70	Planar	16	100 x 37	8x16	800x600	49.500	46.9	75	512 KB	C
32	8 bit Linear	256	100 x 37	8x16	800x600	49.500	46.9	75	1 MB	C
7C	Packed Pixel	256	100 x 37	8x16	800x600	49.500	46.9	75	1 MB	C

Note: Not **all** above resolutions can be supported at both 3.3V and 5V.

† Refer to Electrical Specifications section for maximum clock frequencies for 5V and 3.3V operation.

CRT Codes:

A PS/2 fixed frequency analog CRT monitor or equivalent (31.5 / 35.5 KHz Horizontal Frequency Specification)

B Multi-Frequency CRT monitor (37.5 KHz Minimum Horizontal Frequency Specification) (NEC MultiSync 3D or equivalent)

C Multi-Frequency High-Performance CRT Monitor (48.5 KHz Min H Freq Specification) (Nanao Flexscan 9070s, MultiSync 5D, or equivalent)

Simultaneous Flat Panel / CRT Display

The 65540 / 545 provides simultaneous display operation with Multi-Sync variable frequency or PS/2 fixed frequency CRT monitors and single panel-single drive LCDs (LCD-SS), dual panel-dual drive LCDs (LCD-DD), and plasma and EL panels (which employ single panel-single drive interfaces). Single drive panels sequence data in the same manner as CRTs, so the 65540 / 545 provides simultaneous CRT display with LCD-SS, Plasma, and EL panels by driving the panels with CRT timing. LCD-DD panels require video data alternating between two separate locations in memory. In addition, a dual drive panel requires data from both locations simultaneously. A framestore area, also called the frame buffer, is required to achieve this operation. The 65540 / 545 innovative architecture implements the frame buffer in an unused area of display memory, reducing chip count and subsystem cost. As an option, an extra 16-bit wide DRAM can be used as an external frame buffer, improving performance while in simultaneous flat panel/CRT modes. The 65540 / 545 provides simultaneous display with monochrome and color LCD-DD panels with a single 256Kx16 DRAM.

DISPLAY ENHANCEMENT FEATURES

Display quality is one of the most important features for the success of any flat panel-based system. The 65540 / 545 provides many features to enhance the flat panel display quality.

"TRUE-GRAY" Gray Scale Algorithm

A proprietary polynomial-based Frame Rate Control (FRC) and dithering algorithm in the 65540 / 545's hardware generates a maximum of 61 gray levels on monochrome panels. The FRC technique simulates a maximum of 16 gray levels on monochrome panels by turning the pixels on and off over several frames in time. The dithering technique increases the number of gray scales from 16 to 61 by altering the pattern of gray scales in adjacent pixels. The persistence (response time) of the pixels varies among panel manufacturers and models. By re-programming the polynomial (an 8-bit value in Extension Register XR6E) while viewing the display, the FRC algorithm can be adjusted to match the persistence of the particular panel without increasing the panel's vertical refresh rate. With this technique, the 65540 / 545 produces up to 61 flicker-free gray scales on the latest fast response "mouse quick" film-compensated monochrome STN LCDs. The alternate method of reducing flicker -- increasing the panel's vertical refresh rate -- has several drawbacks. As the vertical refresh rate increases, panel power consumption increases, ghosting (cross-talk) increases, and contrast decreases. CHIPS' polynomial FRC gray scale algorithm reduces flicker without increasing the vertical refresh rate.

RGB Color To Gray Scale Reduction

The 24 bits of color palette data from the VGA standard color lookup table (CLUT) are reduced to 6 bits for 64 gray scales via one of three selectable RGB color to gray scale reduction techniques:

1) NTSC Weighting: 5/16 Red 9/16 Green 2/16 Blue
2) Equal Weighting: 5/16 Red 6/16 Green 5/16 Blue
3) Green Only: 6 bits of Green only

NTSC is the most common weighting, which is used in television broadcasting. Equal weighting increases the weighting for Blue, which is useful for Applications such as Microsoft Windows 3.1 which often uses Blue for background colors. Green-Only is useful for replicating on a flat panel the display of software optimized for IBM's monochrome monitors which use the six green bits of palette data.

SmartMap™

SmartMap™ is a proprietary feature that can be invoked to intelligently map colors to gray levels in text mode. SmartMap™ improves the legibility of flat panel displays by solving a common problem:

Most application programs are optimized for color CRT monitors using multiple colors. For example, a word processor might use a blue background with white characters for normal text, underlined text could be displayed in green, italicized text in yellow, and so on. This variety of colors, which is quite distinct on a color CRT monitor, can be illegible on a monochrome flat panel display if the colors are mapped to adjacent gray scale values. In the example, underlined and italicized text would be illegible if yellow is mapped to gray scale 4, green to gray scale 6 with the blue background mapped to gray scale 5.

SmartMap™ compares and adjusts foreground and background grayscale values to produce adequate display contrast on flat panel displays. The minimum contrast value and the foreground / background grayscale adjustment values are programmed in the 65540 / 545's Extension Registers. This feature can be disabled if desired.

Text Enhancement

Text Enhancement is another feature of the 65540 / 545 that improves image quality on flat panel displays. When enabled, the Text Enhancement feature displays Dim White as Bright White, thereby optimizing the contrast level on flat panels. Text Enhancement can be enabled and disabled by changing a bit in one of the Extension Registers.

Vertical & Horizontal Compensation

Vertical & Horizontal Compensation are programmable features that adjust the display to completely fill the flat panel display. Vertical Compensation increases the useable display area when running lower resolution software on a higher resolution panel. Unlike CRT monitors, flat panels have a fixed number of scan lines (e.g., 200, 400, 480 or 768 lines). Lower resolution software displayed on a higher resolution panel only partially fills the useable display area. For instance, 350-line EGA software displayed on a 480-line panel would leave 130 blank lines at the bottom of the display and 400-line VGA text or Mode 13 images would leave 80 blank lines at the bottom. The 65540 / 545 offers the following Vertical Compensation techniques to increase the useable screen area:

Vertical Centering displays text or graphics images in the center of the flat panel, with a border of unused area at the top and bottom of the display. Automatic Vertical Centering automatically adjusts the Display Start address such that the unused area at the top of the display equals the unused area at the bottom. Non-Automatic Vertical Centering enables the Display Start address to be set (by programming the Extension Registers) such that text or graphics images can be positioned anywhere on the display.

Line replication (referred to as "stretching") duplicates every Nth display line (where N is programmable), thus stretching text characters and graphic images an adjustable amount. The display can be stretched to completely fill the flat panel area. Double scanning, a form of line replication where every line is replicated, is useful for running 200-line software on a 400-line panel or 480-line software on a 1024-line panel.

Blank line insertion, inserts N lines (where N is programmable) between each line of text characters. Thus text can be evenly spaced to fill the entire panel display area without altering the height and shape of the text characters. Blank line insertion can be used in text mode only.

The 65540 / 545 implements the Tall Font™ scheme so that there are very few blank lines on the flat panel in text modes. For example, using an 8x19 Tall Font™ would fill 475 lines on a 480-line panel in VGA mode 3. Lines 1, 9, 12 of the 16 line font may be replicated to generate the 8x19 font. Alternately, line 0 may be replicated twice and line 15 replicated once. The Tall Font™ scheme is implemented in hardware thereby avoiding any compatibility issues.

Each of these Vertical Compensation techniques can be controlled by programming the Extension Registers. Each Vertical Compensation feature can be individually disabled, enabled, and adjusted. A combination of Vertical Compensation features can be used by adjusting the features' priority order. For example, text mode vertical compensation consists of four priority order options:

- Double Scanning+Line Insertion, Double Scanning, Line Insertion
- Double Scanning+Line Insertion, Line Insertion, Double Scanning
- Double Scanning+Tall Fonts, Double Scanning, Tall Fonts
- Double Scanning+Tall Fonts, Tall Fonts, Double Scanning

Text and graphics modes offer two Line Replication priority order options:

- Double Scanning+ Line Replication, Double Scanning, Line Replication
- Double Scanning+ Line Replication, Line Replication, Double Scanning

Horizontal Compensation techniques include Horizontal Compression, Horizontal Centering, and Horizontal Doubling. Horizontal Compression will compress 9-dot text to 8-dots such that 720-dot text in Hercules modes will fit on a 640-dot panel. Automatic Horizontal Centering automatically centers the display on a larger resolution panel such that the unused area at the left of the display equals the unused area at the right. Non-Automatic Horizontal Centering enables the left border to be set (by programming the Horizontal Centering Extension Register) such that the image can be positioned anywhere on the display. Automatic Horizontal Doubling will automatically double the display in the horizontal direction when the horizontal display width is equal to or less than half of the horizontal panel size.

ADVANCED POWER MANAGEMENT

Normal Operating Mode

The 65540 / 545 is a full-custom, sub-micron CMOS integrated circuit optimized for low power consumption during normal operation. The 65540 / 545 provides CAS-before-RAS refresh cycles for the DRAM display memory. The 65540 / 545 provides "mixed" 3.3V and 5.0V operation by providing dedicated Vcc pins for the 65540 / 545's internal logic, bus interface, memory interface, and display interface. If the 65540 / 545 internal logic operates at 3.3V, the memory, bus, and panel interfaces can independently operate at either 3.3V or 5.0V. The clock Vcc must be the same as the Vcc of the internal logic. The 65540 / 545 provides direct interface to 386/486 local bus which conserves power when 3.3V microprocessors are used. A flexible clock synthesizer is used to generate independent memory and video clocks. The 65540 / 545's performance-enhancement features minimize the memory clock frequency (and thus power consumption) required to achieve a given performance level. The 65540 / 545's proprietary gray scaling algorithm produces a flicker-free display with a minimum video clock and panel vertical refresh rate. (Note: the power consumption of the controller increases linearly with video clock frequency).

Panel Off Mode

In 'Panel Off' mode, the 65540 / 545 turns off both the flat panel and CRT interface logic. The VGA subsystem remains active, such that the CPU can read/write display memory and I/O registers. The 65540 / 545's video clock can be reduced significantly, saving power. Panel Off mode is activated by programming Extended Register XR52 bit-3=1.

Standby Mode

In 'Standby' mode, the 65540 / 545 suspends all CPU, memory and display activities. The 65540 / 545 places the DRAM in its self-refresh mode of operation, and the 65540 / 545's clock can be shut off. The VGA subsystem dissipates a minimum amount of power during Standby. Since the 65540 / 545 is a fully static device, the contents of the controller's registers and on-chip palette are maintained during Standby. Therefore, Standby mode provides fast Suspend / Resume modes. The Standby mode may be activated by forcing the STNDBY# pin low or programming XR52 bit-4 to '1'. The state of all 65540 / 545 pins during Standby mode is summarized in the tables on the following page.

CRT Power Management (DPMS)

The 65540 / 545 supports the VESA DPMS (Display Power Management Signaling) protocol. This includes the ability to independently stop HSYNC and/or VSYNC and hold them at a static level to signal the CRT to enter various power-saving states. Additionally, the RAMDAC may be powered down and the clock frequencies lowered for further power savings.

Mixed 3.3V and 5.0V Operation

The 65540 supports operation at either 5.0V ±10% or 3.3V ±0.3V. The 65540 also provides "mixed" 5V and 3.3V operation by providing dedicated Vcc pins for the 65540's internal logic, bus interface, memory interface, and display interface. Each dedicated Vcc can be either 5V or 3.3V, such that the 65540 internal logic operates at 3.3V and the various interfaces at either 3.3V or 5V. The clock VCC must be the same as the Vcc of the internal logic. The following table shows the relationship between the VCC inputs to the 65540 and the interface pins controlled by each Vcc input.

Vcc Pins	Interface	Pins Affected
80, 181	Internal Logic	--
9, 42	Bus	1-54, 178-201, 207
158	Memory A	145-177
142	Memory B	123-144
108	Memory C	90-122
66	Display	61-89
205, 206	Clock*	203, 204
59	DAC	55,57,58,60

* Must be same as the Vcc of the internal logic.

The 65545B1/B2 and 65545B1-5/B2-5 are the same part (die) that has been tested for operation at different voltage requirements.

The 65545B1/B2 provides a dedicated Vcc (Voltage) pins for the internal logic, clock synthesizer, bus interface, memory interface and the display interface. Each dedicated Vcc can be either 5V or 3.3V independently except for the internal core and clock synthesizer which must be at the same voltage level.

The 65545B1-5/B2-5 limits the internal core and clock synthesizer Vcc to 5V only operation and meets all 5V data sheet requirements.

CPU ACTIVITY INDICATOR / TIMER

The 65540 / 545 provides an output pin called ACTI (pin 53) to facilitate an orderly power-down sequence. The ACTI output is an active high signal which is driven high every time a valid VGA memory read/write operation or VGA I/O read/write operation is executed by the CPU. This signal may be used by power management circuitry to put the 65540 / 545 in Panel Off or Standby power down modes. The 65540 / 545 may also evoke its own low power operation by using the activity timer which monitors the ACTI signal. The activity timer will either disable the backlight or evoke Panel Off mode after a specified time interval. This time interval is programmed in 30 second intervals via Extension Register XR5C.

FULL COMPATIBILITY

The 65540 / 545 is fully compatible with the IBM™ VGA standard at the hardware, register, and BIOS level. The 65540 / 545 also provides enhanced backward compatibility to EGA™ and CGA™ standards without using NMIs. These controllers include a variety of features to provide compatibility on flat panel displays in addition to CRT monitors. Internal compensation techniques ensure that industry-standard software designed for different displays can be executed on the single flat panel used in an implementation. Mode initialization is supported at the BIOS and register levels, ensuring compatibility with all application software.

Write Protection

The 65540 / 545 has the ability to write protect most of the standard VGA registers. This feature is used to provide backwards compatibility with software written for older generation display types. The write protection is grouped into register sets and controlled by the Write Protect Register (XR15).

Extension Registers

The 65540 / 545 employs an "Extension" Register set to control its enhanced features. These Extension Registers provide control of the flat panel interface, flat panel timing, vertical compensation, SMARTMAP™, and Backwards Compatibility. These registers are always accessible as an index/data register set at port addresses 3D6-3D7h. None of the unused bits in the regular VGA registers are used for extensions.

Panel Interface Registers

Flat Panel Interface characteristics are controlled by a subset of the Extension Registers. These Registers select the panel type, data formatting, panel configuration, panel size, clock selection and video polarity. Since the 65540 / 545 is designed to support a wide range of panel types and sizes, the control of these features is fully programmable. The video polarity of text and graphics modes is independently selectable to allow black text on a white background and still provide normal graphics images.

Alternate Panel Timing Registers

Flat panel displays usually require sync signal timing that is different from a CRT. To provide full compatibility with the IBM VGA standard, alternate timing registers are used to allow independent timing of the sync signals for flat panel displays. Unlike the values programmed into the standard CRT timing registers, the value programmed into the alternate timing registers is dependent on the panel type used and is independent of the display mode.

Context Switching

For support of multi-tasking, windowing, and context switching, the entire state of the 65540 / 545 (internal registers) is readable and writable. This feature is fully compatible with IBM's VGA. Additional registers are provided to allow read back of internal latches not readable in the IBM VGA.

RESET, SETUP, AND TEST MODES

Reset Mode

When this mode is activated by pulling the RESET# pin low, the 65540 / 545 is forced to VGA-compatible mode and the CRT is selected as the active display. In addition, the 65540 / 545 is disabled; it must be enabled after deactivating the RESET# pin by writing to the Global Enable Register (102h in Setup Mode for ISA bus configurations or to port 3C3h or Local Bus configurations). Access to all Extension Registers is always enabled after reset (at 3D6/3D7h). The RESET# pin must be active for at least 64 clock cycles.

Setup Mode

In this mode, only the Global Enable register is accessible. In IBM-compatible PC implementations, setup mode is entered by writing a 1 to bit-4 of port 46E8h. This port is incorporated in the 65540 / 545. While in Setup mode, the video output is active if it was active prior to entering Setup mode and inactive if it was inactive prior to entering Setup mode. After power up, video BIOS can optionally disable the video 46E8 or 3C3 registers (via XR70) for compatibility in case other non-IBM-compatible peripheral devices use those ports.

Tri-State Mode

In this mode, all output pins of the 65540 / 545 chip may be disabled for testing of circuitry external to the chip. The 65540 / 545 will enter Tri-State mode if it sees a rising edge on XTALI during RESET with one of the display memory data pins pulled low (MAD0 pin 162). The 65540 / 545 will exit Tri-State mode with the enabling memory data pin (MAD0) high or RESET# low.

ICT (In-Circuit Test) Mode

In this mode, all digital pins of the 65540 / 545 chip may be tested individually to determine if they are properly connected (the analog RGB and RESET# pins cannot be tested in ICT mode). The 65540 / 545 will enter ICT mode if it sees a rising edge on XTALI during RESET with one of the display memory data pins pulled low (a different pin from the one used to enable Tri-state mode: MAD1). In ICT mode, all digital signal pins become inputs which are part of a long path starting at ENAVDD (pin 62) and proceeding to lower pin numbers around the chip to pin 1 (except analog pins 55, 57, 58, and 60) then to pin 208 and ending at VSYNC (pin 64). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time (XTALI last) and observing the effect on VSYNC. XTALI must be toggled last because rising edges on XTALI with either of the enabling memory data pins high or RESET# low will exit ICT mode. As a side effect, ICT mode effectively Tri-States all pins except VSYNC.

Mode of Operation	RESET# Pin††	STNDBY# Pin	Display Memory Access	Video Output
Reset	Low	xxx	-----	-----
Setup	-----	-----	No	Yes
Test	-----	-----	No	Yes
Standby†	High	Low	No	No
Panel-Off††	High	High	Yes	No

† It is illegal to go from Panel-Off Mode to Standby Mode. Panel-Off Mode must be exited first and a delay must occur of twice the value programmed into XR5B[7-4] prior to entering Standby Mode.

†† In 65540 ES Silicon reset is active high (RESET); in all following revisions reset is active low (RESET#).

Reset / Setup / Test / Standby / Panel-Off Mode Summary

CHIP ARCHITECTURE

The 65540 / 545 integrates six major internal modules:

Sequencer

The Sequencer generates all CPU and display memory timing. It controls CPU access of display memory by inserting cycles dedicated to CPU access. It also contains mask registers which can prevent writes to individual display memory planes.

CRT Controller

The CRT Controller generates all the sync and timing signals for the display and also generates the multiplexed row and column addresses used for both display refresh and CPU access of display memory.

Graphics Controller

The Graphics Controller interfaces the 8, 16, or 32-bit CPU data bus to the 32-bit internal data bus used by the four planes (Maps) of display memory. It also latches and supplies display memory data to the Attribute Controller for use in refreshing the screen image. For text modes this data is supplied in parallel form (character generator data and attribute code); for graphics modes it is converted to serial form (one bit from each of four bytes form a single pixel). The Graphics Controller can also perform any one of several types of logical operations on data while reading it from or writing it to display memory or the CPU data bus.

Attribute Controller

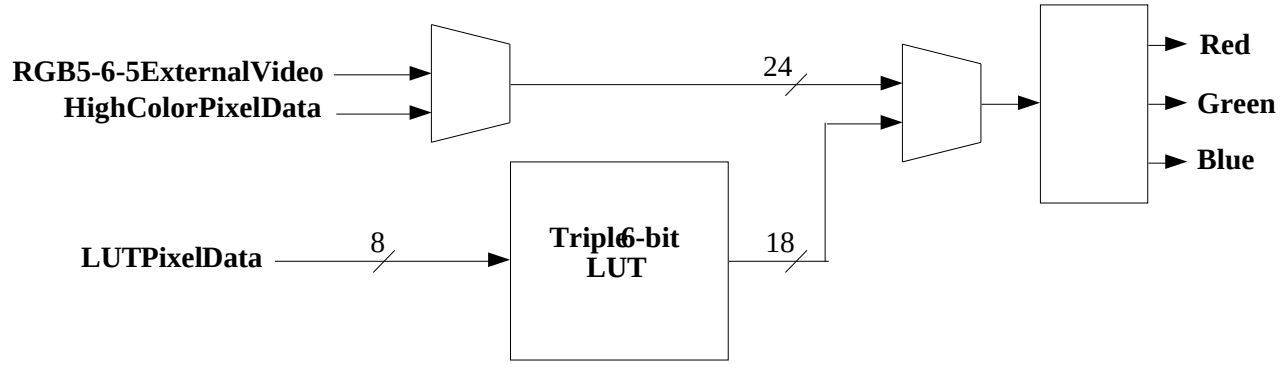
The Attribute Controller generates the 4-bit-wide video data stream used to refresh the display. This is created in text modes from a font pattern and an attribute code which pass through a parallel to serial conversion. In graphics modes, the display memory contains the 4-bit pixel data. In text and 16 color graphic modes the 4-bit pixel data acts as an index into a set of 16 internal color look-up registers which generate a 6-bit color value. Two additional bits of color data are added to provide an 8-bit address to the VGA color palette. In 256-color modes, two 4-bit values may be passed through the color look-up registers and assembled into one 8-bit video data value. In high-resolution 256-color modes, an 8-bit video data value may be provided directly, bypassing the attribute controller color lookup registers. Text and cursor blink, underline and horizontal scrolling are also the responsibility of the Attribute Controller.

VGA / Color Palette DAC

The 65540 / 545 integrates a VGA compatible triple 6-bit Color Lookup Table (sometimes referred to as a "CLUT" or just "LUT") and high speed 6/8-bit DACs. Additionally true color bypass modes are supported displaying color depths of up to 24bpp (8-red, 8-green, 8-blue). The palette DAC can switch between true color data and LUT data on a pixel by pixel basis. Thus, video overlays may be any arbitrary shape and can lie on any pixel boundary. The hardware cursor is also a true color bitmap which may overlay on any pixel boundary.

The internal palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard. In all bus interfaces the palette DAC automatically controls accesses to its registers to avoid data overrun. This is handled by holding RDY in the ISA configuration and by delaying RDY# for VL-Bus and local bus interfaces.

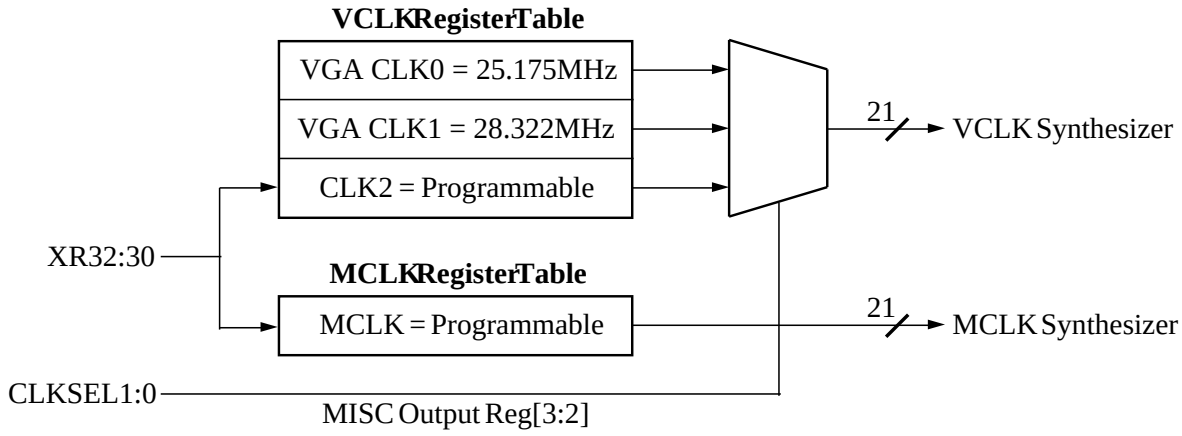
Extended RAMDAC display modes are selected in the Palette Control Register (XR06). Two 16bpp formats are supported: 5-red, 5-green, 5-blue Targa format and 5-red, 6-green, 5-blue XGA format. The internal Palette / DAC may also be disabled via the Palette Control Register (XR06).



Color Palette / DAC Internal Block Diagram

Clock Synthesizers

Integrated clock synthesizers support all pixel clock (VCLK) and memory clock (MCLK) frequencies which may be required by the 65540 / 545. Each of the two clock synthesizers may be programmed to output frequencies ranging between 1MHz and the maximum specified operating frequency for that clock in increments not exceeding 0.5%. The frequencies are set via a programmable 18-bit divisor value which contains fields for Phase Lock Loop (PLL), Voltage Controlled Oscillator (VCO) and Pre/Post Divide Control. A block diagram showing the clock synthesizer registers is included below. Refer to the Functional Description section of this document for additional information.



Clock Synthesizer Register Diagram

CONFIGURATION INPUTS

The 65540 / 545 can read up to nine configuration bits. These signals are sampled on memory address bus AA0-AA8 on the trailing edge of Reset. The 65540 / 545 implements pull-up resistors on-chip on all configuration input pins. If the user wishes to force a certain option, then a 4.7K ohm resistor may be used to pull-down the desired configuration pin.

65540 / 545 Pin #	Signal	Active	Functionality
145	LB#	Low	Bus Configuration
146	ISA#	Low	Bus Configuration
147	2X#	Low	2xCPU Clock Select
148	—	Low	Reserved
149	—	Low	Reserved (Do Not Use)
150	OS#	Low	External Oscillator Select
151	AD#	Low	ENABKL/ACTI=A26,A27
152	TS#	Low	Test Mode Enable
153	LV#	Low	Low Voltage Select

2X# (AA2) Pin 147	ISA# (AA1) Pin 146	LB# (AA0) Pin 145	Bus Functionality
Low	Low	Low	Reserved
Low	Low	High	Reserved
Low	High	Low	Reserved
Low	High	High	32-bit CPU Bus (2x clk)
High	Low	Low	Reserved
High	Low	High	16-bit ISA Bus
High	High	Low	PCI Bus (65545 only)
High	High	High	32-bit VL-Bus (1x clk)

AA2 determines the CPU clock rate for purposes of local bus implementation (0=2x CPU clock, 1=1x CPU clock). AA3 has no hardware function, but the status of the pin is latched in extension register 1 bit 3 on reset so it may be used to input system-specific information. AA4 is reserved and should be sampled high on reset. AA5, if forced to 0, indicates that a reference frequency of 14.31818 MHz must be input on XTALI (pin 203). AA6 selects between ACTI/ENABKL and A26-27 on pins 53-54 (default is ENABKL and ACTI). AA7, when forced low, enables clock test mode (VCLK and MCLK are output on A24-25 (pins 29-30). AA8, when forced low, selects 3.3V level of operation for the internal logic and the clock core.

VIRTUAL SWITCH REGISTER

The 65540 / 545 implements a 'virtual switch register'. In 'EGA' mode, the sense bit of the Feature control register (3C2 bit 4) may be set up to read a selected bit from the 'virtual switch register' (an extension register set up by BIOS at initialization time) instead of reading the state of the internal comparator output.

LIGHT PEN REGISTERS

In the CGA and Hercules modes, the contents of the Display Address counter are saved at the end of the frame before being reset. The saved value can be read in the CRT Controller Register space at indices 10h and 11h. This allows simulation of a light pen hit in CGA and Hercules modes.

BIOS ROM INTERFACE

In typical ISA bus and VL-Bus applications, the 65540 / 545 is placed on the motherboard and the video BIOS is integrated with the system BIOS (in PCI Bus, the video BIOS is always included in the system BIOS). A separate signal (ROMCS#) is generated on the A24 pin for ISA bus or may be created external to the 65540 / 545 for implementing a separate external ROM BIOS.

Typically, an 8-bit BIOS is implemented with one external ROM chip. A 16-bit dedicated video BIOS ROM could be implemented with the 65540 / 545 if required using two BIOS ROM chips, an external PAL, and a 74LS244 buffer. However, a higher-performance and lower-cost video system will result from implementation of the video BIOS as either an 8-bit dedicated video BIOS ROM or as part of the system BIOS and having the video BIOS be copied into system RAM by the system BIOS on startup.

Chips and Technologies, Inc. supplies a video BIOS that is optimized for the 65540 / 545 hardware. The BIOS supports the extended functions of the 65540 / 545, such as switching between the flat panel and the CRT, SMARTMAP™, Vertical Compensation, and palette load/save. The BIOS Modification Program (BMP) enables OEMs to tailor their feature set by programming the extended functions. CHIPS offers the BIOS as a standard production version, a customized version, or as source code.

PACKAGE

The 65540 / 545 is available in a EIAJ-standard 208-pin plastic flat pack with a 28 x 28 mm body size and 0.5 mm (19.7 mil) lead pitch.

APPLICATION SCHEMATIC EXAMPLES

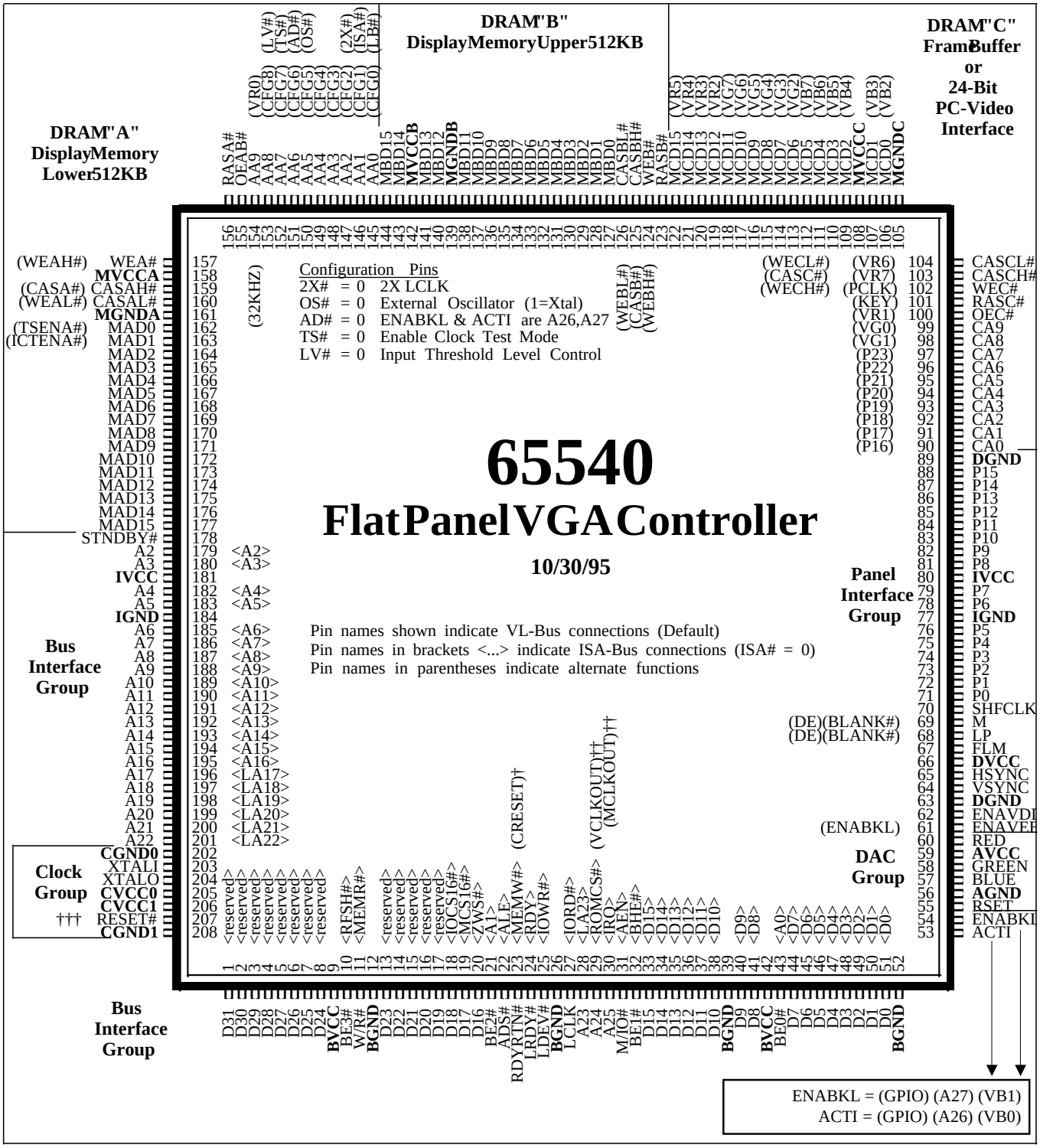
This document includes application schematic examples of the following:

1. Bus Interface - 16-bit EISA/ISA Bus
   Bus Interface - 32-bit 486 Local Bus (1x Clock)
   Bus Interface - 32-bit VL-Bus (1x Clock)
   Bus Interface - 32-bit PCI Bus

2. Display Memory Interface

3. CRT / Panel Interface

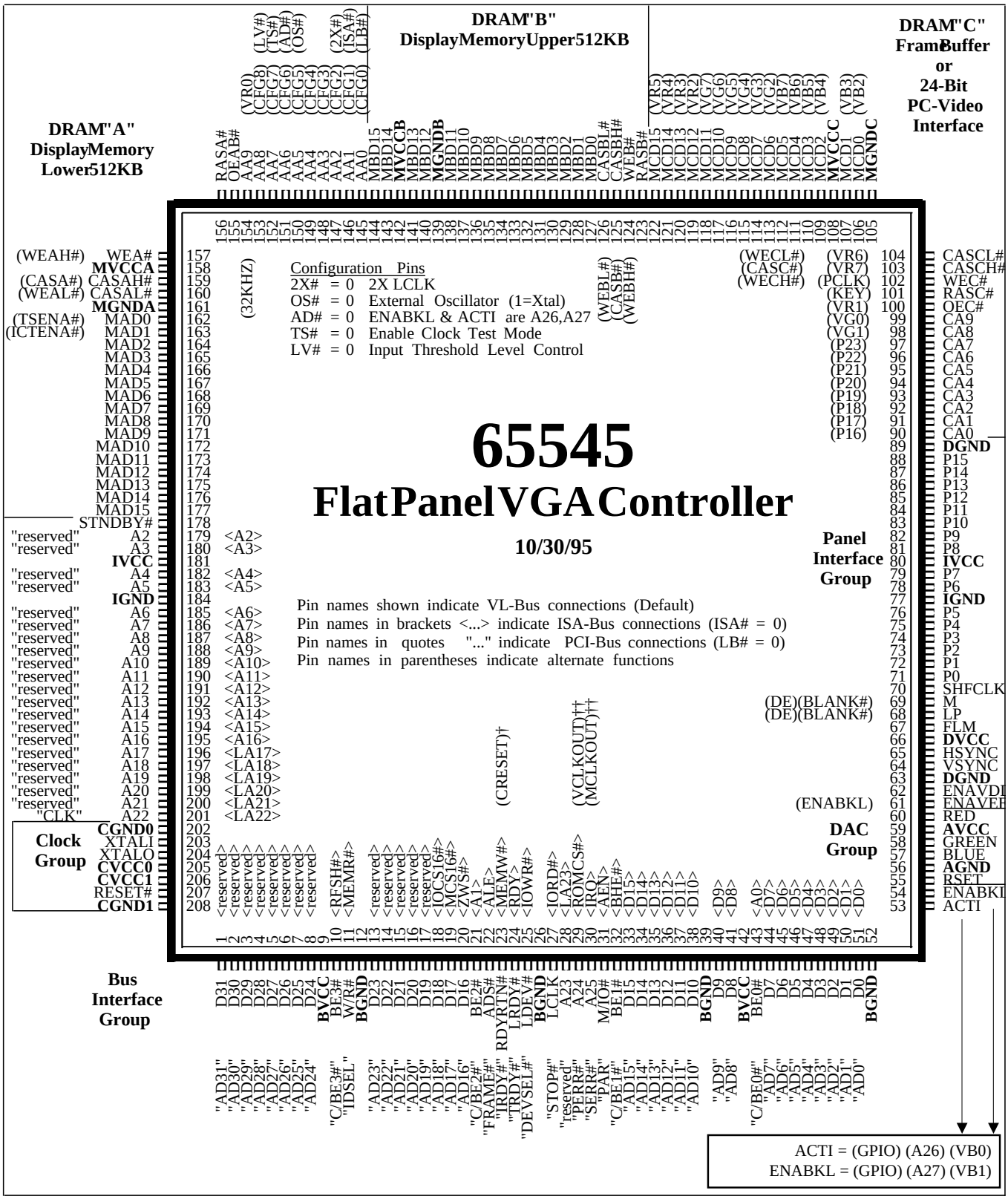
4. PC Video Interface



† In 2x clock mode, pin 23 becomes CRESET instead of RDYRTN#

†† In Test mode, pin 29 becomes VCLKOUT and pin 30 becomes MCLKOUT

††† In 65540 ES Silicon reset is active high (RESET); in all following revisions reset is active low (RESET#).



† In 2x clock mode, pin 23 becomes CRESET instead of RDYRTN#

†† In Test mode, pin 29 becomes VCLKOUT and pin 30 becomes MCLKOUT

Pin Name			Pin #	Dir	Drive
A2			179	In	—
A3			180	In	—
A4			182	In	—
A5			183	In	—
A6			185	In	—
A7			186	In	—
A8			187	In	—
A9			188	In	—
A10			189	In	—
A11			190	In	—
A12			191	In	—
A13			192	In	—
A14			193	In	—
A15			194	In	—
A16			195	In	—
A17	(LA17)		196	In	—
A18	(LA18)		197	In	—
A19	(LA19)		198	In	—
A20	(LA20)		199	In	—
A21	(LA21)		200	In	—
A22	(LA22)	"CLK"	201	In	—
A23	(LA23)		28	In	—
A24	(ROMCS#)	"PERR#"	29	I/O	8mA
A25	(IRQ)	"SERR#"	30	I/O	8mA
AA0	(CFG0)	(LB#)	145	I/O	4mA
AA1	(CFG1)	(ISA#)	146	I/O	4mA
AA2	(CFG2)	(2X#)	147	I/O	4mA
AA3	(CFG3)		148	I/O	4mA
AA4	(CFG4)		149	I/O	4mA
AA5	(CFG5)	(OS#)	150	I/O	4mA
AA6	(CFG6)	(AD#)	151	I/O	4mA
AA7	(CFG7)	(TS#)	152	I/O	4mA
AA8	(CFG8)	(LV#)	153	I/O	4mA
AA9	(32KHZ)	(VR0)	154	I/O	4mA
ACTI	(A26)	(VB0)	53	I/O	8mA
ADS#	(ALE)	"FRAME#"	22	In	—
AGND			56	—	—
AVCC			59	—	—
BE0#	(A0)	"C/BE0#"	43	In	—
BE1#	(BHE#)	"C/BE1#"	32	In	—
BE2#	(A1)	"C/BE2#"	21	In	—
BE3#	(RFSH#)	"C/BE3#"	10	In	—
BLUE			57	Out	—
BGND	(Bus)		12	—	—
BGND	(Bus)		26	—	—
BGND	(Bus)		39	—	—
BGND	(Bus)		52	—	—
BVCC	(Bus)		9	—	—
BVCC	(Bus)		42	—	—
CA0	(P16)		90	Out	4mA
CA1	(P17)		91	Out	4mA
CA2	(P18)		92	Out	4mA
CA3	(P19)		93	Out	4mA
CA4	(P20)		94	Out	4mA
CA5	(P21)		95	Out	4mA
CA6	(P22)		96	Out	4mA
CA7	(P23)		97	Out	4mA
CA8	(VG1)		98	I/O	4mA
CA9	(VG0)		99	I/O	4mA
CASAH#	(CASA#)		159	Out	4mA
CASAL#	(WEAL#)		160	Out	4mA
CASBH#	(CASB#)		125	Out	4mA
CASBL#	(WEBL#)		126	Out	4mA
CASCH#	(CASC#)	(VR7)	103	I/O	4mA
CASCL#	(WECL#)	(VR6)	104	I/O	4mA
CGND0	(Clock)		202	—	—
CGND1	(Clock)		208	—	—
CVCC0	(Clock)		205	—	—
CVCC1	(Clock)		206	—	—
Note: Drive = 5V low drive and 3V high driv					

Pin Name			Pin #	Dir	Drive
D0		"AD0"	51	I/O	8mA
D1		"AD1"	50	I/O	8mA
D2		"AD2"	49	I/O	8mA
D3		"AD3"	48	I/O	8mA
D4		"AD4"	47	I/O	8mA
D5		"AD5"	46	I/O	8mA
D6		"AD6"	45	I/O	8mA
D7		"AD7"	44	I/O	8mA
D8		"AD8"	41	I/O	8mA
D9		"AD9"	40	I/O	8mA
D10		"AD10"	38	I/O	8mA
D11		"AD11"	37	I/O	8mA
D12		"AD12"	36	I/O	8mA
D13		"AD13"	35	I/O	8mA
D14		"AD14"	34	I/O	8mA
D15		"AD15"	33	I/O	8mA
D16	(ZWS#)	"AD16"	20	I/O	8mA
D17	(MCS16#)	"AD17"	19	I/O	8mA
D18	(IOCS16#)	"AD18"	18	I/O	8mA
D19		"AD19"	17	I/O	8mA
D20		"AD20"	16	I/O	8mA
D21		"AD21"	15	I/O	8mA
D22		"AD22"	14	I/O	8mA
D23		"AD23"	13	I/O	8mA
D24		"AD24"	8	I/O	8mA
D25		"AD25"	7	I/O	8mA
D26		"AD26"	6	I/O	8mA
D27		"AD27"	5	I/O	8mA
D28		"AD28"	4	I/O	8mA
D29		"AD29"	3	I/O	8mA
D30		"AD30"	2	I/O	8mA
D31		"AD31"	1	I/O	8mA
DGND	(Display)		63	—	—
DGND	(Display)		89	—	—
DVCC	(Display)		66	—	—
ENABKL	(A27)	(VB1)	54	I/O	8mA
ENAVDD			62	Out	8mA
ENAVEE	(ENABKL)		61	Out	8mA
FLM			67	Out	8mA
GREEN			58	Out	—
HSYNC			65	Out	12mA
IGND	(Internal Logic)		77	—	—
IGND	(Internal Logic)		184	—	—
IVCC	(Internal Logic)		80	—	—
IVCC	(Internal Logic)		181	—	—
LCLK	(IORD#)	"STOP#"	27	In	—
LDEV#	(IOWR#)	"DEVSEL#"	25	I/O	12mA
LRDY#	(RDY)	"TRDY#"	24	Out	12mA
LP	(BLANK#)	(DE)	68	Out	8mA
M	(BLANK#)	(DE)	69	Out	8mA
MAD0	(TSENA#)		162	I/O	2mA
MAD1	(ICTENA#)		163	I/O	2mA
MAD2			164	I/O	2mA
MAD3			165	I/O	2mA
MAD4			166	I/O	2mA
MAD5			167	I/O	2mA
MAD6			168	I/O	2mA
MAD7			169	I/O	2mA
MAD8			170	I/O	2mA
MAD9			171	I/O	2mA
MAD10			172	I/O	2mA
MAD11			173	I/O	2mA
MAD12			174	I/O	2mA
MAD13			175	I/O	2mA
MAD14			176	I/O	2mA
MAD15			177	I/O	2mA
MBD0			127	I/O	2mA
MBD1			128	I/O	2mA
MBD2			129	I/O	2mA
MBD3			130	I/O	2mA

Pin Name			Pin #	Dir	Drive
MBD4			131	I/O	2mA
MBD5			132	I/O	2mA
MBD6			133	I/O	2mA
MBD7			134	I/O	2mA
MBD8			135	I/O	2mA
MBD9			136	I/O	2mA
MBD10			137	I/O	2mA
MBD11			138	I/O	2mA
MBD12			140	I/O	2mA
MBD13			141	I/O	2mA
MBD14			143	I/O	2mA
MBD15			144	I/O	2mA
MCD0	(VB2)		106	I/O	2mA
MCD1	(VB3)		107	I/O	2mA
MCD2	(VB4)		109	I/O	2mA
MCD3	(VB5)		110	I/O	2mA
MCD4	(VB6)		111	I/O	2mA
MCD5	(VB7)		112	I/O	2mA
MCD6	(VG2)		113	I/O	2mA
MCD7	(VG3)		114	I/O	2mA
MCD8	(VG4)		115	I/O	2mA
MCD9	(VG5)		116	I/O	2mA
MCD10	(VG6)		117	I/O	2mA
MCD11	(VG7)		118	I/O	2mA
MCD12	(VR2)		119	I/O	2mA
MCD13	(VR3)		120	I/O	2mA
MCD14	(VR4)		121	I/O	2mA
MCD15	(VR5)		122	I/O	2mA
MGNDA	(Memory A)		161	—	—
MGNDB	(Memory B)		139	—	—
MGNDC	(Memory C)		105	—	—
M/IO#	(AEN)	"PAR"	31	I/O†	4mA
MVCCA	(Memory A)		158	—	—
MVCCB	(Memory B)		142	—	—
MVCCC	(Memory C)		108	—	—
OEAB#			155	Out	4mA
OEC#	(VR1)		100	I/O	4mA
P0			71	Out	8mA
P1			72	Out	8mA
P2			73	Out	8mA
P3			74	Out	8mA
P4			75	Out	8mA
P5			76	Out	8mA
P6			78	Out	8mA
P7			79	Out	8mA
P8			81	Out	8mA
P9			82	Out	8mA
P10			83	Out	8mA
P11			84	Out	8mA
P12			85	Out	8mA
P13			86	Out	8mA
P14			87	Out	8mA
P15			88	Out	8mA
RASA#			156	Out	4mA
RASB#			123	Out	4mA
RASC#	(KEY)		101	I/O	4mA
RRTN#<MEMW#>		"IRDY#"	23	In	—
RED			60	Out	—
RESET#	(540 Rev 0=RESET)		207	In	—
RSET			55	In	—
SHFCLK			70	Out	8mA
STNDBY#			178	In	—
VSYNC			64	Out	12mA
WEA#	(WEAH#)		157	Out	4mA
WEB#	(WEBH#)		124	Out	4mA
WEC#	(WECH#/(PCLK)		102	Out	4mA
W/R#	(MEMR#)	"IDSEL"	11	In	—
XTALI			203	In	—
XTALO			204	Out	—
† I/O in 65545 only for PCI, In for 65540					

PIN LIST - BUS INTERFACE

Pin #	Type	VCC Plane	I_{OH}	I_{OL}	Load	65545 PCI Bus	VL-Bus	CPUDirectLB	ISA Bus
207	In	Bus	–	–	–	RESET#	RESET#	RESET#	RESET#
25	I/O	Bus	–12	12	150	DEVSEL#	LDEV#	LDEV#	IOWR#
24	Out	Bus	–12	12	150	TRDY#	LRDY#	LRDY#	RDY
23	In	Bus	–	–	–	IRDY#	RDYRTN#	CRESET	MEMW#
11	I/O	Bus	–4	4	150	IDSEL	W/R#	W/R#	MEMR#
31	I/O	Bus	–4	4	150	PAR	M/IO#	M/IO#	AEN
22	In	Bus	–	–	–	FRAME#	ADS#	ADS#	ALE
27	In	Bus	–	–	–	STOP#	LCLK	CLK2X	IORD#
32	In	Bus	–	–	–	C/BE1#	BE1#	BE1#	BHE#
10	In	Bus	–	–	–	C/BE3#	BE3#	BE3#	RFSH#
43	In	Bus	–	–	–	C/BE0#	BE0#	BE0#	A0
21	In	Bus	–	–	–	C/BE2#	BE2#	BE2#	A1
179	In	Bus	–	–	–	–	A2	A2	A2
180	In	Bus	–	–	–	–	A3	A3	A3
182	In	Bus	–	–	–	–	A4	A4	A4
183	In	Bus	–	–	–	–	A5	A5	A5
185	In	Bus	–	–	–	–	A6	A6	A6
186	In	Bus	–	–	–	–	A7	A7	A7
187	In	Bus	–	–	–	–	A8	A8	A8
188	In	Bus	–	–	–	–	A9	A9	A9
189	In	Bus	–	–	–	–	A10	A10	A10
190	In	Bus	–	–	–	–	A11	A11	A11
191	In	Bus	–	–	–	–	A12	A12	A12
192	In	Bus	–	–	–	–	A13	A13	A13
193	In	Bus	–	–	–	–	A14	A14	A14
194	In	Bus	–	–	–	–	A15	A15	A15
195	In	Bus	–	–	–	–	A16	A16	A16
196	In	Bus	–	–	–	–	A17	A17	LA17
197	In	Bus	–	–	–	–	A18	A18	LA18
198	In	Bus	–	–	–	–	A19	A19	LA19
199	In	Bus	–	–	–	–	A20	A20	LA20
200	In	Bus	–	–	–	–	A21	A21	LA21
201	In	Bus	–	–	–	CLK	A22	A22	LA22
28	In	Bus	–	–	–	–	A23	A23	LA23
29	I/O	Bus	–8	8	150	PERR#††	A24††	A24††	ROMCS#††
30	I/O	Bus	–8	8	150	SERR#††	A25††	A25††	IRQ††
53	I/O	Bus	–8	8	150	ACTI	A26 †	A26 †	ACTI
54	I/O	Bus	–8	8	150	ENABKL	A27 †	A27 †	ENABKL

† These two pins usually function as ACTI and ENABKL, but can be reconfigured as additional address msbs (for 386/486/VL-Bus only) via configuration bit-6 (see other tables and pin descriptions for more details)

†† In internal clock synthesizer test mode, MCLK is output on A25 and VCLK is output on A24.

LB#	ISA#	2X#	Bus Configuration	
1	1	1	VL-Bus	(1x clock) Pin-23 = RDYRTN#
1	1	0	CPU-Direct	(2x clock) Pin-23 = CRESET
1	0	1	ISA Bus	
1	0	0	-reserved-	
0	1	1	PCI Bus	(65545 only)
0	1	0	-reserved-	
0	0	1	-reserved-	
0	0	0	-reserved-	

Note: I_{OL} and I_{OH} drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)

Note: I_{OL}/I_{OH} are specified in mA; Load is specified in pF

PIN LIST - BUS INTERFACE

Pin #	Type	V_{CC} Plane	I_{OH}	I_{OL}	Load	65545 PCI Bus	VL-Bus	CPUDirectLB	ISA Bus
51	I/O	Bus	–8	8	150	AD0	D0	D0	D0
50	I/O	Bus	–8	8	150	AD1	D1	D1	D1
49	I/O	Bus	–8	8	150	AD2	D2	D2	D2
48	I/O	Bus	–8	8	150	AD3	D3	D3	D3
47	I/O	Bus	–8	8	150	AD4	D4	D4	D4
46	I/O	Bus	–8	8	150	AD5	D5	D5	D5
45	I/O	Bus	–8	8	150	AD6	D6	D6	D6
44	I/O	Bus	–8	8	150	AD7	D7	D7	D7
41	I/O	Bus	–8	8	150	AD8	D8	D8	D8
40	I/O	Bus	–8	8	150	AD9	D9	D9	D9
38	I/O	Bus	–8	8	150	AD10	D10	D10	D10
37	I/O	Bus	–8	8	150	AD11	D11	D11	D11
36	I/O	Bus	–8	8	150	AD12	D12	D12	D12
35	I/O	Bus	–8	8	150	AD13	D13	D13	D13
34	I/O	Bus	–8	8	150	AD14	D14	D14	D14
33	I/O	Bus	–8	8	150	AD15	D15	D15	D15
20	I/O	Bus	–8	8	150	AD16	D16	D16	ZWS#
19	I/O	Bus	–8	8	150	AD17	D17	D17	MCS16#
18	I/O	Bus	–8	8	150	AD18	D18	D18	IOCS16#
17	I/O	Bus	–8	8	150	AD19	D19	D19	—
16	I/O	Bus	–8	8	150	AD20	D20	D20	—
15	I/O	Bus	–8	8	150	AD21	D21	D21	—
14	I/O	Bus	–8	8	150	AD22	D22	D22	—
13	I/O	Bus	–8	8	150	AD23	D23	D23	—
8	I/O	Bus	–8	8	150	AD24	D24	D24	—
7	I/O	Bus	–8	8	150	AD25	D25	D25	—
6	I/O	Bus	–8	8	150	AD26	D26	D26	—
5	I/O	Bus	–8	8	150	AD27	D27	D27	—
4	I/O	Bus	–8	8	150	AD28	D28	D28	—
3	I/O	Bus	–8	8	150	AD29	D29	D29	—
2	I/O	Bus	–8	8	150	AD30	D30	D30	—
1	I/O	Bus	–8	8	150	AD31	D31	D31	—

Note: IOL and IOH drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)

Note: IOL/IOH are specified in mA; Load is specified in pF

PIN LIST - DISPLAY MEMORY INTERFACE

Pin #	Type	IOH	IOL	Load	Function	Alt	Alt
145	I/O	–4	4	50	AA0	CFG0	–
146	I/O	–4	4	50	AA1	CFG1	–
147	I/O	–4	4	50	AA2	CFG2	–
148	I/O	–4	4	50	AA3	CFG3	–
149	I/O	–4	4	50	AA4	CFG4	–
150	I/O	–4	4	50	AA5	CFG5	–
151	I/O	–4	4	50	AA6	CFG6	–
152	I/O	–4	4	50	AA7	CFG7	–
153	I/O	–4	4	50	AA8	CFG8	–
154	I/O	–4	4	50	AA9	32KHZ	VR0
90	Out	–4	4	50	CA0	P16	–
91	Out	–4	4	50	CA1	P17	–
92	Out	–4	4	50	CA2	P18	–
93	Out	–4	4	50	CA3	P19	–
94	Out	–4	4	50	CA4	P20	–
95	Out	–4	4	50	CA5	P21	–
96	Out	–4	4	50	CA6	P22	–
97	Out	–4	4	50	CA7	P23	–
98	I/O	–4	4	50	CA8	–	VG1
99	I/O	–4	4	50	CA9	–	VG0
156	Out	–4	4	50	RASA#	–	–
123	Out	–4	4	50	RASB#	–	–
101	I/O	–4	4	50	RASC#	–	KEY
160	Out	–4	4	50	CASAL#	WEAL#	–
159	Out	–4	4	50	CASAH#	CASA#	–
126	Out	–4	4	50	CASBL#	WEBL#	–
125	Out	–4	4	50	CASBH#	CASB#	–
104	I/O	–4	4	50	CASCL#	WECL#	VR6
103	I/O	–4	4	50	CASCH#	CASC#	VR7
157	Out	–4	4	50	WEA#	WEAH#	–
124	Out	–4	4	50	WEB#	WEBH#	–
102	Out	–4	4	50	WEC#	WECH#	PCLK
155	Out	–4	4	50	OEAB#	–	–
100	I/O	–4	4	50	OEC#	–	VR1

Pin #	Type	IOH	IOL	Load	Function	Alt	Alt
162	I/O	–2	2	30	MAD0		
163	I/O	–2	2	30	MAD1		
164	I/O	–2	2	30	MAD2		
165	I/O	–2	2	30	MAD3		
166	I/O	–2	2	30	MAD4		
167	I/O	–2	2	30	MAD5		
168	I/O	–2	2	30	MAD6		
169	I/O	–2	2	30	MAD7		
170	I/O	–2	2	30	MAD8		
171	I/O	–2	2	30	MAD9		
172	I/O	–2	2	30	MAD10		
173	I/O	–2	2	30	MAD11		
174	I/O	–2	2	30	MAD12		
175	I/O	–2	2	30	MAD13		
176	I/O	–2	2	30	MAD14		
177	I/O	–2	2	30	MAD15		
127	I/O	–2	2	30	MBD0		
128	I/O	–2	2	30	MBD1		
129	I/O	–2	2	30	MBD2		
130	I/O	–2	2	30	MBD3		
131	I/O	–2	2	30	MBD4		
132	I/O	–2	2	30	MBD5		
133	I/O	–2	2	30	MBD6		
134	I/O	–2	2	30	MBD7		
135	I/O	–2	2	30	MBD8		
136	I/O	–2	2	30	MBD9		
137	I/O	–2	2	30	MBD10		
138	I/O	–2	2	30	MBD11		
140	I/O	–2	2	30	MBD12		
141	I/O	–2	2	30	MBD13		
143	I/O	–2	2	30	MBD14		
144	I/O	–2	2	30	MBD15		
106	I/O	–2	2	30	MCD0	VB2	
107	I/O	–2	2	30	MCD1	VB3	
109	I/O	–2	2	30	MCD2	VB4	
110	I/O	–2	2	30	MCD3	VB5	
111	I/O	–2	2	30	MCD4	VB6	
112	I/O	–2	2	30	MCD5	VB7	
113	I/O	–2	2	30	MCD6	VG2	
114	I/O	–2	2	30	MCD7	VG3	
115	I/O	–2	2	30	MCD8	VG4	
116	I/O	–2	2	30	MCD9	VG5	
117	I/O	–2	2	30	MCD10	VG6	
118	I/O	–2	2	30	MCD11	VG7	
119	I/O	–2	2	30	MCD12	VR2	
120	I/O	–2	2	30	MCD13	VR3	
121	I/O	–2	2	30	MCD14	VR4	
122	I/O	–2	2	30	MCD15	VR5	

Note: IOL and IOH drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)

Note: IOL/IOH are specified in mA; Load is specified in pF

PIN PIST - CRT INTERFACE

Pin #	Type	I_{OH}	I_{OL}	Load	Function	Alt
65	Out	–12	12	150	HSYNC	–
64	Out	–12	12	150	VSYNC	–
55	–	–	–	–	RSET	–
60	Out	–	–	–	RED	–
58	Out	–	–	–	GREEN	–
57	Out	–	–	–	BLUE	–
59	Vcc	–	–	–	AVCC	–
56	Gnd	–	–	–	AGND	–

PIN PIST - PANEL INTERFACE

Pin #	Type	I_{OH}	I_{OL}	Load	Function	Alt	Alt
67	Out	–8	8	80	FLM	–	
68	Out	–8	8	80	LP	BLANK#	DE
69	Out	–8	8	80	M	BLANK#	DE
70	Out	–8	8	80	SHFCLK	–	
71	Out	–8	8	80	P0	–	
72	Out	–8	8	80	P1	–	
73	Out	–8	8	80	P2	–	
74	Out	–8	8	80	P3	–	
75	Out	–8	8	80	P4	–	
76	Out	–8	8	80	P5	–	
78	Out	–8	8	80	P6	–	
79	Out	–8	8	80	P7	–	
81	Out	–8	8	80	P8	–	
82	Out	–8	8	80	P9	–	
83	Out	–8	8	80	P10	–	
84	Out	–8	8	80	P11	–	
85	Out	–8	8	80	P12	–	
86	Out	–8	8	80	P13	–	
87	Out	–8	8	80	P14	–	
88	Out	–8	8	80	P15	–	

PIN LIST - POWER MANAGEMENT

Pin #	Type	I_{OH}	I_{OL}	Load	Function	Alt	Alt
62	Out	–8	8	80	ENAVDD	–	–
61	Out	–8	8	80	ENAVEE	ENABKL	–
54	I/O	–8	8	80	ENABKL	A27	VB1
53	I/O	–8	8	80	ACTI	A26	VB0
178	In	–	–	–	STNDBY#	–	–

PIN LIST - CLOCK

Pin #	Type	I_{OH}	I_{OL}	Load	Function	Alt
203	In	–	–	–	XTALI	–
204	Out	–2	2	50	XTALO	–
205	Vcc	–	–	–	CVCC0	–
206	Vcc	–	–	–	CVCC1	–
202	Gnd	–	–	–	CGND0	–
208	Gnd	–	–	–	CGND1	–

Note: CVCC must equal IVCC

PIN LIST - POWER & GROUND

Pin #	Type	I_{OH}	I_{OL}	Load	Function
80	Vcc	–	–	–	IVCC
181	Vcc	–	–	–	IVCC
77	Gnd	–	–	–	IGND
184	Gnd	–	–	–	IGND
9	Vcc	–	–	–	BVCC
42	Vcc	–	–	–	BVCC
12	Gnd	–	–	–	BGND
26	Gnd	–	–	–	BGND
39	Gnd	–	–	–	BGND
52	Gnd	–	–	–	BGND
158	Vcc	–	–	–	MVCCA
142	Vcc	–	–	–	MVCCB
108	Vcc	–	–	–	MVCCC
161	Gnd	–	–	–	MGNDA
139	Gnd	–	–	–	MGNDB
105	Gnd	–	–	–	MGNDC
66	Vcc	–	–	–	DVCC
63	Gnd	–	–	–	DGND
89	Gnd	–	–	–	DGND

Note: IVCC must equal CVCC

Note: IOL and IOH drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)

Note: IOL/IOH are specified in mA; Load is specified in pF

PIN DESCRIPTIONS **ISA/CPU Direct/VL-Bus Interface**

Pin #	Pin Name		Type	Active	Description
207	RESET#		In	Low	Reset. For VL-Bus interfaces, connect to RESET#. For direct CPU local bus interfaces, connect to the system reset generated by the motherboard system logic for all peripherals (not the RESET# pin of the processor). For ISA bus interfaces, RESET must be inverted before connection to this pin.
22	ADS#		In	Low	Address Strobe. In VL-Bus and CPU local bus interfaces indicates valid address and control signal information is present. It is used for all decodes and to indicate the start of a bus cycle.
		(ALE)	In	High	
31	M/IO#		In	Both	Memory / IO. In VL-Bus and CPU local bus interfaces indicates memory or I/O cycle: 1 = memory, 0 = I/O.
		(AEN)	In	High	
11	W/R#		In	Both	Write / Read. This control signal indicates a write (high) or read (low) operation. It is sampled on the rising edge of the (internal) 1x CPU clock when ADS# is active.
		(MEMR#)	In	Low	
23	RDYRTN#	for 1x clock config	In	Low	Ready Return. Handshaking signal in VL-Bus interface indicating synchronization of RDY# by the local bus master / controller to the processor. Upon receipt of this LCLK-synchronous signal the 65540 / 545 will stop driving the bus (if a read cycle was active) and terminate the current cycle.
	CRESET	for 2x clock config	In	High	
		(MEMW#)	In	Low	
24	LRDY#		Out/OC	Low	Local Ready. Driven low during VL-Bus and CPU local bus cycles to indicate the current cycle should be completed. This signal is driven high at the end of the cycle, then tri-stated. In ISA bus interfaces, this signal is active high and may be connected directly to the ISA bus RDY pin.
		(RDY)	Out/OC	High	
25	LDEV#		Out	Low	Local Device. In VL-Bus and CPU local bus interfaces, this pin indicates that the 65540 / 545 owns the current cycle based on the memory or I/O address which has been broadcast. For VL-Bus, it is a direct output reflecting a straight address decode.
		(IOWR#)	In	Low	
27	LCLK		In	Both	Local Clock. In VL-Bus this pin is connected to the CPU 1x clock. In CPU local bus interfaces it is connected to the CPU 1x or 2x clock. If the input is a 2x clock, the processor reset signal must be connected to CRESET (pin 23) for synchronization of the clock phase.
		(IORD#)	In	Low	

Note: Pin names in parentheses (...) indicate alternate functions (in this case, ISA bus control)

PIN DESCRIPTIONS **ISA/CPU Direct/VL-Bus Interface (continued)**

Pin #	Pin Name	Type	Active	Description
43	BE0# (A0) (BLE#)	In	Low	Byte Enable 0. Indicates data transfer on D7:D0 for the current cycle. A0 address input in ISA interfaces. In 16-bit local bus interfaces indicates the low order byte at the current (16-bit) word address is being accessed.
32	BE1# (BHE#)	In	Low	Byte Enable 1. Indicates data transfer on D15:D8 for the current cycle. In ISA, indicates high order byte at the current (16-bit) word address is being accessed.
21	BE2# (A1)	In	Low	Byte Enable 2. Indicates data transfer on D23:D16 for the current cycle. A1 address in ISA & 16-bit local bus.
10	BE3# (RFSH#)	In	Low	Byte Enable 3. BE3# indicates that data is to be transferred over the data bus on D31:24 during the current access. Refresh input in ISA interfaces. Disconnected in 16-bit local bus interfaces.
179	A2	In	High	System Address Bus. In ISA, VL-Bus, and direct CPU interfaces, the address pins are connected directly to the bus. In 386 SX local bus interfaces BE2# is address input A1, BE0# is BLE#, and BE1# is BHE#. In ISA bus interfaces BE2# is address A1, BE0# is address A0, BE1# is BHE#, A17-23 are LA17-23, and A24 is ROMCS# (indicates valid ROM access to memory address range 0C0000-0C7FFFh). Address inputs through A23 are always available; A24-27 may be optionally used for other functions: In internal clock synthesizer test mode (TS#=0 at Reset), A24 becomes VCLK out and A25 becomes MCLK out. A25 may alternately be used as a programmable polarity IRQ output. Set when interrupt on VSYNC is enabled. Cleared by reprogramming register 11h in the CRT Controller. See also XR14 bit–7. For 24-bit RGB Video input, A26-27 may be used as the two lsbs of the Blue Video. Otherwise, A26 and A27 may be used as General Purpose I/O pins or as Activity Indicator and Enable Backlight respectively (see panel interface pin descriptions and XR5C and XR72 for more details).
180	A3	In	High	
182	A4	In	High	
183	A5	In	High	
185	A6	In	High	
186	A7	In	High	
187	A8	In	High	
188	A9	In	High	
189	A10	In	High	
190	A11	In	High	
191	A12	In	High	
192	A13	In	High	
193	A14	In	High	
194	A15	In	High	
195	A16	In	High	
196	A17 (LA17)	In	High	
197	A18 (LA18)	In	High	
198	A19 (LA19)	In	High	
199	A20 (LA20)	In	High	
200	A21 (LA21)	In	High	
201	A22 (LA22)	In	High	
28	A23 (LA23)	In	High	
29	A24 (ROMCS#) (VOUT)	I/O	High	
30	A25 (IRQ) (MOUT)	I/O	High	
53	A26 (ACTI) (VB0) (GP0)	I/O	High	
54	A27 (ENBKL) (VB1) (GP1)	I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **ISA/CPU Direct/VL-Bus Interface (continued)**

Pin #	Pin Name		Type	Active	Description
51	D00		I/O	High	System Data Bus. In 32-bit CPU Local Bus designs these data lines connect directly to the processor data lines. On the VL-Bus they connect to the corresponding buffered or unbuffered data signal. In ISA bus interfaces, D16-18 become outputs for the Zero Wait State, Memory Chip Select 16, and I/O Chip Select 16 respectively. In ISA bus interfaces D19-31 are unused and should be left disconnected.
50	D01		I/O	High	
49	D02		I/O	High	
48	D03		I/O	High	
47	D04		I/O	High	
46	D05		I/O	High	
45	D06		I/O	High	
44	D07		I/O	High	
41	D08		I/O	High	
40	D09		I/O	High	
38	D10		I/O	High	
37	D11		I/O	High	
36	D12		I/O	High	
35	D13		I/O	High	
34	D14		I/O	High	
33	D15		I/O	High	
20	D16	(ZWS#)	I/O	High	
19	D17	(MCS16#)	I/O	High	
18	D18	(IOCS16#)	I/O	High	
17	D19		I/O	High	
16	D20		I/O	High	
15	D21		I/O	High	
14	D22		I/O	High	
13	D23		I/O	High	
8	D24		I/O	High	
7	D25		I/O	High	
6	D26		I/O	High	
5	D27		I/O	High	
4	D28		I/O	High	
3	D29		I/O	High	
2	D30		I/O	High	
1	D31		I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS

PCI Bus Interface (65545 Only)

Pin #	Pin Name	Type	Active	Description
207	RESET#	In	Low	Reset. This input is used to bring signals and registers in the chip to a consistent state. All outputs from the chip are tri-stated or driven to an inactive state.
201	CLK	In	High	Bus Clock. This input provides the timing reference for all bus transactions. All bus inputs except RESET# and INTA# are sampled on the rising edge of CLK. CLK may be any frequency from DC to 33MHz.
31	PAR	I/O	High	Parity. This signal is used to maintain even parity across AD0-31 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase (i.e., PAR has the same timing as AD0-31 but delayed by one clock). The bus master drives PAR for address and write data phases; the target drives PAR for read data phases.
22	FRAME#	In	Low	Cycle Frame. Driven by the current master to indicate the beginning and duration of an access. Assertion indicates a bus transaction is beginning (while asserted, data transfers continue); de-assertion indicates the transaction is in the final data phase.
23	IRDY#	In	Low	Initiator Ready. Indicates the bus master's ability to complete the current data phase of the transaction. During a write, IRDY# indicates valid data is present on AD0-31; during a read it indicates the master is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted (wait cycles are inserted until this occurs).
24	TRDY#	S/TS	Low	Target Ready. Indicates the target's ability to complete the current data phase of the transaction. During a read, TRDY# indicates that valid data is present on AD0-31; during a write it indicates the target is prepared to accept data. A data phase is completed on any clock when both IRDY# and TRDY# are sampled asserted (wait cycles are inserted until this occurs).
27	STOP#	S/TS	Low	Stop. Indicates the current target is requesting the master to stop the current transaction.
25	DEVSEL#	S/TS	Low	Device Select. Indicates the current target has decoded its address as the target of the current access.

Note: S/TS stands for "Sustained Tri-state". These signals are driven by only one device at a time, are driven high for one clock before being released, and are not driven for at least one cycle after being released by the previous device. A pull-up provided by the bus controller is used to maintain an inactive level between transactions.

PIN DESCRIPTIONS **PCI Bus Interface (65545 Only)**

Pin #	Pin Name		Type	Active	Description
29	PERR#	(VCLKOUT)	S/TS	Low	Parity Error. This signal is for the reporting of data parity errors (except for Special Cycles where SERR# is used). The PERR# pin is Sustained Tri-state and is driven active by the agent receiving the data for two clocks following the data when a data parity error is detected. PERR# will be driven high for one clock before being tri-stated as with all sustained tri-state signals. PERR# will not be reported until the 65545 has claimed the access by asserting DEVSEL# and completing the data phase.
30	SERR#	(MCLKOUT)	OD	Low	System Error. Used to report system errors where the result will be catastrophic (address parity error, data parity errors for Special Cycle commands, etc.). This output is actively driven for a single PCI clock cycle synchronous to CLK and meets the same setup and hold time requirements as all other bused signals. SERR# is not driven high by the 65545 after being asserted; it is pulled high only by a weak pull-up provided by the system, so SERR# on the PCI bus may take two or three clock periods to fully return to an inactive state.
28	Reserved		n/a	n/a	These pins are reserved for future use and should not be connected. All the pins in this group are tri-stated at all times in PCI interface mode.
179-180	Reserved		n/a	n/a	
182-183	Reserved		n/a	n/a	
185-200	Reserved		n/a	n/a	

Note: S/TS stands for "Sustained Tri-state". These signals are driven by only one device at a time, are driven high for one clock before being released, and are not driven for at least one cycle after being released by the previous device. A central pull-up provided by the bus controller is used to maintain an inactive level between transactions.

PIN DESCRIPTIONS

PCI Bus Interface (65545 Only)

Pin #	Pin Name	Type	Active	Description
51	AD00	I/O	High	PCI Address / Data Bus
50	AD01	I/O	High	
49	AD02	I/O	High	Address and data are multiplexed on the same pins. A bus transaction consists of an address phase followed by one or more data phases (both read and write bursts are allowed by the bus definition).
48	AD03	I/O	High	
47	AD04	I/O	High	
46	AD05	I/O	High	
45	AD06	I/O	High	
44	AD07	I/O	High	The address phase is the clock cycle in which FRAME# is asserted (AD0-31 contain a 32-bit physical address). For I/O, the address is a byte address, for memory and configuration, the address is a DWORD address. During data phases AD0-7 contain the LSB and 24-31 contain the MSB. Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks when both IRDY# and TRDY# are asserted.
41	AD08	I/O	High	
40	AD09	I/O	High	
38	AD10	I/O	High	
37	AD11	I/O	High	
36	AD12	I/O	High	
35	AD13	I/O	High	
34	AD14	I/O	High	
33	AD15	I/O	High	
20	AD16	I/O	High	
19	AD17	I/O	High	
18	AD18	I/O	High	
17	AD19	I/O	High	
16	AD20	I/O	High	
15	AD21	I/O	High	
14	AD22	I/O	High	
13	AD23	I/O	High	
8	AD24	I/O	High	
7	AD25	I/O	High	
6	AD26	I/O	High	
5	AD27	I/O	High	
4	AD28	I/O	High	
3	AD29	I/O	High	
2	AD30	I/O	High	
1	AD31	I/O	High	
43	C/BE0#	In	Low	Bus Command / Byte Enables. During the address phase of a bus transaction, these pins define the bus command (see list above). During the data phase, these pins are byte enables that determine which byte lanes carry meaningful data: byte 0 corresponds to AD0-7, byte 1 to 8-15, byte 2 to 16-23, and byte 3 to 24-31.
32	C/BE1#	In	Low	
21	C/BE2#	In	Low	
10	C/BE3#	In	Low	
11	IDSEL	In	High	Initialization Device Select. Used as a chip select during configuration read and write transactions.

C/BE3-0	CommandType	65545
0000	Interrupt Acknowledge	
0001	Special Cycle	
0010	**I/O Read**	✔
0011	**I/O Write**	✔
0100	-reserved-	
0101	-reserved-	
0110	**Memory Read**	✔
0111	**Memory Write**	✔
1000	-reserved-	
1001	-reserved-	
1010	**Configuration Read**	✔
1011	**Configuration Write**	✔
1100	Memory Read Multiple	
1101	Dual Address Cycle	
1110	Memory Read Line	
1111	Memory Read & Invalidate	

PIN DESCRIPTIONS

Display Memory Interface

Pin #	Pin Name			Type	Active	Description
145	AA0	(LB#)	(CFG0)	I/O	High	Address bus for DRAMs A and B.
146	AA1	(ISA#)	(CFG1)	I/O	High	
147	AA2	(2X#)	(CFG2)	I/O	High	Please see the configuration table in the Extended
148	AA3	(Reserved)	(CFG3)	I/O	High	Register description section for complete details on the
149	AA4	(Reserved)	(CFG4)	I/O	High	configuration options (XR01 and XR6C).
150	AA5	(OS#)	(CFG5)	I/O	High	
151	AA6	(AD#)	(CFG6)	I/O	High	
152	AA7	(TS#)	(CFG7)	I/O	High	
153	AA8	(LV#)	(CFG8)	I/O	High	
154	AA9	(32KHz)	(VR0)	I/O	High	AA9, alternately, becomes clock input for refresh of non-self-refresh DRAMs and panel power sequencing or video input red lsb.
90	CA0		(P16)	Out	High	Address bus for DRAM C.
91	CA1		(P17)	Out	High	
92	CA2		(P18)	Out	High	
93	CA3		(P19)	Out	High	
94	CA4		(P20)	Out	High	
95	CA5		(P21)	Out	High	
96	CA6		(P22)	Out	High	
97	CA7		(P23)	Out	High	
98	CA8		(VG1)	I/O	High	
99	CA9		(VG0)	I/O	High	
156	RASA#			Out	Low	Row address strobe for DRAM A
123	RASB#			Out	Low	Row address strobe for DRAM B
101	RASC#			Out	Low	Row address strobe for DRAM C
			(KEY)	In	High	or color key input from external video source
160	CASAL#	(WEAL#)		Out	Low	Column address strobe for the DRAM A lower byte
159	CASAH#	(CASA#)		Out	Low	Column address strobe for the DRAM A upper byte
126	CASBL#	(WEBL#)		Out	Low	Column address strobe for the DRAM B lower byte
125	CASBH#	(CASB#)		Out	Low	Column address strobe for the DRAM B upper byte
104	CASCL#	(WECL#)	(VR6)	I/O	Both	CAS for the DRAM C lower byte or video in red bit-6
103	CASCH#	(CASC#)	(VR7)	I/O	Both	CAS for the DRAM C upper byte or video in red bit-7
157	WEA#	(WEAH#)		Out	Low	Write enable for DRAM A
124	WEB#	(WEBH#)		Out	Low	Write enable for DRAM B
102	WEC#	(WECH#)	(PCLK)	Out	Both	Write enable for DRAM C or video in port PCLK out
155	OEAB#			Out	Low	Output enable for DRAMs A and B
100	OEC#		(VR1)	I/O	Both	Output enable for DRAM C or video in red bit-1

Note: Pin names in parentheses (...) indicate alternate functions

PIN DESCRIPTIONS **Display Memory Interface (continued)**

Pin #	Pin Name		Type	Active	Description
162	MAD0	(TSENA#)	I/O	High	Memory data bus for DRAM A (lower 512KB of display memory)
163	MAD1	(ICTENA#)	I/O	High	
164	MAD2		I/O	High	
165	MAD3		I/O	High	
166	MAD4		I/O	High	
167	MAD5		I/O	High	
168	MAD6		I/O	High	
169	MAD7		I/O	High	
170	MAD8		I/O	High	
171	MAD9		I/O	High	
172	MAD10		I/O	High	
173	MAD11		I/O	High	
174	MAD12		I/O	High	
175	MAD13		I/O	High	
176	MAD14		I/O	High	
177	MAD15		I/O	High	
127	MBD0		I/O	High	Memory data bus for DRAM B (upper 512KB)
128	MBD1		I/O	High	
129	MBD2		I/O	High	
130	MBD3		I/O	High	
131	MBD4		I/O	High	
132	MBD5		I/O	High	
133	MBD6		I/O	High	
134	MBD7		I/O	High	
135	MBD8		I/O	High	
136	MBD9		I/O	High	
137	MBD10		I/O	High	
138	MBD11		I/O	High	
140	MBD12		I/O	High	
141	MBD13		I/O	High	
143	MBD14		I/O	High	
144	MBD15		I/O	High	
106	MCD0	(VB2)	I/O	High	Memory data bus for DRAM C (Frame Buffer) When a frame buffer DRAM is not required, this bus may optionally be used to input up to 24 bits of RGB data from an external PC-Video subsystem. For the remaining pins of the 24-bit video input port see the pin descriptions of DRAM C address, DRAM C control, AA9, ACTI, and ENABKL. Note that this configuration also provides for additional panel outputs so that a full 24-bit video input port may be implemented along with a 24-bit true-color TFT panel (TFT panels never need DRAM C).
107	MCD1	(VB3)	I/O	High	
109	MCD2	(VB4)	I/O	High	
110	MCD3	(VB5)	I/O	High	
111	MCD4	(VB6)	I/O	High	
112	MCD5	(VB7)	I/O	High	
113	MCD6	(VG2)	I/O	High	
114	MCD7	(VG3)	I/O	High	
115	MCD8	(VG4)	I/O	High	
116	MCD9	(VG5)	I/O	High	
117	MCD10	(VG6)	I/O	High	
118	MCD11	(VG7)	I/O	High	
119	MCD12	(VR2)	I/O	High	
120	MCD13	(VR3)	I/O	High	
121	MCD14	(VR4)	I/O	High	
122	MCD15	(VR5)	I/O	High	

Note: Pin names in parentheses (...) indicate alternate functions.

Note: If ICTENA# is low with RESET# low, a rising edge on XTALI will put the chip into 'In Circuit Test' mode. In ICT mode, all digital signal pins become inputs which are part of a long path starting at ENAVDD (pin 62) and proceeding to lower pin numbers around the chip to pin 1 then to pin 208 and ending at VSYNC (pin 64). If all pins in the path are high, the VSYNC output will be high. If any pin is low, the VSYNC output will be low. Thus the chip can be checked in circuit to determine if all pins are connected properly by toggling all pins one at a time and observing the effect on VSYNC. XTALI must be toggled last because rising edges on XTALI with ICTENA# high or RESET# high will exit ICT mode. As a side effect, ICT mode effectively 3-states all pins except VSYNC. If TSENA# is low with RESET # low, a rising edge on XTALI will 3-state all pins. An XTALI rising edge without the enabling conditions exits 3-state.

PIN DESCRIPTIONS — Flat Panel Display Interface

Pin #	Pin Name	Type	Active	Description
71	P0	Out	High	8, 9, 12, or 16-bit flat panel data output. 18-bit and 24-bit panel interfaces may also be supported (see CA0-7 for P16-23). Refer to the table below for configurations for various panel types.
72	P1	Out	High	
73	P2	Out	High	
74	P3	Out	High	
75	P4	Out	High	
76	P5	Out	High	
78	P6	Out	High	
79	P7	Out	High	
81	P8 (SHFCLKU)	Out	High	
82	P9	Out	High	
83	P10	Out	High	
84	P11	Out	High	
85	P12	Out	High	
86	P13	Out	High	
87	P14	Out	High	
88	P15	Out	High	
70	SHFCLK (CL2) (SHFCLKL)	Out	High	Shift Clock. Pixel clock for flat panel data.
67	FLM	Out	High	First Line Marker. Flat Panel equivalent of VSYNC.
68	LP (CL1) (DE) (BLANK#)	Out	High	Latch Pulse. Flat Panel equivalent of HSYNC.
69	M (DE) (BLANK#)	Out	High	M signal for panel AC drive control (may also be called ACDCLK). May also be configured as BLANK# or as Display Enable (DE) for TFT Panels (see XR4F bit-6).
62	ENAVDD	Out	High	Power sequencing controls for panel driver electronics voltage V_{DD} and panel LCD bias voltage V_{EE}
61	ENAVEE (ENABKL)	Out	High	
53	ACTI (GP0)(VB0)(A26)	I/O	High	Activity Indicator and Enable Backlight outputs. May be configured for other functions (see Extension Registers XR5C and XR72 and pin descriptions of MCD0-15 and A26/A27 for more information).
54	ENABKL (GP1)(VB1)(A27)	I/O	High	

6554x Pin#	6554x PinName	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/16-bit	Color TFT 18/24-bit	Color TFT HR 18/24-bit	Color STN SS 8-bit(X4bP)	Color STN SS 16-bit(4bP)	Color STN DD 8-bit(4bP)	Color STN DD 16-bit(4bP)
71	P0	–	UD3	UD7	B0	B0	B00	R1...	R1...	UR1...	UR0...
72	P1	–	UD2	UD6	B1	B1	B01	B1...	G1...	UG1...	UG0...
73	P2	–	UD1	UD5	B2	B2	B02	G2...	B1...	UB1...	UB0...
74	P3	–	UD0	UD4	B3	B3	B03	R3...	R2...	UR2...	UR1...
75	P4	–	LD3	UD3	B4	B4	B10	B3...	G2...	LR1...	LR0...
76	P5	–	LD2	UD2	G0	B5	B11	G4...	B2...	LG1...	LG0...
78	P6	–	LD1	UD1	G1	B6	B12	R5...	R3...	LB1...	LB0...
79	P7	–	LD0	UD0	G2	B7	B13	B5...	G3...	LR2...	LR1...
81	P8	P0	–	LD7	G3	G0	G00	**SHFCLKU**	B3...	–	UG1...
82	P9	P1	–	LD6	G4	G1	G01	–	R4...	–	UB1...
83	P10	P2	–	LD5	G5	G2	G02	–	G4...	–	UR2...
84	P11	P3	–	LD4	R0	G3	G03	–	B4...	–	UG2...
85	P12	P4	–	LD3	R1	G4	G10	–	R5...	–	LG1...
86	P13	P5	–	LD2	R2	G5	G11	–	G5...	–	LB1...
87	P14	P6	–	LD1	R3	G6	G12	–	B5...	–	LR2...
88	P15	P7	–	LD0	R4	G7	G13	–	R6...	–	LG2...
90	P16	–	–	–	–	R0	R00	–	–	–	–
91	P17	–	–	–	–	R1	R01	–	–	–	–
92	P18	–	–	–	–	R2	R02	–	–	–	–
93	P19	–	–	–	–	R3	R03	–	–	–	–
94	P20	–	–	–	–	R4	R10	–	–	–	–
95	P21	–	–	–	–	R5	R11	–	–	–	–
96	P22	–	–	–	–	R6	R12	–	–	–	–
97	P23	–	–	–	–	R7	R13	–	–	–	–
70	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	**SHFCLKL**	SHFCLK	SHFCLK	SHFCLK
Pixels / Clock:		**8**	**8**	**16**	**1**	**1**	**2**	**2-2/3**	**5-1/3**	**2-2/3**	**5-1/3**

PINDESCRIPTIONS **CRT and Clock Interface**

Pin #	Pin Name		Type	Active	Description
65	HSYNC		Out	Both	CRT Horizontal Sync (polarity is programmable)
64	VSYNC		Out	Both	CRT Vertical Sync (polarity is programmable)
60 58 57	RED GREEN BLUE		Out Out Out	High High High	CRT analog video outputs from the internal color palette DAC.
55	RSET		In	n/a	Set point resistor for the internal color palette DAC. A 270Ω 1% resistor is required between RSET and AGND.
59 56	AVCC AGND		VCC GND	-- --	Analog power and ground pins for noise isolation for the internal color palette DAC. AVCC should be isolated from digital VCC as described in the Functional Description of the internal color palette DAC. AGND should be common with digital ground but must be tightly decoupled to AVCC. See the Functional Description of the internal color palette DAC for further information.
203	XTALI	(MCLK)	I/O	High	Crystal In. When the internal clock synthesizer is used, this pin serves as either the series resonant crystal input or as the input for an external reference oscillator (usually 14.31818 MHz). Note that in test mode for the internal clock synthesizer, MCLK is output on A25 (pin 30) and VCLK is output on A24 (pin 29).
204	XTALO		Out	High	Crystal Out. When the internal oscillator is used, this pin serves as the series resonant crystal output. When an external oscillator is used, this pin must be left disconnected.
205 202 206 208	CVCC0 CGND0 CVCC1 CGND1		VCC GND VCC GND	-- -- -- --	Analog power and ground pins for noise isolation for the internal clock synthesizer. Must be the same as VCC for internal logic. VCC/GND pair 0 and VCC/GND pair 1 pins must be carefully decoupled individually. Refer also to the section on clock ground layout in the Functional Description. Note that the CVCC voltage must be the same as the voltage for the internal logic (IVCC).

Note: Pin names in parentheses (...) indicate alternate functions

CRT/Panel Output Signal Status During Standby Mode

6554x Pin #	Signal Name	Signal Status	Signal Polarity
67	FLM	ForcedLow	XR54 bit 7
68	LP	ForcedLow	XR54 bit 6
70	SHFCLK	ForcedLow	N/A
69	M	ForcedLow	N/A
71	P0	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
72	P1	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
73	P2	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
74	P3	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
75	P4	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
76	P5	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
78	P6	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
79	P7	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
81	P8	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
82	P9	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
83	P10	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
84	P11	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
85	P12	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
86	P13	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
87	P14	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
88	P15	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
90	P16/CA0	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
91	P17/CA1	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
92	P18/CA2	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
93	P19/CA3	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
94	P20/CA4	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
95	P21/CA5	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
96	P22/CA6	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
97	P23/CA7	ForcedLow	XR61 bit 7 (text); XR63 bit 7 (graphics)
62	ENAVDD	ForcedLow	N/A
61	ENAVEE	ForcedLow	N/A
54	ENABKL/A27	ForcedLow	N/A
65	HSYNC	ForcedLow	N/A
64	VSYNC	ForcedLow	N/A
53	ACTI/A26	ForcedLow	N/A
60,58,57	R,G,B	ForcedLow	N/A

Display Memory Output Signal Status During Standby Mode

6554x Pin #	Signal Name	Signal Status
156	RASA#	Driven Low
123	RASB#	Driven Low
101	RASC#	Driven Low (see note 1)
157	WEA#	Driven High
124	WEB#	Driven High
102	WEC#	Driven High (see note 1)
160	CASAL#	Driven Low
159	CASAH#	Driven Low
126	CASBL#	Driven Low
125	CASBH#	Driven Low
104	CASCL#	Driven Low (see note 1)
103	CASCH#	Driven Low (see note 1)
155	OEAB#	Driven High
100	OEC#	Driven High (see note 1)
154-145	AA9-0	Pulled low with weak resistor
99-90	CA9-0	Driven Low
177-162	MAD15-0	Pulled low with weak resistor
144-143,141-140,138-127	MBD15-0	Pulled low with weak resistor
122-109,107-66	MCD15-0	Pulled low with weak resistor (see note 1)

Notes:
1 These pins are inputs when using the video input port. These pins are driven as outputs when using a frame buffer DRAM.

PIN DESCRIPTIONS **Power / Ground and Standby Control**

Pin #	Pin Name	Type	Active	Description
178	STNDBY#	In	Low	Standby Control Pin. Pulling this pin to ground places the 65540 / 545 in Standby Mode.
80	IVCC	Vcc	–	Power / Ground (Internal Logic). 5V±10% or 3.3V ±0.3V. Note that this voltage must be the same as CVCC (voltage for internal clock synthesizer).
77	IGND	Gnd	–	
181	IVCC	Vcc	–	
184	IGND	Gnd	–	
9	BVCC	Vcc	–	Power / Ground (Bus Interface). 5V±10% or 3.3V ±0.3V.
12	BGND	Gnd	–	
26	BGND	Gnd	–	
42	BVCC	Vcc	–	
39	BGND	Gnd	–	
52	BGND	Gnd	–	
66	DVCC	Vcc	–	Power / Ground (Display Interface). 5V±10% or 3.3V ±0.3V.
63	DGND	Gnd	–	
89	DGND	Gnd	–	
158	MVCCA	Vcc	–	Power / Ground (Memory Interface A). 5V±10% or 3.3V ±0.3V.
161	MGNDA	Gnd	–	
142	MVCCB	Vcc	–	Power / Ground (Memory Interface B). 5V±10% or 3.3V ±0.3V.
139	MGNDB	Gnd	–	
108	MVCCC	Vcc	–	Power / Ground (Memory Interface C). 5V±10% or 3.3V ±0.3V.
105	MGNDC	Gnd	–	

Bus/ClockOutputSignalStatusDuringStandbyMode

		Signal Status	
6554x Pin #	**SignalName**	**VL-Bus**	**ISA Bus**
204	XTALO	Driven (see note 1)	Driven (see note 1)
29	ROMCS# / A24	N/A	Driven High
30	IRQ / A25	N/A	Tri-Stated
53	ACTI / A26	(see previous page)	N/A
54	ENABKL / A27	(see previous page)	N/A
24	LRDY# / RDY	Tri-Stated	Tri-Stated
25	LDEV#	Driven High	N/A
51-44, 41-40,38-33	D0-15	Tri-Stated	Tri-Stated
20	D16 / ZWS#	Tri-Stated	Tri-Stated
19	D17 / MCS16#	Tri-Stated	Tri-Stated
18	D18 / IOCS16#	Tri-Stated	Tri-Stated
17-13, 8-1	D19-31	Tri-Stated	Tri-Stated

Notes:
1 The XTALO pin will always be driven except when XR33 bit-2 is set to '1'.

I/O Map

Port Address	Read	Write
102	Global Enable (ISA Bus Only)	Global Enable (ISA Bus Only)
3B0	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B1	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B2	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B3	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B4	CRTC Index	CRTC Index
3B5	CRTC Data	CRTC Data
3B6	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B7	Reserved for MDA/Hercules	Reserved for MDA/Hercules
3B8	Hercules Mode Register (MODE)	Hercules Mode Register (MODE)
3B9	--	Set Light Pen FF (ignored)
3BA	Status Register (STAT)	Feature Control Register (FCR)
3BB	--	Clear Light Pen FF (ignored)
3BC		
3BD	Reserved for system parallel port	
3BE		
3BF	Hercules Configuration Register (HCFG)	Hercules Configuration Register (HCFG)
3C0	Attribute Controller Index / Data	Attribute Controller Index / Data
3C1	Attribute Controller Index / Data	Attribute Controller Index / Data
3C2	Feature Read Register (FEAT)	Miscellaneous Output Register (MSR)
3C3	Video Subsystem Enable (VSE)(LB Only)	Video Subsystem Enable (VSE)(LB Only)
3C4	Sequencer Index	Sequencer Index
3C5	Sequencer Data	Sequencer Data
3C6	Color Palette Mask	Color Palette Mask
3C7	Color Palette State	Color Palette Read Mode Index
3C8	Color Palette Write Mode Index	Color Palette Write Mode Index
3C9	Color Palette Data	Color Palette Data
3CA	Feature Control Register (FCR)	--
3CB	--	--
3CC	Miscellaneous Output Register (MSR)	--
3CD	--	--
3CE	Graphics Controller Index	Graphics Controller Index
3CF	Graphics Controller Data	Graphics Controller Data
n3D0†	32-Bit DR Register Extensions (65545 only)	32-Bit DR Register Extensions (65545 only)
n3D1†	32-Bit DR Register Extensions (65545 only)	32-Bit DR Register Extensions (65545 only)
n3D2†	32-Bit DR Register Extensions (65545 only)	32-Bit DR Register Extensions (65545 only)
n3D3†	32-Bit DR Register Extensions (65545 only)	32-Bit DR Register Extensions (65545 only)
03D4	CRTC Index	CRTC Index
03D5	CRTC Data	CRTC Data
03D6	CHIPS™ Extensions Index	CHIPS™ Extensions Index
03D7	CHIPS™ Extensions Data	CHIPS™ Extensions Data
03D8	CGA Mode Register (MODE)	CGA Mode Register (MODE)
03D9	CGA Color Register (COLOR)	CGA Color Register (COLOR)
03DA	Status Register (STAT)	Feature Control Register (FCR)
03DB	--	Clear Light Pen FF (ignored)
03DC	--	Set Light Pen FF (ignored)
46E8	--	Setup Control (ISA Bus Only)

Mono Mode

Color Mode

† 32-Bit register addresses are of the form 'bnnn nn1b bbbb bb00' where 'bbbbbbbb' is specified by I/O base register XR07 and 'nnnnn' specifies 1 of 32 DRxx 32-bit registers

REGISTER SUMMARY - CGA, MDA, AND HERCULES MODEs

Register	Register Name	Bits	Access	I/O Port - MDA/Herc	I/O Port - CGA	Comment
ST00 (STAT)	Display Status	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	ref only: no light pen
MODE	CGA/MDA/Hercules Mode Control	7	R/W	3B8	3D8	
COLOR	CGA Color Select	6	R/W	n/a	3D9	R/W at XR7E also
HCFG	Hercules Configuration	2	W	3BF	n/a	
			R	3D6-3D7 index 14	n/a	XR14
RX, R0-11	'6845' Registers	0-8	R/W	3B4-3B5	3D4-3D5	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - EGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
MSR	Miscellaneous Output	7	W	3C2	3C2	
FCR	Feature Control	3	W	3BA	3DA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	7	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	ref only: no light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	ref only: no light pen
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	

REGISTER SUMMARY - VGA MODE

Register	Register Name	Bits	Access	I/O Port - Mono	I/O Port - Color	Comment
VSE	Video Subsystem Enable	1	W	3C3 if LB	3C3 if LB	Disabled by XR70 bit-7
SETUP	Setup Control	2	W	46E8 if ISA	46E8 if ISA	Disabled by XR70 bit-7
ENABLE	Global Enable	1	R/W	102 if ISA	102 if ISA	Setup Only in ISA Bus
PR0-17	PCI Configuration	8, 16, 32	R/W	System Dependent	System Dependent	PCI Bus Only
MSR	Miscellaneous Output	7	W	3C2	3C2	
			R	3CC	3CC	
FCR	Feature Control	3	W	3BA	3DA	
			R	3CA	3CA	
ST00 (FEAT)	Feature Read (Input Status 0)	4	R	3C2	3C2	
ST01 (STAT)	Display Status (Input Status 1)	6	R	3BA	3DA	
CLPEN	Clear Light Pen Flip Flop	0	W(n/a)	3BB(ignored)	3DB(ignored)	Ref only: No light pen
SLPEN	Set Light Pen Flip Flop	0	W(n/a)	3B9(ignored)	3DC(ignored)	Ref only: No light pen
DACMASK	Color Palette Pixel Mask	8	R/W	3C6	3C6	
DACSTATE	Color Palette State	2	R	3C7	3C7	
DACRX	Color Palette Read-Mode Index	8	W	3C7	3C7	
DACWX	Color Palette Write-Mode Index	8	R/W	3C8	3C8	
DACDATA	Color Palette Data 0-FF	3x6	R/W	3C9	3C9	
SRX, SR0-7	Sequencer	0-8	R/W	3C4-3C5	3C4-3C5	
CRX, CR0-3F	CRT Controller	0-8	R/W	3B4-3B5	3D4-3D5	
GRX, GR0-8	Graphics Controller	0-8	R/W	3CE-3CF	3CE-3CF	
ARX, AR0-14	Attributes Controller	0-8	R/W	3C0-3C1	3C0-3C1	
XRX, XR0-7F	Extension Registers	0-8	R/W	3D6-3D7	3D6-3D7	
DR00-DR0C	32-Bit Extension Registers	32	R/W	n3D0-n3D3	n3D0-n3D3	Programmable I/O address

REGISTER SUMMARY - INDEXED REGISTERS (VGA)

Register	Register Name	Bits	Register Type	Access (VGA)	Access (EGA)	I/O Port
SRX	Sequencer Index	3	VGA/EGA	R/W	R/W	3C4
SR0	Reset	2	VGA/EGA	R/W	R/W	3C5
SR1	Clocking Mode	6	VGA/EGA	R/W	R/W	3C5
SR2	Plane Mask	4	VGA/EGA	R/W	R/W	3C5
SR3	Character Map Select	6	VGA/EGA	R/W	R/W	3C5
SR4	Memory Mode	3	VGA/EGA	R/W	R/W	3C5
SR7	Reset Horizontal Character Counter	0	VGA	W	n/a	3C5
CRX	CRTC Index	6	VGA/EGA	R/W	R/W	3B4 Mono, 3D4 Color
CR0	Horizontal Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR1	Horizontal Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR2	Horizontal Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR3	Horizontal Blanking End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR4	Horizontal Retrace Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR5	Horizontal Retrace End	5+2+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR6	Vertical Total	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR7	Overflow	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR8	Preset Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR9	Character Cell Height	5+3	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRA	Cursor Start	5+1	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRB	Cursor End	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRC	Start Address High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRD	Start Address Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRE	Cursor Location High	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CRF	Cursor Location Low	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
LPENH	Light Pen High	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
LPENL	Light Pen Low	8	VGA/EGA	R	R	3B5 Mono, 3D5 Color
CR10	Vertical Retrace Start	8	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR11	Vertical Retrace End	4+4	VGA/EGA	R/W	W	3B5 Mono, 3D5 Color
CR12	Vertical Display End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR13	Offset	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR14	Underline Row Scan	5+2	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR15	Vertical Blanking Start	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR16	Vertical Blanking End	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR17	CRT Mode Control	7	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR18	Line Compare	8	VGA/EGA	R/W	R/W	3B5 Mono, 3D5 Color
CR22	Graphics Controller Data Latches	8	VGA	R	n/a	3B5 Mono, 3D5 Color
CR24	Attribute Controller Index/Data Latch	1	VGA	R	n/a	3B5 Mono, 3D5 Color
GRX	Graphics Controller Index	4	VGA/EGA	R/W	R/W	3CE
GR0	Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR1	Enable Set/Reset	4	VGA/EGA	R/W	R/W	3CF
GR2	Color Compare	4	VGA/EGA	R/W	R/W	3CF
GR3	Data Rotate	5	VGA/EGA	R/W	R/W	3CF
GR4	Read Map Select	2	VGA/EGA	R/W	R/W	3CF
GR5	Mode	6	VGA/EGA	R/W	R/W	3CF
GR6	Miscellaneous	4	VGA/EGA	R/W	R/W	3CF
GR7	Color Don't Care	4	VGA/EGA	R/W	R/W	3CF
GR8	Bit Mask	8	VGA/EGA	R/W	R/W	3CF
ARX	Attribute Controller Index	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR0-F	Internal Palette Regs 0-15	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR10	Mode Control	7	VGA/EGA	R/W	R/W	3C0 (3C1)
AR11	Overscan Color	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR12	Color Plane Enable	6	VGA/EGA	R/W	R/W	3C0 (3C1)
AR13	Horizontal Pixel Panning	4	VGA/EGA	R/W	R/W	3C0 (3C1)
AR14	Color Select	4	VGA	R/W	n/a	3C0 (3C1)

EXTENSION REGISTER SUMMARY: 00-2F

Reg	Register Name	Bits	Access	Port	Reset	CHIPS' VGA Product Family				
						82C450	64300/310	65510	65530	65535
XRX	**Extension Index Register**	7	R/W	3D6	- x x x x x x x	✓	✓	✓	✓	✓
XR00	**Chip Version (65540: v=0; 65545: v=1)**	8	R/O	3D7	1 1 0 1 v r r r	✓	✓	✓	✓	✓
XR01	**Configuration**	8	R/O	3D7	d d d d d d d d	✓	✓	✓	✓	✓
XR02	**CPU Interface Control 1**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓
XR03	**CPU Interface Control 2** *(ROM Intfc)*	2	R/W	3D7	- - - - - - 0 x	.	✓	.	.	.
XR04	**Memory Control 1**	4	R/W	3D7	- - 0 - - 0 0 0	✓	✓	✓	✓	✓
XR05	**Memory Control 2** *(Clock Control)*	8	R/W	3D7	0 0 0 0 0 0 0 0	.	✓	.	.	✓
XR06	**Palette Control** *(DRAM Intfc)*	8	R/W	3D7	0 0 0 0 0 0 0 0	.	✓	✓	✓	✓
XR07	**I/O Base (65545 Only)**	8	R/W	3D7	1 1 1 1 0 1 0 0	.	✓	.	.	.
XR08	**Linear Addressing Base** *(Linear Base L)*	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR09	-reserved- *(Linear Base H)*	--	--	3D7		.	✓	.	.	.
XR0A	-reserved- *(XRAM Mode)*	--	--	3D7		.	✓	.	.	.
XR0B	**CPU Paging**	5	R/W	3D7	- - 0 0 • 0 0 0	✓	✓	✓	✓	✓
XR0C	**Start Address Top**	2	R/W	3D7	- - - - - - x x	✓	✓	✓	✓	✓
XR0D	**Auxiliary Offset**	2	R/W	3D7	- - - - - - 0 0	✓	✓	✓	✓	✓
XR0E	**Text Mode Control**	6	R/W	3D7	0 0 0 0 0 0 - -	✓	✓	✓	✓	✓
XR0F	**Software Flags 0**	8	R/W	3D7	x x x x x x x x	.	✓	✓	✓	✓
XR10	**Single/Low Map**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR11	**High Map**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR12	-reserved-	--	--	3D7		.	.	.	.	.
XR13	-reserved-	--	--	3D7		.	.	.	.	.
XR14	**Emulation Mode**	8	R/W	3D7	0 0 0 0 h h 0 0	✓	✓	✓	✓	✓
XR15	**Write Protect**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓
XR16	**Vertical Overflow**	5	R/W	3D7	• 0 • 0 • 0 0 0	.	✓	.	.	✓
XR17	**Horizontal Overflow**	7	R/W	3D7	• 0 0 0 0 0 0 0	.	✓	.	.	✓
XR18	**Alternate H Disp End**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR19	**Alternate H Sync Start** *(Half-line)*	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1A	**Alternate H Sync End**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1B	**Alternate H Total**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1C	**Alternate Blank Start / H Panel Size**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1D	**Alternate H Blank End**	8	R/W	3D7	0 x x x x x x x	✓	✓	✓	✓	✓
XR1E	**Alternate Offset**	8	R/W	3D7	x x x x x x x x	✓	✓	✓	✓	✓
XR1F	**Virtual EGA Switch Register**	5	R/W	3D7	0 - - - x x x x	✓	✓	✓	✓	✓
XR20	-reserved-	--	--	3D7		.	.	.	.	.
XR21	-reserved-	--	--	3D7		.	.	.	✓	.
XR22	-reserved-	--	--	3D7		.	.	.	✓	.
XR23	-reserved-	--	--	3D7		.	.	.	✓	.
XR24	**FP Alt Max Scanline**	5	R/W	3D7	• • • x x x x x	.	.	✓	✓	✓
XR25	**FP Alt Txt H Virt Panel Size**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓
XR26	**Alt H Sync Start**	8	R/W	3D7	x x x x x x x x	.	.	.	.	✓
XR27	-reserved-	--	--	3D7		.	.	.	.	.
XR28	**Video Interface**	5	R/W	3D7	0 0 0 0 - - 0 -	✓	✓	✓	✓	✓
XR29	**Half Line Compare**	8	R/W	3D7	x x x x x x x x	.	.	.	.	.
XR2A	-reserved-	--	--	3D7		.	.	.	.	.
XR2B	**Software Flags 1**	8	R/W	3D7	0 0 0 0 0 0 0 0	✓	✓	✓	✓	✓
XR2C	**FLM Delay**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR2D	**LP Delay**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR2E	**LP Delay**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓
XR2F	**LP Width**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓

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h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0/1 by trailing edge of reset

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 30-5F

Reg	Register Name	Bits	Access	Port	Reset	CHIPS' VGA Product Family				
						82C450	64300/310	65510	65530	65535
XR30	**Clock Divide Control**	4	R/W	3D7	• • • • x x x x	.	✓	.	.	✓
XR31	**Clock M-Divisor**	7	R/W	3D7	• x x x x x x x	.	✓	.	.	✓
XR32	**Clock N-Divisor**	7	R/W	3D7	• x x x x x x x	.	✓	.	.	✓
XR33	**Clock Control**	7	R/W	3D7	0 0 0 0 • 0 0 0	.	✓	.	.	✓
XR34	-reserved-	--	--	3D7		.	.	.	.	.
XR35	-reserved-	--	--	3D7		.	.	.	.	.
XR36	-reserved-	--	--	3D7		.	.	.	.	.
XR37	-reserved-	--	--	3D7		.	.	.	.	.
XR38	-reserved-	--	--	3D7		.	.	.	.	.
XR39	-reserved-	--	--	3D7		.	.	.	.	.
XR3A	**Color Key 0**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR3B	**Color Key 1**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR3C	**Color Key 2**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR3D	**Color Key Mask 0**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR3E	**Color Key Mask 1**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR3F	**Color Key Mask 2**	8	R/W	3D7	x x x x x x x x	.	✓	.	.	✓
XR40	**BitBLT Configuration (65545 Only)**	2	R/W	3D7	- - - - - - x x	.	✓	.	.	.
XR41	-reserved-	--	--	3D7		.	.	.	.	.
XR42	-reserved-	--	--	3D7		.	.	.	.	.
XR43	-reserved-	--	--	3D7		.	.	.	.	.
XR44	**Software Flag Register 2**	8	R/W	3D7	x x x x x x x x	.	✓	✓	✓	✓
XR45	**Software Flag Register 3**	8	R/W	3D7	x x x x x x x x	.	.	.	.	✓
XR46	-reserved-	--	--	3D7		.	.	.	.	.
XR47	-reserved-	--	--	3D7		.	.	.	.	.
XR48	-reserved-	--	--	3D7		.	.	.	.	.
XR49	-reserved-	--	--	3D7		.	.	.	.	.
XR4A	-reserved-	--	--	3D7		.	.	.	.	.
XR4B	-reserved-	--	--	3D7		.	.	.	.	.
XR4C	-reserved-	--	--	3D7		.	.	.	.	.
XR4D	-reserved-	--	--	3D7		.	.	.	.	.
XR4E	-reserved-	--	--	3D7		.	.	.	.	.
XR4F	**Panel Format 2**	5	R/W	3D7	x x • • • x x x	.	.	.	.	✓
XR50	**Panel Format 1**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR51	**Display Type**	7	R/W	3D7	0 0 0 • 0 0 0 0	.	.	✓	✓	✓
XR52	**Power Down Control**	8	R/W	3D7	0 0 0 0 0 0 0 1	.	✓	✓	✓	✓
XR53	**Panel Format 3**	7	R/W	3D7	• 0 0 0 0 0 x 0	.	.	✓	✓	✓
XR54	**Panel Interface**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR55	**H Compensation**	6	R/W	3D7	x x x x • • x x	.	.	✓	✓	✓
XR56	**H Centering**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR57	**V Compensation**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR58	**V Centering**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR59	**V Line Insertion**	7	R/W	3D7	x x x • x x x x	.	.	✓	✓	✓
XR5A	**V Line Replication**	4	R/W	3D7	• • • • x x x x	.	.	✓	✓	✓
XR5B	**Power Sequencing Delay**	8	R/W	3D7	1 0 0 0 0 0 0 1	.	.	✓	✓	✓
XR5C	**Activity Indicator Control**	7	R/W	3D7	0 x • x x x x x	.	.	.	.	✓
XR5D	**FP Diagnostic**	8	R/W	3D7	0 0 0 0 0 0 0 0	.	.	.	.	✓
XR5E	**ACDCLK (M) Control**	8	R/W	3D7	x x x x x x x x	.	.	✓	✓	✓
XR5F	**Power Down Mode Refresh**	8	R/W	3D7	x x x x x x x x	.	.	.	✓	✓

Reset Codes: x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding data bus pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0/1 by trailing edge of reset

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

EXTENSION REGISTER SUMMARY: 60-7F

Reg	Register Name	Bits	Access	Port	Reset	CHIPS' VGA Product Family				
						82C450	64300/310	65510	65530	65535
XR60	**Blink Rate Control**	8	R/W	3D7	10000011	.	✓	✓	✓	✓
XR61	**SmartMap™ Control**	8	R/W	3D7	xxxxxxxx	.	.	✓	✓	✓
XR62	**SmartMap™ Shift Parameter**	8	R/W	3D7	xxxxxxxx	.	.	✓	✓	✓
XR63	**SmartMap™ Color Mapping Control**	8	R/W	3D7	x1xxxxxx	.	.	✓	✓	✓
XR64	**FP Alternate Vertical Total**	8	R/W	3D7	xxxxxxxx	.	.	✓	✓	✓
XR65	**FP Alternate Overflow**	6	R/W	3D7	xxx••xxx	.	.	✓	✓	✓
XR66	**FP Alternate Vertical Sync Start**	8	R/W	3D7	xxxxxxxx	.	.	✓	✓	✓
XR67	**FP Alternate Vertical Sync End**	4	R/W	3D7	••••xxxx	.	.	✓	✓	✓
XR68	**FP Vertical Panel Size**	8	R/W	3D7	xxxxxxxx	.	.	✓	✓	✓
XR69	-reserved-	--	--	3D7		.	.	.	.	.
XR6A	-reserved-	--	--	3D7		.	.	.	.	.
XR6B	-reserved-	--	--	3D7		.	.	.	.	.
XR6C	**Programmable Output Drive**	5	R/W	3D7	••0000d•	.	.	✓	✓	✓
XR6D	-reserved-	--	--	3D7		.	.	.	.	.
XR6E	**Polynomial FRC Control**	8	R/W	3D7	10111101	.	.	✓	✓	✓
XR6F	**Frame Buffer Control**	8	R/W	3D7	00000000	.	.	.	✓	✓
XR70	**Setup / Disable Control**	1	R/W	3D7	0-------	✓	✓	✓	✓	✓
XR71	-reserved- *(GPIO Control)*	--	--	3D7		.	✓	.	.	.
XR72	**External Device I/O** *(GPIO Data)*	7	R/W	3D7	0000000•	.	✓	.	.	✓
XR73	**Miscellaneous Control**	6	R/W	3D7	00--0000	.	✓	.	.	✓
XR74	-reserved- *(Configuration 2)*	--	--	3D7		.	✓	.	.	.
XR75	-reserved- *(Software Flags 3)*	--	--	3D7		.	✓	.	.	.
XR76	-reserved-	--	--	3D7		.	.	.	.	.
XR77	-reserved-	--	--	3D7		.	.	.	.	.
XR78	-reserved-	--	--	3D7		.	.	.	.	.
XR79	-reserved-	--	--	3D7		.	.	.	.	.
XR7A	-reserved-	--	--	3D7		.	.	.	.	.
XR7B	-reserved-	--	--	3D7		.	.	.	.	.
XR7C	-reserved-	--	--	3D7		.	.	.	.	.
XR7D	**Diagnostic**	1	R/W	3D7	0------•	.	.	✓	✓	.
XR7E	**CGA/Hercules Color Select**	6	R/W	3D7	--xxxxxx	✓	✓	✓	✓	✓
XR7F	**Diagnostic**	8	R/W	3D7	00xxxx00	✓	✓	✓	✓	✓

Reset Codes: x = Not changed by reset (indeterminate on power-up)
d = Set from the corresponding data bus pin on trailing edge of reset
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0/1 by trailing edge of reset

Note: Check marks in the table above indicate the register listed to the left is implemented in the chip named at the top of the column
Note: 82C450 & 64xxx VGAs drive CRTs only, 65xxx VGAs drive both CRT and Flat Panel displays (Plasma, EL, and LCD)

32-BIT EXTENSION REGISTER SUMMARY

Reg	Group	Register Name	Bits	Access	Port	Reset			
DR00	BitBLT	BitBLT Offset	16/32	R/W	83D0-3	----xxxx	xxxxxxxx	----xxxx	xxxxxxxx
DR01	BitBLT	BitBLT Pattern ROP	16/32	R/W	87D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR02	BitBLT	BitBLT BG Color	16/32	R/W	8BD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR03	BitBLT	BitBLT FG Color	16/32	R/W	8FD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR04	BitBLT	BitBLT Control	16/32	R/W	93D0-3	--------	---0xxxx	xxxxxxxx	xxxxxxxx
DR05	BitBLT	BitBLT Source	16/32	R/W	97D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR06	BitBLT	BitBLT Destination	16/32	R/W	9BD0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx
DR07	BitBLT	BitBLT Command	16/32	R/W	9FD0-3	----0000	00000000	----xxxx	xxxxxxxx
DR08	Cursor	Cursor Control	16/32	R/W	A3D0-3	--------	--------	••••0000	000•••00
DR09	Cursor	Cursor Color 0-1	16/32	R/W	A7D0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR0A	Cursor	Cursor Color 2-3	16/32	R/W	ABD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DR0B	Cursor	Cursor Position	16/32	R/W	AFD0-3	x----xxx	xxxxxxxx	x----xxx	xxxxxxxx
DR0C	Cursor	Cursor Base Address	16/32	R/W	B3D0-3	--------	----xxxx	xxxxxx--	--------

Reset Codes:
x = Not changed by reset (indeterminate on power-up)
d = Set from configuration pin on trailing edge of reset
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Not implemented (read/write, reset to 0)
0/1 = Reset to 0/1 by trailing edge of reset

PCI CONFIGURATION REGISTER SUMMARY

Reg	Register Name	Bits	Access	Offset	Reset			
VENID	Vendor ID	16	R	00h			00010000	00101100
DEVID	Device ID	16	R	02h			00000000	11011000
DEVCTL	Device Control	16	R/W	04h			------10	10000000
DEVSTAT	Device Status	16	R/C	06h			00000000	0-------
REV	Revision	8	R	08h				-----rrr
PRG	Programming Interface	8	R	09h				00000000
SUB	Sub Class Code	8	R	0Ah				00000000
BASE	Base Class Code	8	R	0Bh				00000011
MBASE	Memory Base Address	32	R/W	10h	xxxxxxxx	xxx-----	--------	----0000
IOBASE	I/O Base Address	32	R/W	14h	xxxxxxxx	xxxxxxxx	xxxxxx--	------01

Note: R = Read, W = Write, C = Clear (1s written to specific bits will clear those bits)

Registers

GLOBAL CONTROL (SETUP) REGISTERS

The Setup Control Register and Video Subsystem Enable registers are used to enable or disable the VGA. The Setup Control register is also used to place the VGA in normal or setup mode (the Global Enable Register is accessible only during Setup mode). The Setup Control register is used only in ISA bus interfaces; the Video Subsystem Enable register is used only in Local Bus configurations. The various internal 'disable' bits 'OR' together to provide multiple ways of disabling the chip; all 'disable' bits must be off to enable access to the chip. When the chip is 'disabled' in this fashion, only bus access is disabled; other functions remain operational (memory refresh, display refresh, etc.).

Note: In setup mode in the IBM VGA, the Global Setup Register (defined as port address 102) actually occupies the *entire I/O space* . Only the lower 3 bits are used to decode and select this register. To avoid bus conflicts with other peripherals, reads should only be performed at the 10xh port addresses while in setup mode. To eliminate potential compatibility problems in widely varying PC systems, CHIPS' VGA controllers decode the Global Setup register at I/O port 102h only.

PCI CONFIGURATION REGISTERS (65545)

For PCI bus configuration in the 65545, ten 16-bit registers are implemented to allow identification of the chip, examination of various internal states, configuration of memory and I/O base addresses, and control of settings for various modes of operation. These registers are located at various offsets into the PCI configuration space which may be I/O or memory mapped depending on the system design.

GENERAL CONTROL REGISTERS

Two Input Status Registers read the SENSE function (Virtual Switch Register or internal RGB comparator output), pending CRT interrupt, display enable / horizontal sync output, and vertical retrace / video output. The Feature Control Register selects the vertical sync function while the Miscellaneous Output Register controls I/O address selection, clock selection, CPU access to display memory, display memory page selection, and horizontal and vertical sync polarity.

CGA/HERCULES REGISTERS

CGA Mode and Color Select registers are provided on-chip for emulation of CGA modes. Hercules Mode and Configuration registers are provided on-chip for emulation of Hercules mode.

SEQUENCER REGISTERS

The Sequencer Index Register contains a 3-bit index to the Sequencer Data Registers. The Reset Register forces an asynchronous or synchronous reset of the sequencer. The Sequencer Clocking Mode Register controls master clocking functions, video enable/disable and selects either an 8 or 9 dot character clock. A Plane/Map Mask Register enables the color plane and write protect. The Character Font Select Register handles video intensity and character generation and controls the display memory plane through the character generator select. The Sequencer Memory Mode Register handles all memory, giving access by the CPU to 4 / 16 / 32 KBytes, Odd / Even addresses (planes) and writing of data to display memory.

CRT CONTROLLER REGISTERS

The CRT Controller Index Register contains a 6-bit index to the CRT Controller Registers. Twenty one registers control various display functions: horizontal and vertical blanking and sync timing, panning and scrolling, cursor size and location, light pen, and text-mode underline.

GRAPHICS CONTROLLER REGISTERS

The Graphics Controller Index Register contains a 4-bit index to the Graphics Controller Registers. The Set/Reset Register controls the format of the CPU data to display memory. It also works with the Enable Set/Reset Register. Reducing 32 bits of display data to 8 bits of CPU data is accomplished by the Color Compare Register. Data Rotate Registers specify the CPU data bits to be rotated and subjected to logical operations. The Read Map Select Register reduces memory data for the CPU in the four plane (16 color) graphics mode. The Graphics Mode Register controls the write, read, and shift register modes. The Miscellaneous Register handles graphics/text, chaining of odd/even planes, and display memory mapping. Additional registers include Color Don't Care and Bit Mask.

ATTRIBUTE CONTROLLER AND COLOR PALETTE REGISTERS

The Attribute Controller Index Register contains a 5-bit index to the Attribute Controller Registers which consist of a 16-entry color lookup table with 6 bits per entry plus five additional control registers. A sixth index register bit is used to enable video. The Attribute Controller Registers handle color lookup table mapping, text/graphics mode control, overscan color selection, and color plane enabling. One register allows the display to be shifted left up to 8 pixels. Another register provides default values to extend the 6-bit lookup table values to 8 bits for modes providing less than 8 bits per pixel.

The color palette registers control the interface to the on-chip color palette. This on-chip palette fully implements the functions of the VGA-standard palette (Inmos IMSG176, Brooktree BT471/476, or equivalent functionality). The color palette primarily consists of a 256-entry color lookup table (also sometimes referred to as a CLUT), a mask register, index registers used to access the CLUT data, and triple 6 / 8-bit DACs used to drive analog RGB outputs to a CRT monitor. Each entry in the CLUT is 18 bits in length (6 bits each for red, green, and blue) so each CLUT data entry must be accessed sequentially as 3 separate bytes and each DAC output operates with 6 bits of resolution. In 24-bpp "True-Color" modes, the CLUT is bypassed and each DAC operates with 8-bit resolution.

EXTENSION REGISTERS

The 65540 / 545 defines a set of extension registers (called "XR's") which are addressed with the 7-bit Extension Register Index. The I/O port address is fixed at 3D6-3D7h and read/write access is always enabled to improve software performance.

The extension registers handle a variety of interfacing, compatibility, and display functions as discussed below. They are grouped into the following logical groups for discussion purposes:

1. Miscellaneous Registers include the chip version/revision, configuration, and various interface control and diagnostic functions.
2. Mapping Registers include paging controls and base registers for relocation of I/O and memory blocks.
3. Software Flags Registers provide locations for BIOS and driver software to store various temporary variable values on-chip
4. Clock Registers control the operation of the on-chip clock synthesizer
5. MultimediaRegisters control the operation of the video input port color key and mask
6. BitBLT Registers control the operation of the Bit-Block-Transfer (BitBLT) engine (65545 only) for graphicsacceleration.
7. Backwards Compatibility Registers control Hercules, MDA, and CGA emulation modes. Write Protect functions are provided to increase flexibility in providing backwards compatibility.
8. Alternate Horizontal and Vertical Registers handle all horizontal and vertical timing, including sync, blank and offset. These are used for backwards compatibility.
9. Flat Panel Registers handle all internal logic specific to driving of flat panel displays.

32-BIT REGISTERS

The 65545 also implements a group of sixteen 32-bit doubleword extension registers (called "DR's"). These registers are used for control of the high performance BitBLT and Hardware Cursor subsystems and may be mapped anywhere in the I/O and/or memory address space.

For ISA and VL-Bus configurations, the 32-bit registers take up 32 doubleword locations in the 16-bit I/O address space (only the first 13 registers are defined; the remaining locations are reserved). An 8-bit extension register is provided to program the base address. The address is of the form "bnnn nn1b bbbb bbxx" (where b specifies the value programmed into the base register and 'n' selects one of the 32 register locations). The base register is typically programmed with '74h' to map the 32-bit registers to I/O addresses x3D0-x3D3h (unused ports in the standard VGA I/O address range).

For PCI bus configurations, the 32-bit registers are mapped to both the memory and I/O address spaces. The PCI configuration registers contain an I/O base register which defines a 1KB space (256 doublewords) which allows the 32-bit register space to start on any 1KB boundary in the I/O address space. In addition, the PCI memory base register specifies an 8MB memory address space; display memory is mapped into the lower 2 megabytes and the 32-bit registers are mapped into the upper 6 megabytes.

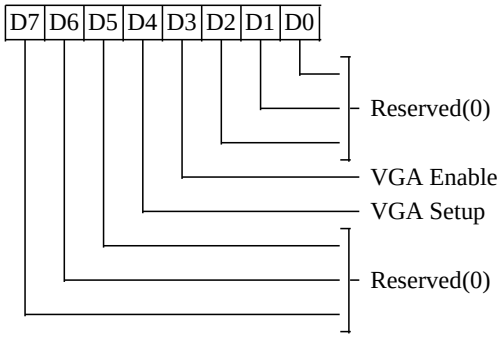
Note: The state of most of the standard VGA registers is undefined at reset. The state at Reset of all registers specific to the 65540 / 545 (extension registers and 32-bit registers) is summarized in the register summary tables.

Global Control (Setup) Registers

Register Mnemonic	Register Name	Index	Access	I/O I/O Address	Page
SETUP	Setup Control	–	W	46E8h (ISA Bus Only)	53
VSE	Video Subsystem Enable	–	W	3C3h (Local Bus Only)	53
ENAB	Global Enable	–	RW	102h (ISA Bus / Setup Mode Only)	54

SETUP CONTROL REGISTER (SETUP)

Write only at I/O Address 46E8h



This register is effective in ISA bus configuration only and is not used in local bus or PCI bus configurations. In ISA bus configuration, this register is ignored if XR70 bit-7 is set to 1 (the default is 0).

In local bus configurations, the VGA may be enabled and disabled using register 3C3. In PCI bus configurations (65545), the VGA may be enabled and disabled via the PCI configuration registers. Setup mode is available only in ISA bus configuration via this register.

This register is cleared by RESET.

2-0 Reserved (0)

3 VGA Enable

0 VGA is disabled
1 VGA is enabled

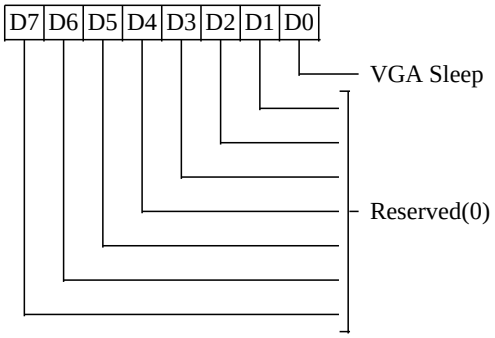
4 Setup Mode

0 VGA is in Normal Mode
1 VGA is in Setup Mode

7-5 Reserved (0)

VIDEOSUBSYSTEMENABLEREGISTER(VSE)

Write Only at I/O Address 3C3h



This register is accessible in Local Bus configurations only. It is ignored in ISA bus configurations (registers 102h and 46E8h are used in ISA bus configurations to control VGA enable and disable). Access to this register may be disabled by setting XR70 bit-7 to 1 (the default is 0).

This register is cleared by RESET to disable the VGA. In this state, only register 3C3 is accessible (the other registers in the VGA I/O address range will be inaccessible and read or write accesses to VGA I/O addresses other than 3C3 will be ignored) until bit-0 of this register is set to 1.

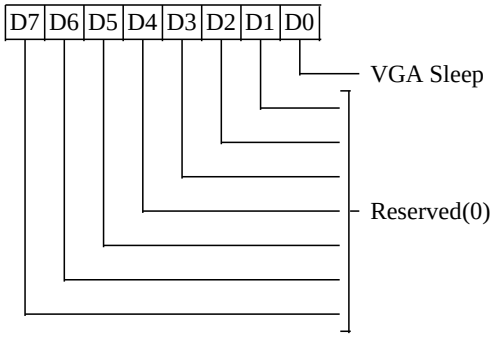
In PCI bus configurations, VGA enable and disable are controlled via the PCI configuration registers and this register is ignored.

0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

GLOBAL ENABLE REGISTER (ENAB)
Read/Write at I/O Address 102h



This register is accessible only in setup mode (46E8 bit-4 = 1). If the VGA is not in setup mode (46E8 bit-4 = 0), attempts to access this register are ignored.

Bit-0 of this register is cleared by RESET in ISA bus configurations to disable the VGA (all VGA memory and I/O addresses except 102h and 46E8h are ignored). Bit-0 of this register is AND'ed with bit-3 of register 46E8: the VGA is enabled only if both bits are set. If the VGA is disabled, only register 46E8 is accessible.

0 VGA Sleep

0 VGA is disabled
1 VGA is enabled

7-1 Reserved (0)

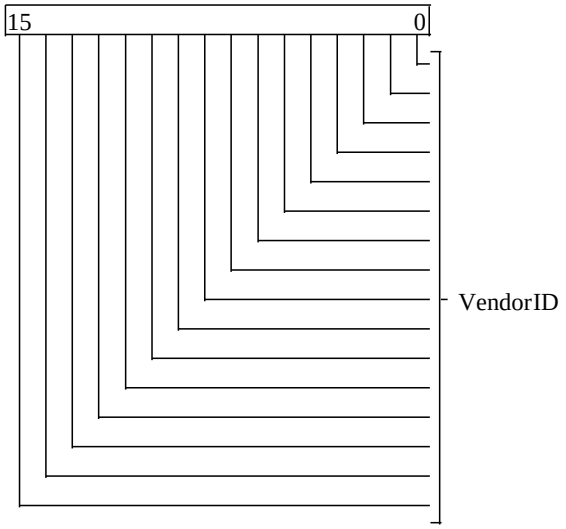
PCI Configuration Registers

Register Mnemonic	Register Name	Offset	Access	Reset State	Page
VENID	Vendor ID	00h	R	0001 0000 0010 1100	55
DEVID	Device ID	02h	R	0000 0000 1101 1000	55
DEVCTL	Device Control	04h	R/W	0000 0010 1000 0000	56
DEVSTAT	Device Status	06h	R/C	0000 0000 0000 0000	56
REV	Revision	08h	R	0000 0000	57
PRG	Programming Interface	09h	R	0000 0000	57
SUB	Sub Class Code	0Ah	R	0000 0000	57
BASE	Base Class Code	0Bh	R	0000 0011	57
MBASE	Memory Base Address	10h	R/W	xxxx xxxx xxx0 0000 0000 0000 0000 0000	58
IOBASE	I/O Base Address	14h	R/W	xxxx xxxx xxxx xxxx xxxx xx00 0000 0001	58

Note: 'Access' codes are R=Read, W=Write, and C=Clear (writing a 1 to a bit clears that bit)

VENDOR ID REGISTER (VENID)

Read/Only at PCI Configuration Offset 00h
Byte or Word Accessible
Accessible in PCI Bus Configuration Only

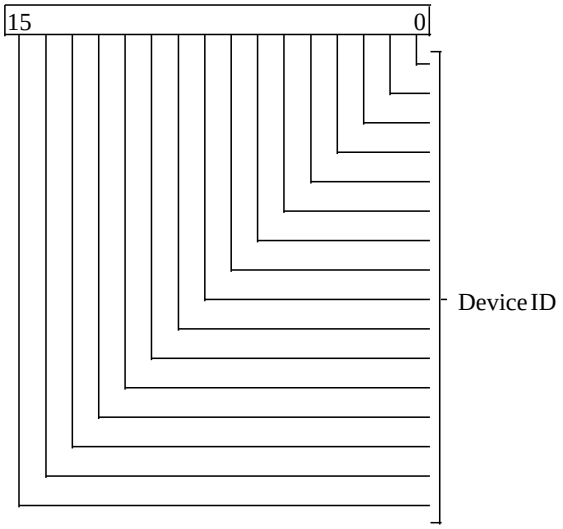


15–0 Vendor ID

Read-Only. Always returns 102Ch (4140d)

DEVICE ID REGISTER (DEVID)

Read/Only at PCI Configuration Offset 02h
Byte or Word Accessible
Accessible in PCI Bus Configuration Only

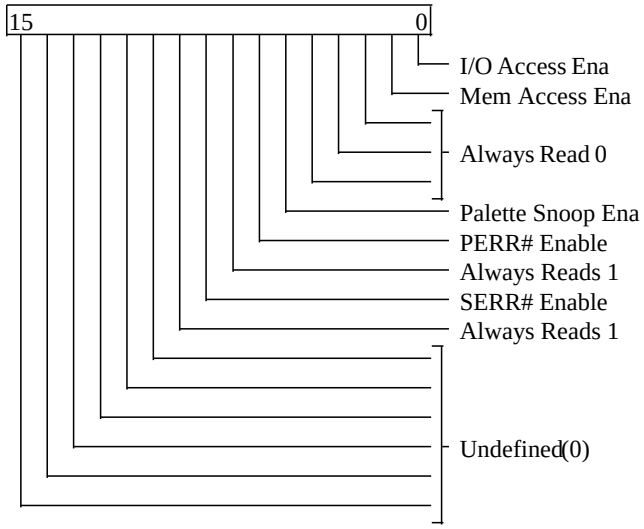


15–0 Device ID

Read-Only. Always returns 00D8h

DEVICE CONTROL REGISTER (DEVCTL)

Read/Write at PCI Configuration Offset 04h
Byte or Word Accessible
Accessible in PCI Bus Configuration Only



0 I/O Access Enable

When set, the chip will respond to I/O cycles for addresses within the range specified by the IOBASE register.

1 Memory Access Enable

When set, the chip will respond to memory cycles for addresses within the range specified by the MBASE register.

2 Bus Master (Always Reads 0)

3 Special Cycles (Always Reads 0)

4 Mem Write & Invalidate (Always Reads 0)

5 Palette Snoop Enable

When set, the chip will not respond to VGA Palette Accesses. Reads will be ignored but writes will still update the internal palette.

6 PERR# Enable

Set to enable PERR# response for detected data parity errors.

7 Wait Cycle Control (Always Reads 1)

8 SERR# Enable

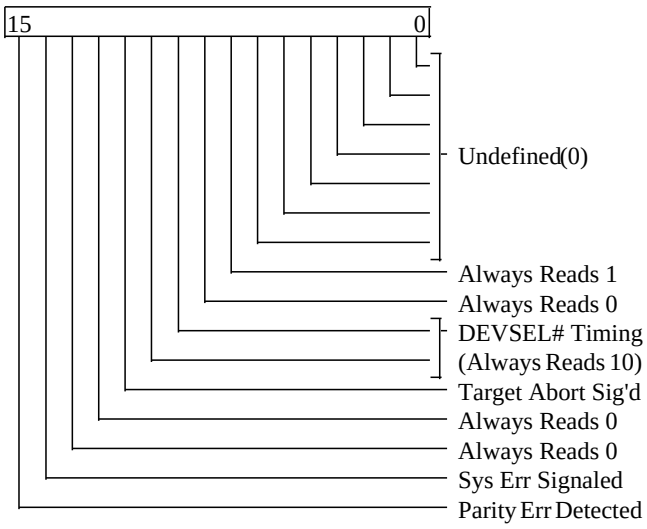
Set to enable SERR# response for detected address / command parity errors. The chip will also generate a Target Abort.

9 Fast Back-to-Back Enable for Masters (Always Reads 0)

15-10 Undefined / Reserved (0)

DEVICE STATUS REGISTER (DEVSTAT)

Read/Only at PCI Configuration Offset 06h
Byte or Word Accessible
Accessible in PCI Bus Configuration Only



6–0 Undefined / Reserved (0)

7 Fast Back-to-Back Capable (1)

8 Data Parity Error Detect (0)

Implemented by bus masters only.

10–9 DEVSEL# Timing

Always responds '10' (Slow)

11 Target Abort Signaled

Set whenever a Target Abort is generated on the bus. This can happen under the following conditions:

1) Command/Address cycle parity error
2) Invalid byte enables received
3) VGA core unable to complete a cycle

12 Received Target Abort (0)

Implemented by bus masters only.

13 Master Abort (0)

Implemented by bus masters only.

14 System Error Signaled

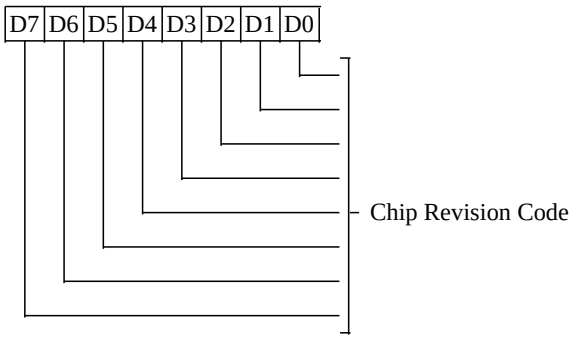
Set whenever SERR# is asserted.

15 Parity Error Detected

Set when data parity error is detected even if PERR# response disabled (DEVCTL bit-6)

REVISION REGISTER (REV)

Read/Only at PCI Configuration Offset 08h
Byte Accessible
Accessible in PCI Bus Configuration Only



2-0 Chip Revision Code

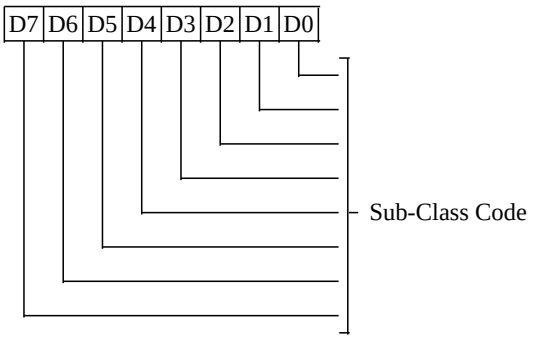
These bits match XR00 bits 2-0. Revision codes start at 0 and are incremented for each silicon revision.

7-3 Reserved (0)

These bits are defined by the PCI 2.0 specification as additional revision code bits. They always read zero.

SUB CLASS CODE REGISTER (SUB)

Read/Only at PCI Configuration Offset 0Ah
Byte Accessible
Accessable in PCI Bus Configuration Only

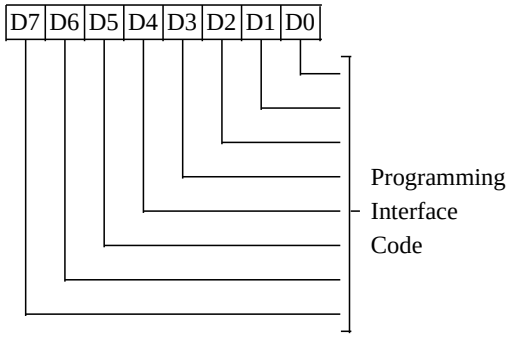


7-0 Sub-Class Code

This register always returns a value of 00h to indicate "VGA Compatible Controller".

PROGRAMMING INTERFACE REGISTER (PRG)

Read/Only at PCI Configuration Offset 09h
Byte Accessible
Accessable in PCI Bus Configuration Only

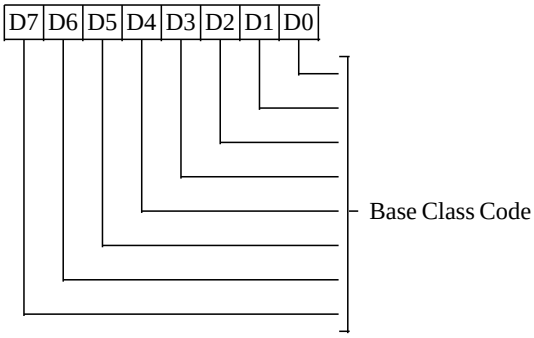


7-0 Programming Interface Code

This register always returns a value of 00h (no special register-level device-independent interface definition is defined).

BASE CLASS CODE REGISTER (BASE)

Read/Only at PCI Configuration Offset 0Bh
Byte Accessible
Accessable in PCI Bus Configuration Only

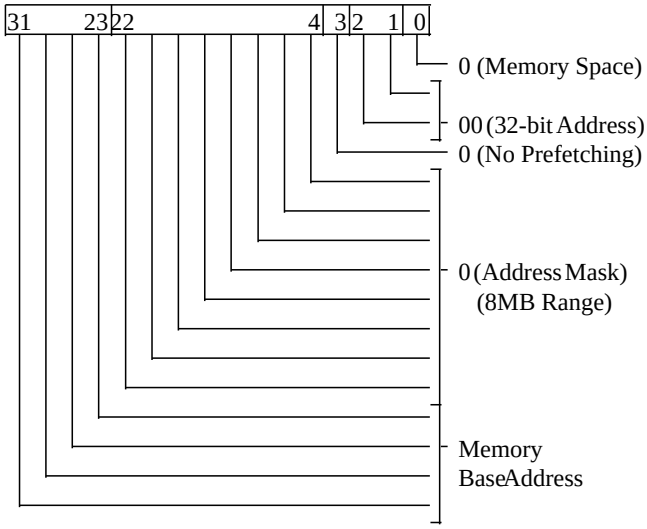


7-0 Base Class Code

This register always returns a value of 03h to indicate base class "Display Controller".

MEMORY BASE REGISTER (MBASE)

Read/Write at PCI Configuration Offset 10h
Byte, Word, or DoubleWord Accessible
Accessable in PCI Bus Configuration Only



0 Memory / IO Space (0)

Always returns 0 to indicate memory space

2-1 Memory Type (00)

Always return 0 to indicate 32-bit address

3 Prefetchable Memory (0)

Always return 0 to prevent prefetching

22-4 Address Mask (0)

Always returns 0 to indicate an 8MB range

31-23 Memory Base Address

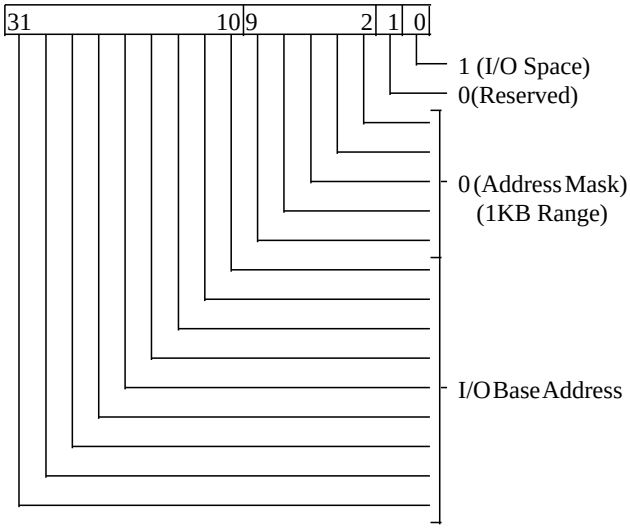
R/W in bits 23 and above to indicate an 8MB address range. The lower 2MB is for video memory and the rest is for memory mapped IO. The actual value programmed in this field determines the start of the range in the 32-bit memory address space. For example:

	Value Programmed	Memory Address Range
0:	000000000b	IllegalSetting
8MB:	000000001b	00800000h - 00FFFFFFh
16MB:	000000010b	01000000h - 017FFFFFh
24MB:	000000011b	01800000h - 01FFFFFFh
32MB:	000000100b	02000000h - 027FFFFFh
40MB:	000000101b	02800000h - 02FFFFFFh
...	...	...

Note: XR08 provides the same function for ISA/VL. It is ignored in PCI bus mode.

I/O BASE REGISTER (IOBASE)

Read/Write at PCI Configuration Offset 14h
Byte, Word, or DoubleWord Accessible
Accessable in PCI Bus Configuration Only



0 Memory / IO Space (1)

Always returns 1 to indicate I/O space

1 Undefined / Reserved (0)

9-2 Address Mask (0)

All bits in in this field return 0 to indicate a 1KB I/O address range

31-10 I/O Base Address

R/W in bits 10 and above to indicate a 1KB address range for the 32-bit registers (DRxx registers). The actual value programmed in this field determines the start of the range in the 32-bit I/O address space. For example:

Value Programmed	I/O Address Range
000000h	IllegalSetting
000001h	00000400h - 000007FFh
000002h	00000800h - 00000BFFh
000003h	00000C00h - 00000FFFh
000004h	00001000h - 000013FFh
...	...

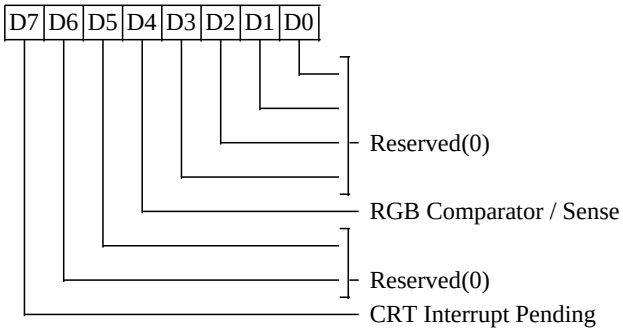
Note: XR07 provides the same function for ISA/VL. It is ignored in PCI bus mode.

Note: In PCI bus configuration, the DR registers may also be memory mapped to the upper megabyte of the 2MB memory space (see MBASE).

General Control & Status Registers

Register Mnemonic	RegisterName	Index	Access	I/O Address	Protect Group	Page
ST00	Input Status 0	–	R	3C2h	–	59
ST01	Input Status 1	–	R	3BAh/3DAh	–	59
FCR	Feature Control	–	W	3BAh/3DAh	5	60
			R	3CAh		
MSR	MiscellaneousOutput	–	W	3C2h	5	60
			R	3CCh		

INPUT STATUS REGISTER 0 (ST00)
Read only at I/O Address at 3C2h



3-0 Reserved (0)

4 RGB Comparator / Sense

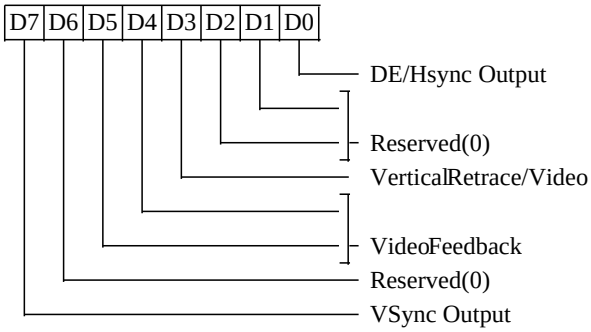
This bit returns the state of the output of the RGB output comparator or the output of the Virtual Switch Register (XR1F bit 0, 1, 2, or 3) if enabled by XR1F bit-7.

6-5 Reserved (0)

7 CRT Interrupt Pending

0 Indicates no CRT interrupt is pending
1 Indicates a CRT interrupt is waiting to be serviced

INPUT STATUS REGISTER 1 (ST01)
Read only at I/O Address 3BAh/3DAh



0 Display Enable/HSYNC Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-4).

0 Indicates DE or HSYNC inactive
1 Indicates DE or HSYNC active

2-1 Reserved (0)

3 Vertical Retrace/Video

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-5).

0 Indicates VSYNC or video inactive
1 Indicates VSYNC or video active

5-4 Video Feedback 1, 0

These are diagnostic video bits which are selected via the Color Plane Enable Register.

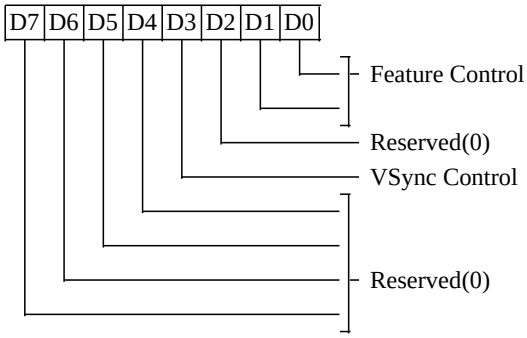
6 Reserved (0)

7 VSync Output

The functionality of this bit is controlled by the Emulation Mode register (XR14 bit-6). It reflects the active status of the VSYNC output: 0=inactive, 1=active.

FEATURE CONTROL REGISTER (FCR)

Write at I/O Address 3BAh/3DAh
Read at I/O Address 3CAh
Group 5 Protection



1-0 Feature Control

These bits are used internal to the chip in conjunction with the Configuration Register (XR01). When enabled by XR01 bits 2-3 and Misc Output Register bits 3-2 = 10, these bits determine the pixel clock frequency typically as follows:

FCR1:0 = 00 = 40.000 MHz
FCR1:0 = 01 = 50.350 MHz
FCR1:0 = 10 = User defined
FCR1:0 = 11 = 44.900 MHz

This preserves compatibility with drivers developed for earlier generation Chips and Technologies VGA controllers.

2 Reserved (0)

3 VSync Control

This bit is cleared by RESET.

0 VSync output on the VSYNC pin
1 Logical 'OR' of VSync and Display Enable output on the VSYNC pin

This capability is not typically very useful, but is provided for IBM compatibility.

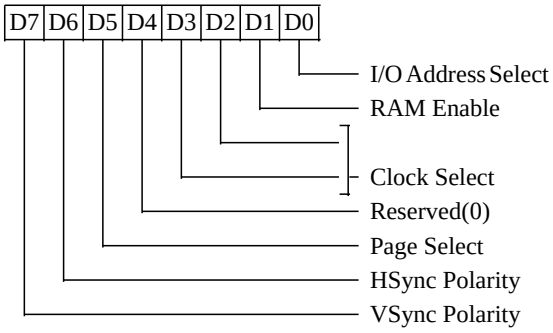
7-4 Reserved (0)

CRT Display Sync Polarities

V	H	Display	HFreq	VFreq
P	P	>480 Line	Variable	Variable
P	P	200 Line	15.7 KHz	60 Hz
N	P	350 Line	21.8 KHz	60 Hz
P	N	400 Line	31.5 KHz	70 Hz
N	N	480 Line	31.5 KHz	60 Hz

MISCELLANEOUSOUTPUTREGISTER(MSR)

Write at I/O Address 3C2h
Read at I/O Address 3CCh
Group 5 Protection



This register is cleared by RESET.

0 I/O Address Select
This bit selects 3Bxh or 3Dxh as the I/O address for the CRT Controller registers, the Feature Control Register (FCR), and Input Status Register 1 (ST01).

0 Select 3Bxh I/O address
1 Select 3Dxh I/O address

1 RAM Enable

0 Prevent CPU access to display memory
1 Allow CPU access to display memory

3-2 Clock Select. These bits usually select the dot clock source for the CRT interface:

MSR3:2 = 00 = Select CLK0
MSR3:2 = 01 = Select CLK1
MSR3:2 = 10 = Select CLK2
MSR3:2 = 11 = Select CLK3

See extension register XR01 bits 2-3 (Configuration) and FCR bits 0-1 for variations of the above clock selection mapping. See also XR1F (Virtual Switch Register) for additional functionality potentially controlled by these bits.

4 Reserved (0)

5 Page Select. In Odd/Even Memory Map Mode 1 (GR6), this bit selects the upper or lower 64 KByte page in display memory for CPU access: 0=select upper page; 1=select lower page.

6 CRT HSync Polarity. 0=pos, 1=neg

7 CRT VSync Polarity. 0=pos, 1=neg

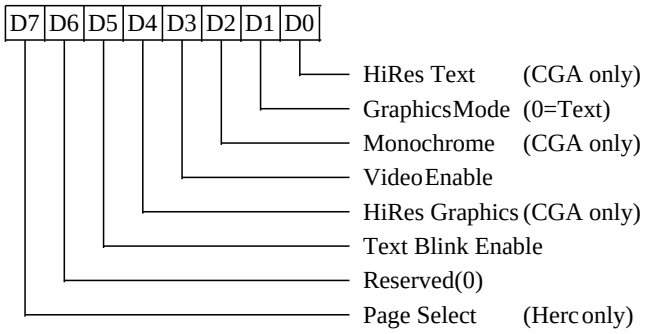
(Blank pin polarity can be controlled via the Video Interface Register, XR28). XR55 bits 6-7 are used to control H/V sync polarity instead of these bits if XR51 bit-2 = 1 (display type = flat panel).

CGA/Hercules Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
MODE	CGA/Hercules Mode	–	R/W	3D8h	–	61
COLOR	CGA Color Select	–	R/W	3D9h	–	62
HCFG	Hercules Configuration	–	R/W	3BFh	–	62

CGA/HERCULES MODE CONTROL REGISTER (MODE)

Read/Write at I/O Address 3B8h/3D8h



This register is effective only in CGA and Hercules modes. It is accessible if CGA or Hercules emulation mode is selected or the extension registers are enabled. If the extension registers are enabled, the address is determined by the address select in the Miscellaneous Outputs register. Otherwise the address is determined by the emulation mode. It is cleared by RESET.

0 CGA 80/40 Column Text Mode

0 Select 40 column CGA text mode
1 Select 80 column CGA text mode

1 CGA/Hercules Graphics/Text Mode

0 Select text mode
1 Select graphics mode

2 CGA Mono/Color Mode

0 Select CGA color mode
1 Select CGA monochrome mode

3 CGA/Hercules Video Enable

0 Blank the screen
1 Enable video output

4 CGA High Resolution Mode

0 Select 320x200 graphics mode
1 Select 640x200 graphics mode

5 CGA/Hercules Text Blink Enable

0 Disable character blink attribute (blink attribute bit-7 used to control background intensity)

1 Enable character blink attribute

6 Reserved (0)

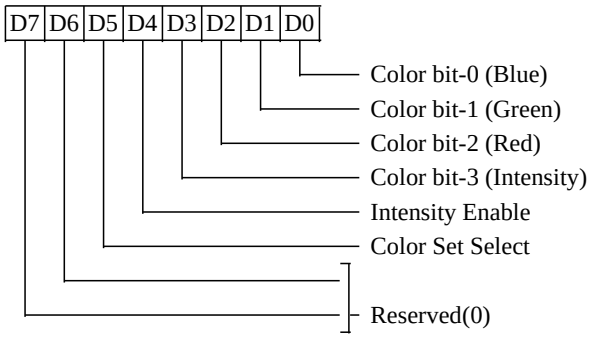
7 Hercules Page Select

0 Select the lower part of memory (starting address B0000h) in Hercules Graphics Mode

1 Select the upper part of the memory (starting address B8000h) in Hercules Graphics Mode

CGA COLOR SELECT REGISTER (COLOR)

Read/Write at I/O Address 3D9h



This register is effective only in CGA modes. It is accessible if CGA emulation mode is selected or the extension registers are enabled. This register may also be read or written as an Extension Register (XR7E). It is cleared by Reset.

3-0 Color

320x200 4-color: Background Color (color when the pixel value is 0)

The foreground colors (colors when the pixel value is 1-3) are determined by bit-5 of this register.

640x200 2-color:
Foreground Color (color when the pixel value is 1)

The background color (color when the pixel value is 0) is black.

4 Intensity Enable

Text Mode:	Enables intensified background colors
320x200 4-color:	Enables intensified colors 0-3
640x200 2-color:	Don't care

5 Color Set Select

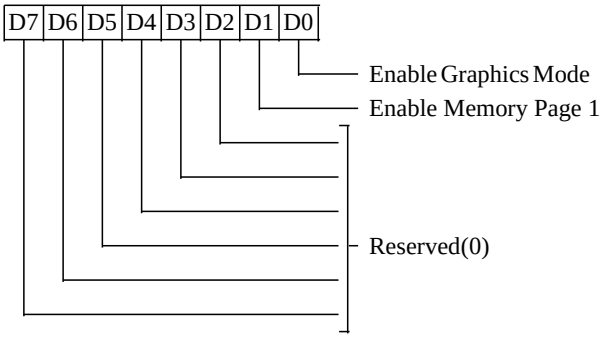
This bit selects one of two available CGA color palettes to be used in 320x200 graphics mode (it is ignored in all other modes) according to the following table:

Pixel Value	Color Set 0	Color Set 1
0 0	Color per bits 0-3	Color per bits 0-3
0 1	Green	Cyan
1 0	Red	Magenta
1 1	Brown	White

7-6 Reserved(0)

HERCULES CONFIGURATION REGISTER (HCFG)

Write only at I/O Address 3BFh



This register is effective only in Hercules mode. It is accessible in Hercules emulation mode or if the extension registers are enabled. It may be read back through XR14 bits 2 & 3. It is cleared by Reset.

0 Enable Graphics Mode

0 Lock the chip in Hercules text mode. In this mode, the CPU has access only to memory address range B0000h-B7FFFh (in text mode the same area of display memory wraps around 8 times within this range such that B0000 accesses the same display memory location as B1000, B2000, etc.).

1 Permit entry to Hercules Graphics mode

1 Enable Memory Page 1

0 Prevent setting of the Page Select bit (bit 7 of the Hercules Mode Control Register). This function also restricts memory usage to addresses B0000h-B7FFFh.

1 The Page Select bit can be set and the upper part of display memory (addresses B8000h - BFFFFh) is available.

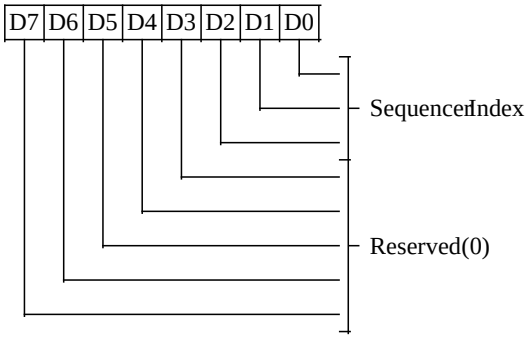
7-2 Reserved (0)

Sequencer Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
SRX	Sequencer Index	–	R/W	3C4h	1	63
SR00	Reset	00h	R/W	3C5h	1	63
SR01	Clocking Mode	01h	R/W	3C5h	1	64
SR02	Plane/Map Mask	02h	R/W	3C5h	1	64
SR03	Character Font	03h	R/W	3C5h	1	65
SR04	Memory Mode	04h	R/W	3C5h	1	66
SR07	Horizontal Character Counter Reset	07h	W	3C5h	–	66

SEQUENCER INDEX REGISTER (SRX)

Read/Write at I/O Address 3C4h



This register is cleared by reset.

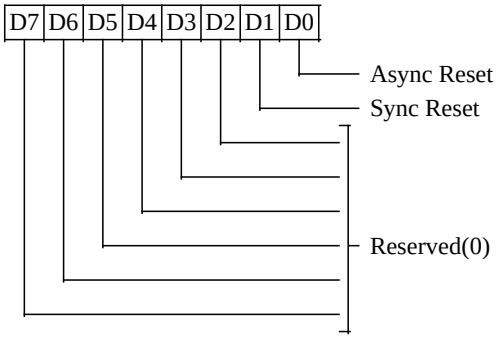
2-0 Sequencer Index

These bits contain a 3-bit Sequencer Index value used to access sequencer data registers at indices 0 through 7.

7-3 Reserved (0)

SEQUENCER RESET REGISTER (SR00)

Read/Write at I/O Address 3C5h
Index 00h
Group 1 Protection



0 Asynchronous Reset

0 Force asynchronous reset
1 Normal operation

Display memory data will be corrupted if this bit is set to zero.

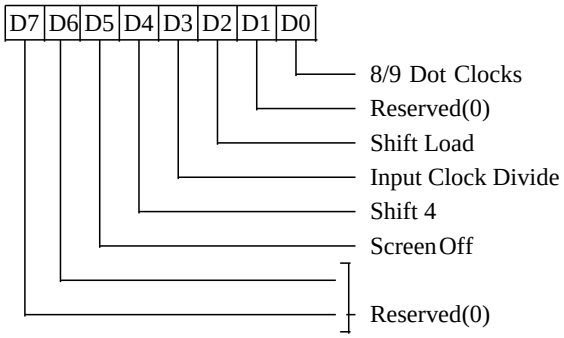
1 Synchronous Reset

0 Force synchronous reset
1 Normal operation

Display memory data is not corrupted if this bit is set to zero for a short period of time (a few tenths of a microsecond). See also XR0E.

7-2 Reserved (0)

SEQUENCER CLOCKING MODE REGISTER (SR01)
Read/Write at I/O Address 3C5h
Index 01h
Group 1 Protection



0 8/9 Dot Clocks

This bit determines whether a character clock is 8 or 9 dot clocks long.

0 Select 9 dots/character clock
1 Select 8 dots/character clock

1 Reserved (0)

2 Shift Load

0 Load video data shift registers every character clock
1 Load video data shift registers every other character clock

Bit-4 of this register must be 0 for this bit to be effective.

3 Input Clock Divide

0 Sequencer master clock output on the PCLK pin (used for 640 (720) pixel modes)
1 Master clock divided by 2 output on the PCLK pin (used for 320 (360) pixel modes)

4 Shift 4

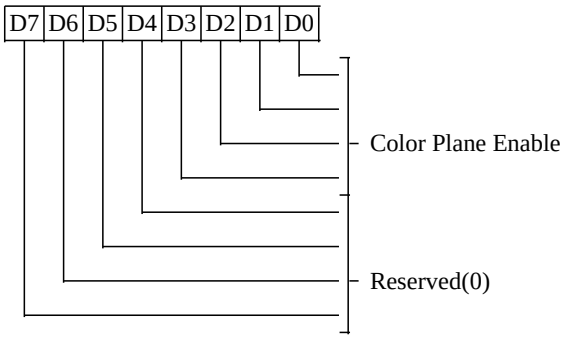
0 Load video shift registers every 1 or 2 character clocks (depending on bit-2 of this register)
1 Load shift registers every 4th character clock.

5 Screen Off

0 Normal Operation
1 Disable video output and assign all display memory bandwidth for CPU accesses

7-6 Reserved (0)

SEQUENCER PLANE/MAP MASK REGISTER (SR02)
Read/Write at I/O Address 3C5h
Index 02h
Group 1 Protection



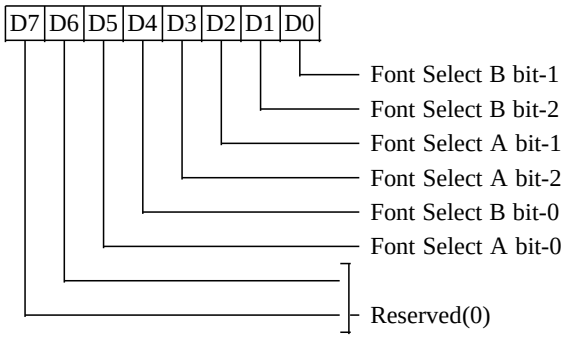
3-0 Color Plane Enable

0 Write protect corresponding color plane
1 Allow write to corresponding color plane.

In Odd/Even and Quad modes, these bits still control access to the corresponding color plane.

7-4 Reserved (0)

CHARACTER FONT SELECT REGISTER (SR03)
Read/Write at I/O Address 3C5h
Index 03h
Group 1 Protection



In text modes, bit-3 of the video data's attribute byte normally controls the foreground intensity. This bit may be redefined to control switching between character sets. This latter function is enabled whenever there is a difference in the values of the Character Font Select A and the Character Font Select B bits. If the two values are the same, the character select function is disabled and attribute bit-3 controls the foreground intensity.

SR04 bit-1 must be 1 for the character font select function to be active. Otherwise, only character fonts 0 and 4 are available.

1-0 High order bits of Character Generator Select B

3-2 High order bits of Character Generator Select A

4 Low order bit of Character Generator Select B

5 Low order bit of Character Generator SelectA

7-6 Reserved (0)

The following table shows the display memory plane selected by the Character Generator Select A and B bits.

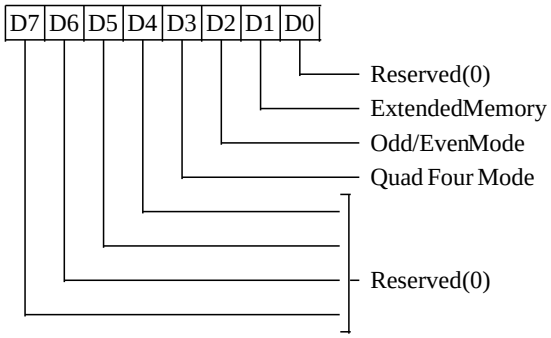
Code	Character Generator Table Location
0	First 8K of Plane 2
1	Second 8K of Plane 2
2	Third 8K of Plane 2
3	Fourth 8K of Plane 2
4	Fifth 8K of Plane 2
5	Sixth 8K of Plane 2
6	Seventh 8K of Plane 2
7	Eighth 8K of Plane 2

where 'code' is:

Character Generator Select A (bits 3, 2, 5) when bit-3 of the attribute byte is one.

Character Generator Select B (bits 1, 0, 4) when bit-3 of the attribute byte is zero.

SEQUENCER MEMORY MODE REGISTER (SR04)
Read/Write at I/O Address 3C5h
Index 04h
Group 1 Protection



0 Reserved (0)

1 Extended Memory

0 Restrict CPU access to 4 / 16 / 32 KBytes
1 Allow complete access to memory

This bit should normally be 1.

2 Odd/Even Mode

0 CPU accesses to Odd/Even addresses are directed to corresponding odd/even planes
1 All planes are accessed simultaneously (IRGB color)

Bit-3 of this register must be 0 for this bit to be effective. This bit affects only CPU write accesses to display memory.

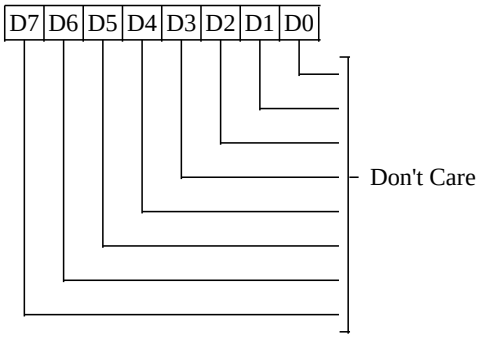
3 Quad Four Mode

0 CPU addresses are mapped to display memory as defined by bit-2 of this register
1 CPU addresses are mapped to display memory modulo 4. The two low order CPU address bits select the display memory plane.

This bit affects both CPU reads and writes to display memory.

7-4 Reserved (0)

SEQUENCER HORIZONTAL CHARACTER COUNTER RESET (SR07)
Read/Write at I/O Address 3C5h
Index 07h



Writing to SR07 with any data will cause the horizontal character counter to be held reset (character counter output = 0) until a write to any other sequencer register with any data value. The write to any index in the range 0-6 clears the latch that is holding the reset condition on the character counter.

The vertical line counter is clocked by a signal derived from horizontal display enable (which does not occur if the horizontal counter is held reset). Therefore, if the write to SR07 occurs during vertical retrace, the horizontal and vertical counters will both be set to zero. A write to any other sequencer register may then be used to start both counters with reasonable synchronization to an external event via software control.

This is a standard VGA register which was not documented by IBM.

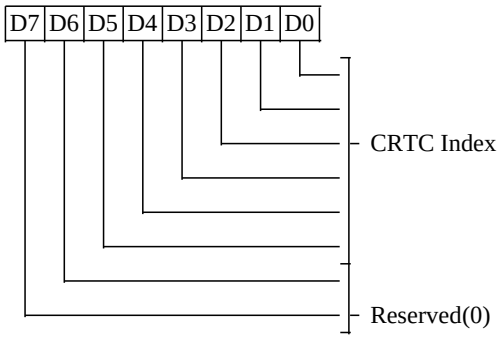
CRT Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
CRX	CRTC Index	–	R/W	3B4h/3D4h	–	68
CR00	Horizontal Total	00h	R/W	3B5h/3D5h	0	68
CR01	Horizontal Display Enable End	01h	R/W	3B5h/3D5h	0	68
CR02	Horizontal Blank Start	02h	R/W	3B5h/3D5h	0	69
CR03	Horizontal Blank End	03h	R/W	3B5h/3D5h	0	69
CR04	Horizontal Sync Start	04h	R/W	3B5h/3D5h	0	70
CR05	Horizontal Sync End	05h	R/W	3B5h/3D5h	0	70
CR06	Vertical Total	06h	R/W	3B5h/3D5h	0	71
CR07	Overflow	07h	R/W	3B5h/3D5h	0/3	71
CR08	Preset Row Scan	08h	R/W	3B5h/3D5h	3	72
CR09	Maximum Scan Line	09h	R/W	3B5h/3D5h	2/4	72
CR0A	Cursor Start Scan Line	0Ah	R/W	3B5h/3D5h	2	73
CR0B	Cursor End Scan Line	0Bh	R/W	3B5h/3D5h	2	73
CR0C	Start Address High	0Ch	R/W	3B5h/3D5h	–	74
CR0D	Start Address Low	0Dh	R/W	3B5h/3D5h	–	74
CR0E	Cursor Location High	0Eh	R/W	3B5h/3D5h	–	74
CR0F	Cursor Location Low	0Fh	R/W	3B5h/3D5h	–	74
CR10	Vertical Sync Start (See Note 2)	10h	W or R/W	3B5h/3D5h	4	75
CR11	Vertical Sync End (See Note 2)	11h	W or R/W	3B5h/3D5h	3/4	75
CR10	Lightpen High (See Note 2)	10h	R	3B5h/3D5h	–	75
CR11	Lightpen Low (See Note 2)	11h	R	3B5h/3D5h	–	75
CR12	Vertical Display Enable End	12h	R/W	3B5h/3D5h	4	76
CR13	Offset	13h	R/W	3B5h/3D5h	3	76
CR14	Underline Row	14h	R/W	3B5h/3D5h	3	76
CR15	Vertical Blank Start	15h	R/W	3B5h/3D5h	4	77
CR16	Vertical Blank End	16h	R/W	3B5h/3D5h	4	77
CR17	CRT Mode Control	17h	R/W	3B5h/3D5h	3/4	78
CR18	Line Compare	18h	R/W	3B5h/3D5h	3	79
CR22	Memory Data Latches	22h	R	3B5h/3D5h	–	80
CR24	Attribute Controller Toggle	24h	R	3B5h/3D5h	–	80

Note 1: When MDA or Hercules emulation is enabled, the CRTC I/O address should be set to 3B0h-3B7h by setting the I/O address select bit in the Miscellaneous Output register (3C2h/3CCh bit-0) to zero. When CGA emulation is enabled, the CRTC I/O address should be set to 3D0h-3D7h by setting Misc Output Register bit-0 to 1.

Note 2: In the EGA, all CRTC registers except the cursor (CR0C-CR0F) and light pen (CR10 and CR11) registers are write-only (i.e., no read back). In both the EGA and VGA, the light pen registers are at index locations conflicting with the vertical sync registers. This would normally prevent reads and writes from occurring at the same index. Since the light pen registers are not normally useful, the VGA provides software control (CR03 bit-7) of whether the vertical sync or light pen registers are readable at indices 10-11.

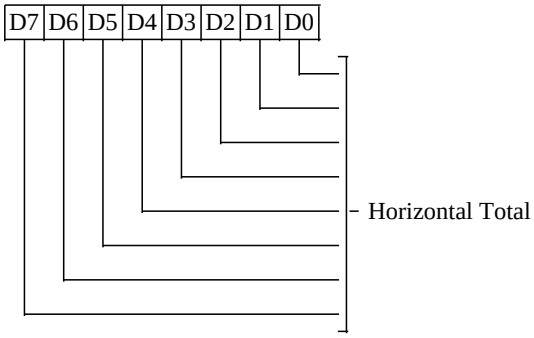
CRTC INDEX REGISTER (CRX)
Read/Write at I/O Address 3B4h/3D4h



5-0 CRTC Data Register Index

7-6 Reserved (0)

HORIZONTAL TOTAL REGISTER (CR00)
Read/Write at I/O Address 3B5h/3D5h
Index 00h
Group 0 Protection

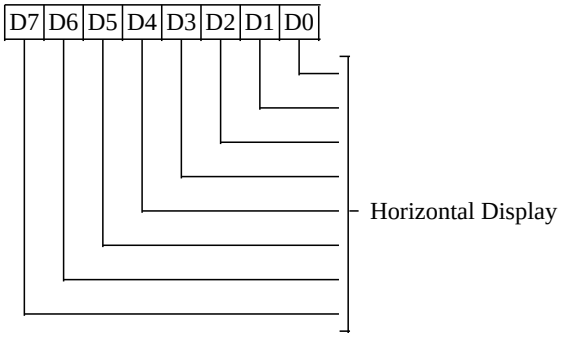


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Total

Total number of character clocks per line = contents of this register + 5. This register determines the horizontal sweep rate.

HORIZONTAL DISPLAY ENABLE END REGISTER (CR01)
Read/Write at I/O Address 3B5h/3D5h
Index 01h
Group 0 Protection

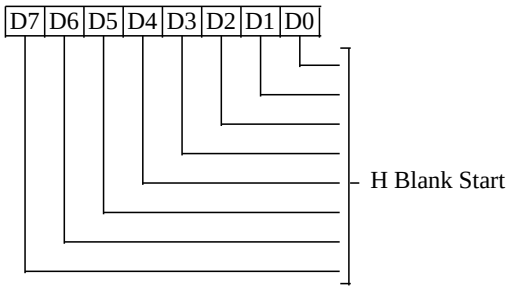


This register is used for all VGA and EGA modes on CRTs. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Display

Number of Characters displayed per scan line – 1.

HORIZONTAL BLANK START REGISTER (CR02)
Read/Write at I/O Address 3B5h/3D5h
Index 02h
Group 0 Protection

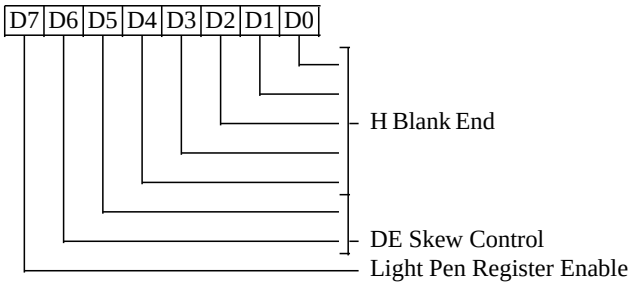


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Blank Start

These bits specify the beginning of horizontal blank in terms of character clocks from the beginning of the display scan. The period between Horizontal Display Enable End and Horizontal Blank Start is the right side border on screen.

HORIZONTAL BLANK END REGISTER (CR03)
Read/Write at I/O Address 3B5h/3D5h
Index 03h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Blank End

These are the lower 5 bits of the character clock count used to define the end of horizontal blank. The interval between the end of horizontal blank and the beginning of the display (a count of 0) is the left side border on the screen. If the horizontal blank width desired is W clocks, the 5-bit value programmed in this register = [contents of CR02 + W] and 1Fh. The most significant bit is programmed in CR05 bit-7. This bit = [(CR02 + W) and 20h]/20h.

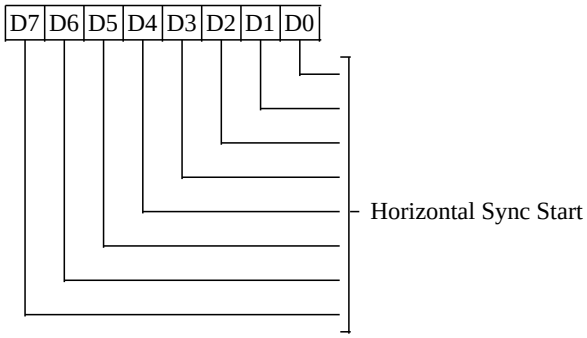
6-5 Display Enable Skew Control

Defines the number of character clocks that the Display Enable signal is delayed to compensate for internal pipeline delays.

7 Light Pen Register Enable

This bit must be 1 for normal operation; when this bit is 0, CRTC registers CR10 and CR11 function as lightpen readback registers.

HORIZONTAL SYNC START REGISTER (CR04)
Read/Write at I/O Address 3B5h/3D5h
Index 04h
Group 0 Protection

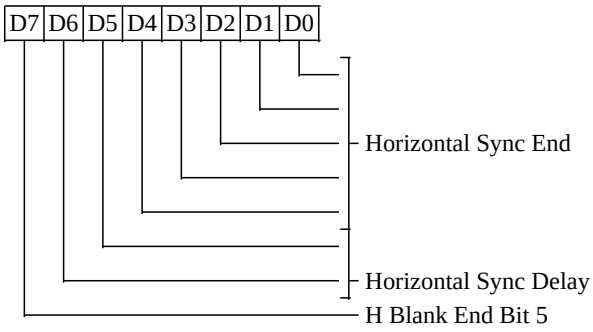


This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

7-0 Horizontal Sync Start

These bits specify the beginning of HSync in terms of Character clocks from the beginning of the display scan. These bits also determine display centering on the screen.

HORIZONTAL SYNC END REGISTER (CR05)
Read/Write at I/O Address 3B5h/3D5h
Index 05h
Group 0 Protection



This register is used for all VGA and EGA modes. It is also used for 640 column CGA modes and MDA/Hercules text mode. In all 320 column CGA modes and Hercules graphics mode, the alternate register is used.

4-0 Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of Horizontal Sync. If the horizontal sync width desired is N clocks, then these bits = (N + contents of CR04) and 1Fh.

6-5 Horizontal Sync Delay

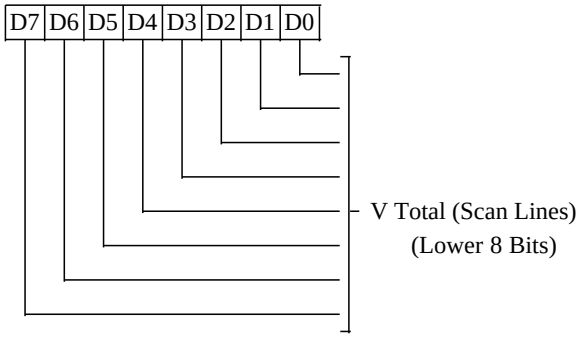
These bits specify the number of character clocks that the Horizontal Sync is delayed to compensate for internal pipeline delays.

7 Horizontal Blank End Bit 5

This bit is the sixth bit of the Horizontal Blank End Register (CR03).

VERTICAL TOTAL REGISTER (CR06)

Read/Write at I/O Address 3B5h/3D5h
Index 06h
Group 0 Protection



This register is used in all modes.

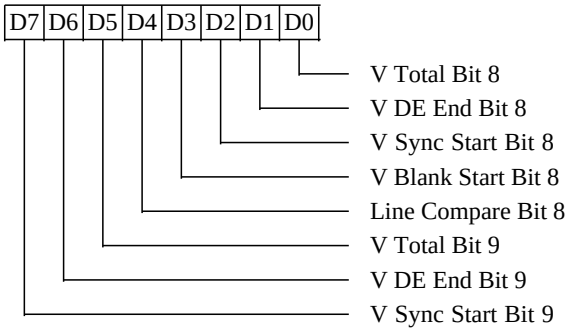
7-0 Vertical Total

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow Register. The Vertical Total value specifies the total number of scan lines (horizontal retrace periods) per frame.

Programmed Count = Actual Count – 2

OVERFLOW REGISTER (CR07)

Read/Write at I/O Address 3B5h/3D5h
Index 07h
Group 0 Protection on bits 0-3 and bits 5-7
Group 3 Protection on bit 4



This register is used in all modes.

0 Vertical Total Bit 8

1 Vertical Display Enable End Bit 8

2 Vertical Sync Start Bit 8

3 Vertical Blank Start Bit 8

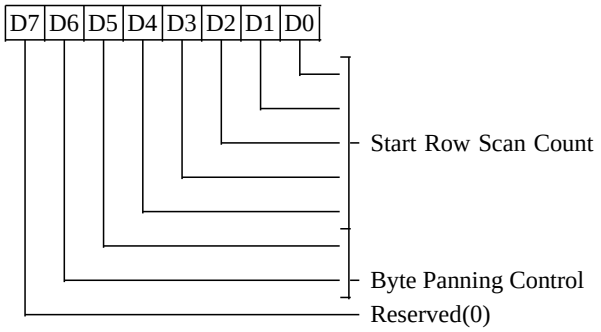
4 Line Compare Bit 8

5 Vertical Total Bit 9

6 Vertical Display Enable End Bit 9

7 Vertical Sync Start Bit 9

PRESET ROW SCAN REGISTER (CR08)
Read/Write at I/O Address 3B5h/3D5h
Index 08h
Group 3 Protection



4-0 Start Row Scan Count

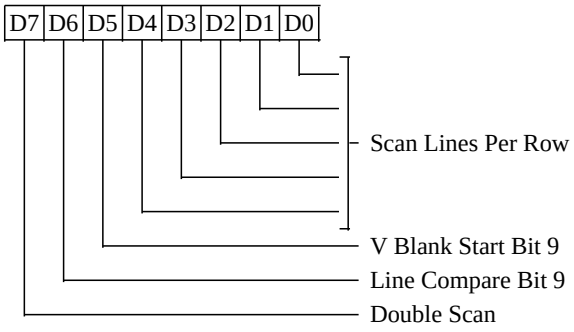
These bits specify the starting row scan count after each vertical retrace. Every horizontal retrace increments the character row scan line counter. The horizontal row scan counter is cleared at maximum row scan count during active display. This register is used for soft scrolling in text modes.

6-5 Byte Panning Control

These bits specify the lower order bits for the display start address. They are used for horizontal panning in Odd/Even and Quad modes.

7 Reserved (0)

MAXIMUM SCAN LINE REGISTER (CR09)
Read/Write at I/O Address 3B5h/3D5h
Index 09h
Group 2 Protection on bits 0-4
Group 4 Protection on bits 5-7



4-0 Scan Lines Per Row

These bits specify the number of scan lines in a row:

Programmed Value = Actual Value – 1

5 Vertical Blank Start Register Bit 9

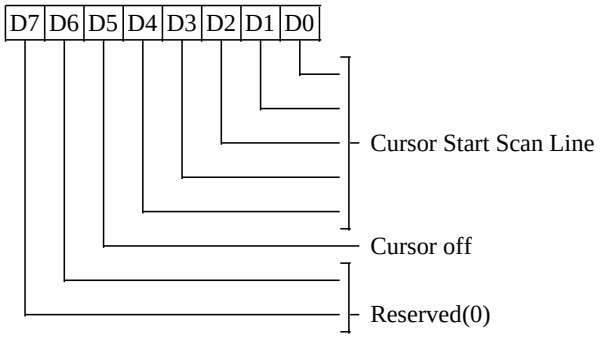
6 Line Compare Register Bit 9

7 Double Scan

0 NormalOperation
1 Enable scan line doubling

The vertical parameters in the CRT Controller (even for a split screen) are not affected, only the CRTC row scan counter (bits 0-4 of this register) and display memory addressing screen refresh are affected.

CURSOR START SCAN LINE REGISTER CR0A)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ah
Group 2 Protection



4-0 Cursor Start Scan Line

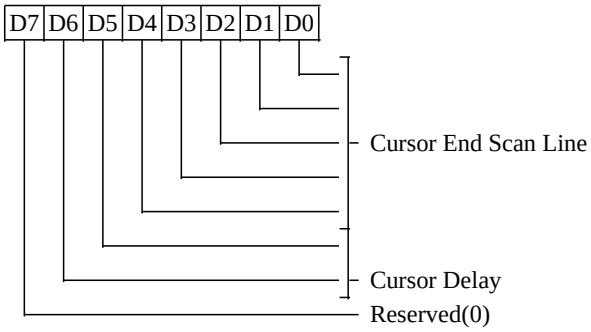
These bits specify the scan line of the character row where the cursor display begins.

5 Cursor Off

0 Text Cursor On
1 Text Cursor Off

7-6 Reserved (0)

CURSOR END SCAN LINE REGISTER (CR0B)
Read/Write at I/O Address 3B5h/3D5h
Index 0Bh
Group 2 Protection



4-0 Cursor End Scan Line

These bits specify the scan line of a character row where the cursor display ends (i.e., last scan line for the block cursor):

Programmed Value = Actual Value + 1

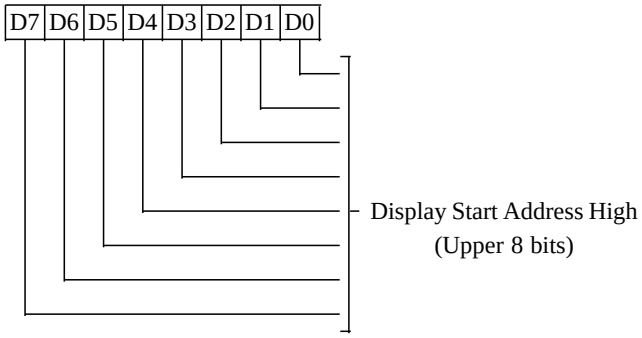
6-5 Cursor Delay

These bits define the number of character clocks that the cursor is delayed to compensate for internal pipeline delay.

7 Reserved (0)

Note: If the Cursor Start Line is greater than the Cursor End Line, then no cursor is generated.

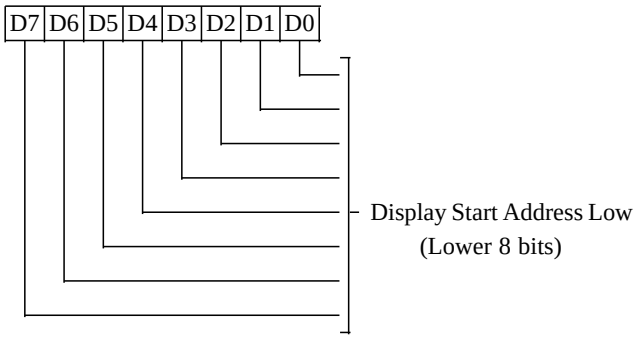
START ADDRESS HIGH REGISTER (CR0C)
Read/Write at I/O Address 3B5h/3D5h
Index 0Ch



7-0 Display Start Address High

This register contains the upper 8 bits of the display start address. In CGA / MDA / Hercules modes, this register wraps around at the 16K, 32K, and 64KByte boundaries respectively.

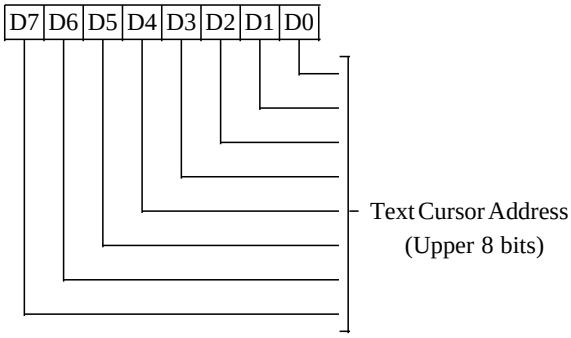
START ADDRESS LOW REGISTER (CR0D)
Read/Write at I/O Address 3B5h/3D5h
Index 0Dh



7-0 Display Start Address Low

This register contains the lower 8 bits of the display start address. The display start address points to the memory address corresponding to the top left corner of the screen.

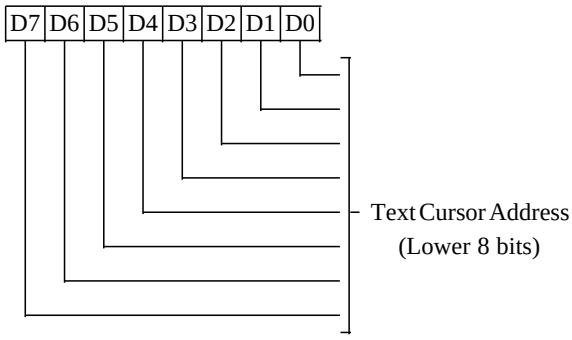
CURSOR LOCATION HIGH REGISTER (CR0E)
Read/Write at I/O Address 3B5h/3D5h
Index 0Eh



7-0 Text Cursor Location High

This register contains the upper 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64KByte boundaries respectively.

CURSOR LOCATION LOW REGISTER (CR0F)
Read/Write at I/O Address 3B5h/3D5h
Index 0Fh



7-0 Text Cursor Location Low

This register contains the lower 8 bits of the memory address where the text cursor is active. In CGA / MDA / Hercules modes, this register wraps around at 16K, 32K, and 64KByte boundaries respectively.

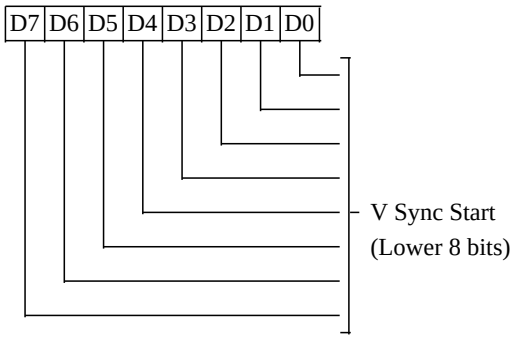
LIGHTPEN HIGH REGISTER (CR10)
Read only at I/O Address 3B5h/3D5h
Index 10h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

LIGHTPEN LOW REGISTER (CR11)
Read only at I/O Address 3B5h/3D5h
Index 11h

Read-only Register loaded at line compare (the light pen flip-flop is not implemented). Effective only in MDA and Hercules modes or when CR03 bit-7 = 0.

VERTICAL SYNC START REGISTER (CR10)
Read/Write at I/O Address 3B5h/3D5h
Index 10h
Group 4 Protection

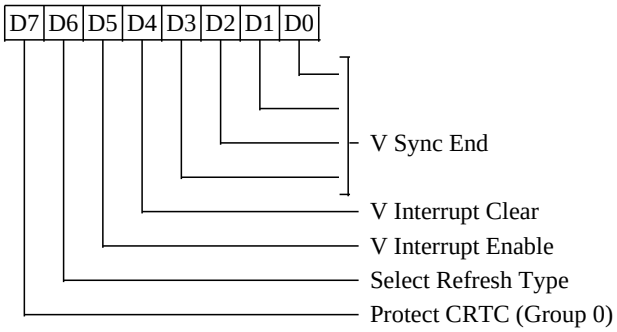


This register is used in all modes. This register is not readable in (Line Compare bit-9) MDA/Hercules emulation or when CR03 bit-7=1.

7-0 Vertical Sync Start

The eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRTC Overflow Register. They define the scan line position at which Vertical Sync becomes active.

VERTICAL SYNC END REGISTER (CR11)
Read/Write at I/O Address 3B5h/3D5h
Index 11h
Group 3 Protection for bits 4 and 5
Group 4 Protection for bits 0-3, 6, and 7



This register is used in all modes. This register is not readable in MDA/Hercules emulation or when CR03 bit-7=1.

3-0 Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. If the vertical sync width desired is N lines, then bits 3-0 of this register = (CR10 + N) AND 0Fh.

4 Vertical Interrupt Clear

0=Clear vertical interrupt generated on the IRQ output; 1=Normal operation. This bit is cleared by RESET.

5 Vertical Interrupt Enable

0 Enable vertical interrupt (default)
1 Disable vertical interrupt

This bit is cleared by RESET.

6 Select Refresh Type (Ignored)

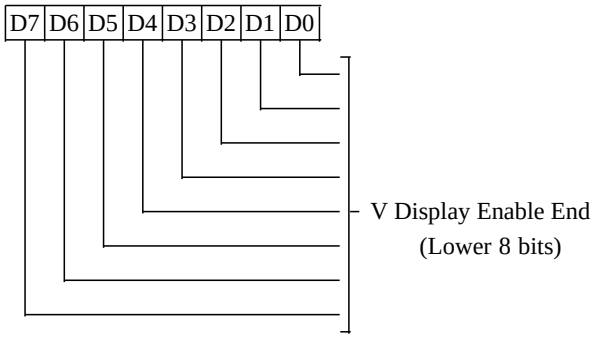
7 Group Protect 0

This bit is logically ORed with XR15 bit-6 to determine the protection for group 0 registers. This bit is cleared by RESET.

0 Enable writes to CR00-CR07
1 Disable writes to CR00-CR07

CR07 bit-4 (Line Compare bit-9) is not affected by this bit.

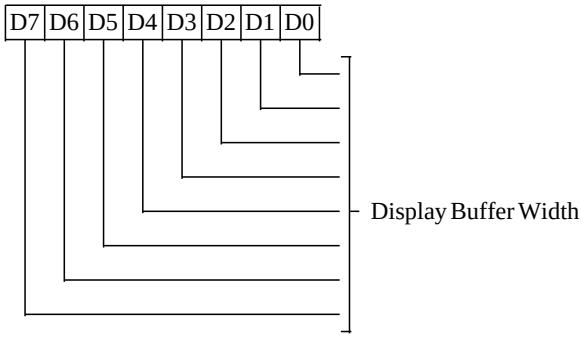
VERTICAL DISPLAY ENABLE END REGISTER (CR12)
Read/Write at I/O Address 3B5h/3D5h
Index 12h
Group 4 Protection



7-0 Vertical Display Enable End

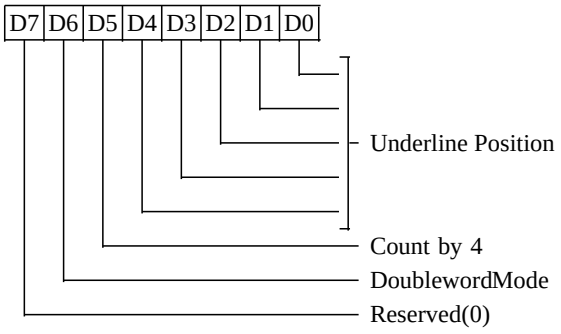
These are the eight low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow register. The actual count = Contents of this register + 1.

OFFSET REGISTER (CR13)
Read/Write at I/O Address 3B5h/3D5h
Index 13h
Group 3 Protection



7-0 Display Buffer Width. The byte starting address of the next display row = Byte Start Address for current row + K* (CR13 + Z/2), where Z = bit defined in XR0D, K = 2 in byte mode, and K = 4 in word mode. Byte, word and double word mode is selected by bit-6 of CR17 and bit-6 of CR14. A less significant bit than bit-0 of this register is defined in the Auxiliary Offset register (XR0D). This allows finer resolution of the bit map width. Byte, word and doubleword mode affects the translation of the 'logical' display memory address to the 'physical' display memory address.

UNDERLINE LOCATION REGISTER (CR14)
Read/Write at I/O Address 3B5h/3D5h
Index 14h
Group 3 Protection



4-0 Underline Position

These bits specify the underline's scan line position within a character row.

Programmed Value = Actual scan line number – 1

5 Count by 4 for Doubleword Mode

0 Frame Buffer Address is incremented by 1 or 2
1 Frame Buffer Address is incremented by 4 or 2

See CR17 bit-3 for further details.

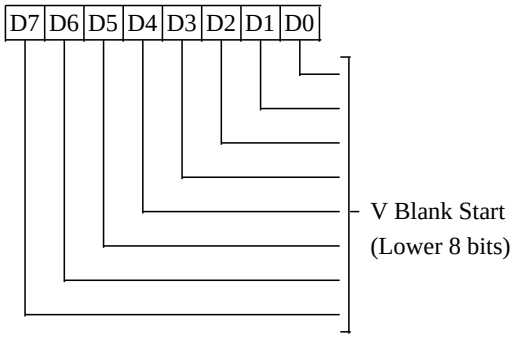
6 Doubleword Mode

0 Frame Buffer Address is byte or word address
1 Frame Buffer Address is doubleword address

This bit is used in conjunction with CR17 bit-6 to select the display memory addressing mode.

7 Reserved (0)

VERTICAL BLANK START REGISTER (CR15)
Read/Write at I/O Address 3B5h/3D5h
Index 15h
Group 4 Protection

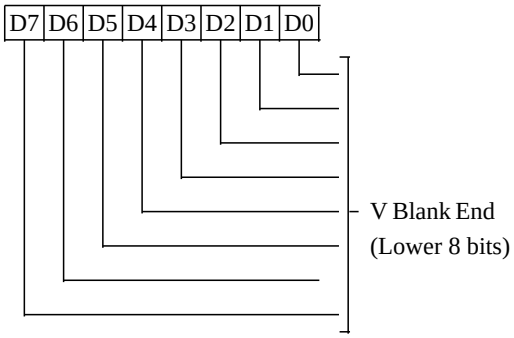


This register is used in all modes.

7-0 Vertical Blank Start

These are the 8 low order bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers respectively. Together these 10 bits define the scan line position where vertical blank begins. The interval between the end of the vertical display and the beginning of vertical blank is the bottom border on the screen.

VERTICAL BLANK END REGISTER (CR16)
Read/Write at I/O Address 3B5h/3D5h
Index 16h
Group 4 Protection

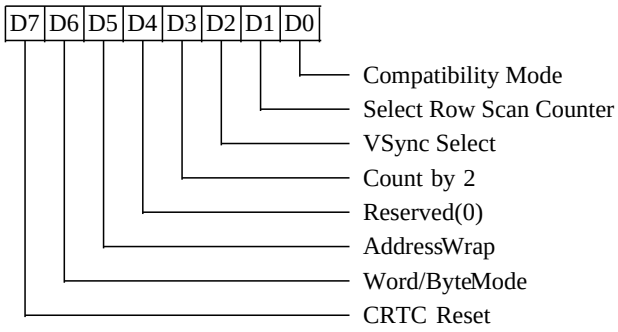


This register is used in all modes.

7-0 Vertical Blank End

These are the 8 low order bits of the scan line count which specifies the end of Vertical Blank. If the vertical blank width desired is Z lines these bits = (Vertical Blank Start + Z) and 0FFh.

CRT MODE CONTROL REGISTER (CR17)
Read/Write at I/O Address 3B5h/3D5h
Index 17h
Group 3 Protection for bits 0, 1, and 3-7
Group 4 Protection for bit 2



0 Compatibility Mode Support

This bit allows compatibility with the IBM CGA two-bank graphics mode.

0 Character row scan line counter bit 0 is substituted for memory address bit 13 during active display time
1 Normal operation, no substitution takes place

1 Select Row Scan Counter

This bit allows compatibility with Hercules graphics and with any other 4-bank graphics system.

0 Character row scan line counter bit 1 is substituted for memory address bit 14 during active display time
1 Normal operation, no substitution takes place

2 Vertical Sync Select

This bit controls the vertical resolution of the CRT Controller by permitting selection of the clock rate input to the vertical counters. When set to 1, the vertical counters are clocked by the horizontal retrace clock divided by 2.

3 Count By Two

0 Memory address counter is incremented every character clock
1 Memory address counter is incremented every two character clocks, used in conjunction with bit 5 of 0Fh.

Note: This bit is used in conjunction with CR14 bit-5. The net effect is as follows:

CR14 Bit-5	CR17 Bit-3	Increment Addressing Every
0	0	1 CCLK
0	1	2 CCLK
1	0	4 CCLK
1	1	2 CCLK

Note: In Hercules graphics and Hi-res CGA modes, address increments every two clocks.

4 Reserved (0)

5 AddressWrap (effective only in word mode)

0 Wrap display memory address at 16 KBytes. Used in IBM CGA mode.
1 Normal operation (extended mode).

6 Word Mode or Byte Mode

0 Select Word Mode. In this mode the display memory address counter bits are shifted down by one, causing the most-significant bit of the counter to appear on the least-significant bit of the display memory address output
1 Select byte mode

Note: This bit is used in conjunction with CR14 bit-6 to select byte, word, or double word memory addressing as follows:

CR14 Bit-6	CR17 Bit-6	Addressing Mode
0	0	Word Mode
0	1	Byte Mode
1	0	Double Word Mode
1	1	Double Word Mode

Display memory addresses are affected as shown in the table on the following page.

7 CRTC Reset

0 Force HSYNC and VSYNC inactive. No other registers or outputs affected.
1 Normal Operation

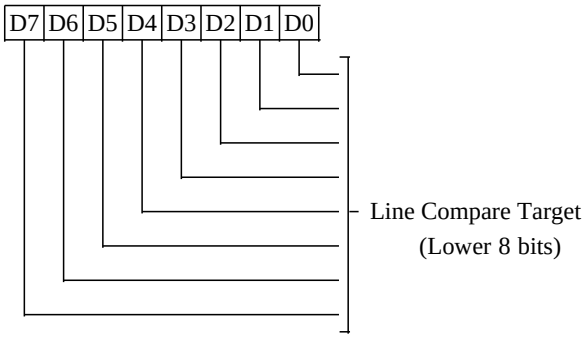
This bit is cleared by RESET.

Display memory addresses are affected by CR17 bit 6 as shown in the table below:

Logical Memory Address	Physical Memory Address Byte Mode	Word Mode	DoubleWord Mode
MA00	A00	Note 1	Note 2
MA01	A01	A00	Note 3
MA02	A02	A01	A00
MA03	A03	A02	A01
MA04	A04	A03	A02
MA05	A05	A04	A03
MA06	A06	A05	A04
MA07	A07	A06	A05
MA08	A08	A07	A06
MA09	A09	A08	A07
MA10	A10	A09	A08
MA11	A11	A10	A09
MA12	A12	A11	A10
MA13	A13	A12	A11
MA14	A14	A13	A12
MA15	A15	A14	A13

Note 1 = A13 * NOT CR17 bit 5
+ A15 * CR17 bit 5
Note 2 = A12 xor (A14 * XR04 bit 2)
Note 3 = A13 xor (A15 * XR04 bit 2)

LINE COMPARE REGISTER (CR18)
Read/Write at I/O Address 3B5h/3D5h
Index 18h
Group 3 Protection

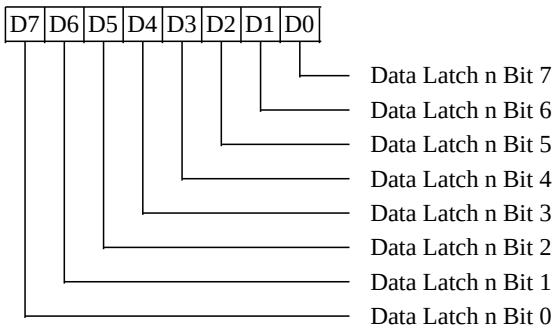


7-0 Line Compare Target

These are the low order 8 bits of a 10-bit register. The 9th and 10th bits are located in the CRT Controller Overflow and Maximum Scan Line Registers, respectively. This register is used to implement a split screen function. When the scan line counter value is equal to the contents of this register, the memory address counter is cleared to 0. The display memory address counter then sequentially addresses the display memory starting at address 0. Each subsequent row address is generated by the addition of the Offset Register contents. This register is not affected by the double scanning bit (CR09 bit 7).

MEMORY DATA LATCH REGISTER (CR22)

Read only at I/O Address 3B5h/3D5h
Index 22h



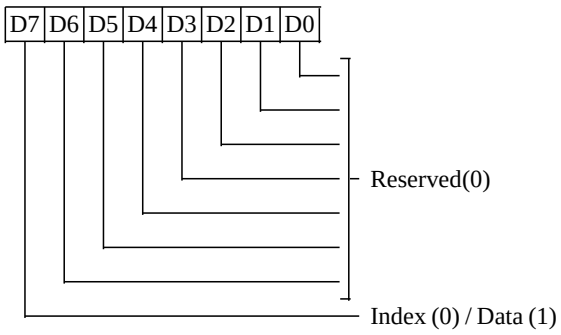
This register may be used to read the state of Graphics Controller Memory Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR04 bits 0–1) and is in the range 0–3.

Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

ATTRIBUTE CONTROLLER TOGGLE REGISTER (CR24)

Read only at I/O Address 3B5h/3D5h
Index 24h



6-0 Reserved (0)

7 Index/Data

This bit may be used to read back the state of the attribute controller index/data latch. This latch indicates whether the next write to the attribute controller at 3C0h will be to the register index pointer or to an indexed register.

0 Next write is to the index
1 Next write is to an indexed register

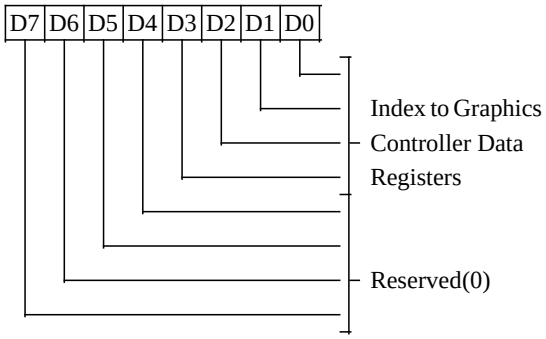
Writes to this register are not decoded and will be ignored.

This is a standard VGA register which was not documented by IBM.

Graphics Controller Registers

Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
GRX	Graphics Index	–	R/W	3CEh	1	81
GR00	Set/Reset	00h	R/W	3CFh	1	81
GR01	Enable Set/Reset	01h	R/W	3CFh	1	82
GR02	Color Compare	02h	R/W	3CFh	1	82
GR03	Data Rotate	03h	R/W	3CFh	1	83
GR04	Read Map Select	04h	R/W	3CFh	1	83
GR05	Graphics mode	05h	R/W	3CFh	1	84
GR06	Miscellaneous	06h	R/W	3CFh	1	86
GR07	Color Don't Care	07h	R/W	3CFh	1	86
GR08	Bit Mask	08h	R/W	3CFh	1	87

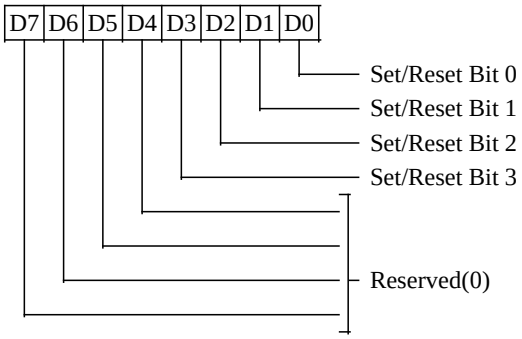
GRAPHICS CONTROLLER INDEX REGISTER (GRX)
Write only at I/O Address 3CEh
Group 1 Protection



3-0 4-bit Index to Graphics Controller Registers

7-4 Reserved (0)

SET/RESET REGISTER (GR00)
Read/Write at I/O Address 3CFh
Index 00h
Group 1 Protection



The SET/RESET and ENABLE SET/RESET registers are used to 'expand' 8 bits of CPU data to 32 bits of display memory.

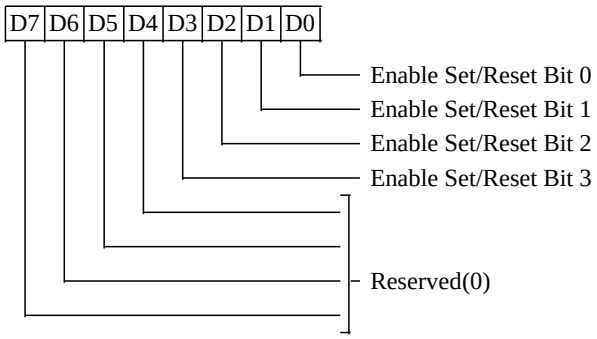
3-0 Set / Reset Planes 3-0

When the Graphics Mode register selects Write Mode 0, all 8 bits of each display memory plane are set as specified in the corresponding bit in this register. The Enable Set/Reset register (GR01) allows selection of some of the source of data to be written to individual planes. In Write Mode 3 (see GR05), these bits determine the color value.

7-4 Reserved (0)

ENABLE SET/RESET REGISTER (GR01)

Read/Write at I/O Address 3CFh
Index 01h
Group 1 Protection



3-0 Enable Set / Reset Planes 3-0

This register works in conjunction with the Set/Reset register (GR00). The Graphics Mode register must be programmed to Write Mode 0 in order for this register to have any effect.

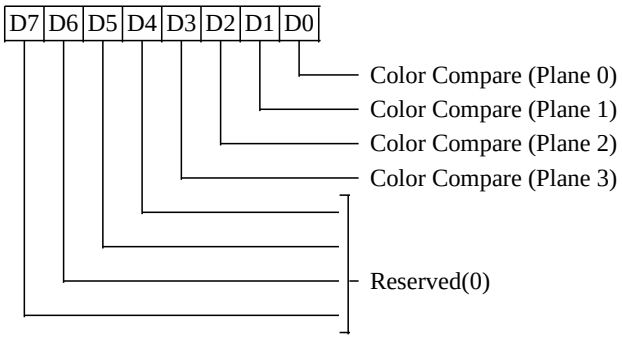
0 The corresponding plane is written with the data from the CPU data bus

1 The corresponding plane is set to 0 or 1 as specified in the Set/Reset Register

7-4 Reserved (0)

COLOR COMPARE REGISTER (GR02)

Read/Write at I/O Address 3CFh
Index 02h
Group 1 Protection



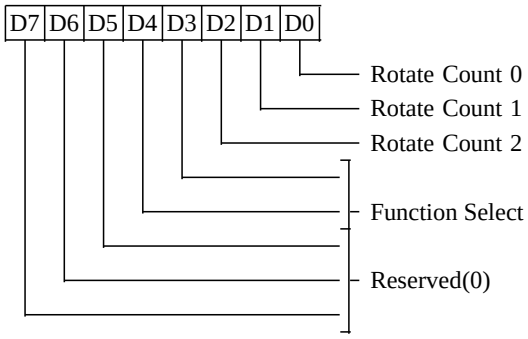
3-0 Color Compare Planes 3-0

This register is used to 'reduce' 32 bits of memory data to 8 bits for the CPU in 4-plane graphics mode. These bits provide a reference color value to compare to data read from display memory planes 0-3. The Color Don't Care register (GR07) is used to affect the result. This register is active only if the Graphics Mode register (GR05) is set to Read Mode 1. A match between the memory data and the Color Compare register (GR02) (for the bits specified in the Color Don't Care register) causes a logical 1 to be placed on the CPU data bus for the corresponding data bit; a mis-match returns a logical 0.

7-4 Reserved (0)

DATA ROTATE REGISTER (GR03)

Read/Write at I/O Address 3CFh
Index 03h
Group 1 Protection



2-0 Data Rotate Count

These bits specify the number of bits to rotate to the right the data being written by the CPU. The CPU data bits are first rotated, then subjected to the logical operation as specified in the Function Select bit field. The rotate function is active only if the Graphics Mode register is programmed for Write Mode 0.

4-3 Function Select

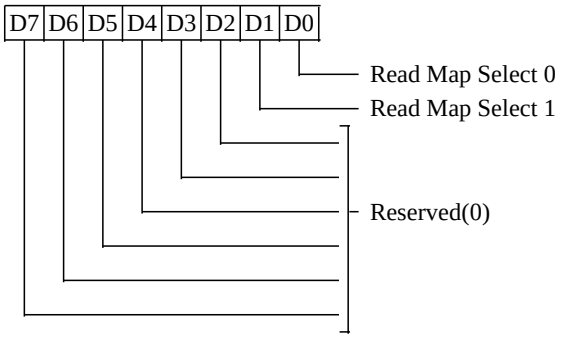
These Function Select bits specify the logical function performed on the contents of the processor latches (loaded on a previous CPU read cycle) before the data is written to display memory. These bits operate as follows:

Bit 4	Bit 3	Result
0	0	No change to the Data
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

7-5 Reserved (0)

READ MAP SELECT REGISTER (GR04)

Read/Write at I/O Address 3CFh
Index 04h
Group 1 Protection



1-0 Read Map Select

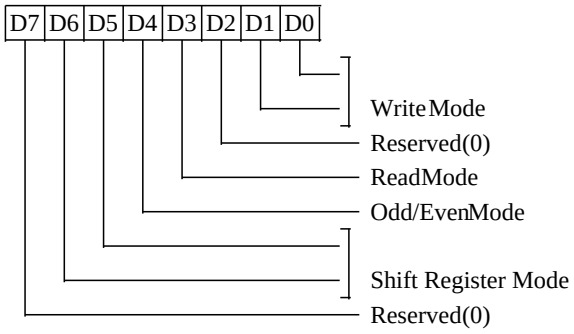
This register is also used to 'reduce' 32 bits of memory data to 8 bits for the CPU in the 4-plane graphics mode. These bits select the memory plane from which the CPU reads data in Read Mode 0. In Odd/Even mode, bit-0 is ignored. In Quad mode, bits 0 and 1 are both ignored.

The four memory maps are selected as follows:

Bit 1	Bit 0	MapSelected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

7-2 Reserved (0)

GRAPHICS MODE REGISTER (GR05)
Read/Write at I/O Address 3CFh
Index 05h
Group 1 Protection



1-0 Write Mode

For 16-bit writes, the operation is repeated on the lower and upper bytes of CPU data.

1	0	Write Mode
0	0	**Write mode 0**. Each of the four display memory planes is written with the CPU data rotated by the number of counts in the Rotate Register, except when the Set/Reset Register is enabled for any of the four planes. When the Set/Reset Register is enabled, the corresponding plane is written with the data stored in the Set/Reset Register.
0	1	**Write mode 1**. Each of the four display memory planes is written with the data previously loaded in the processor latches. These latches are loaded during all read operations.
1	0	**Write mode 2**. The CPU data bus data is treated as the color value for the addressed byte in planes 0-3. All eight pixels in the addressed byte are modified unless protected by the Bit Mask register setting. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset and Enable Set/Reset registers are ignored. The Function Select bits in the Data Rotate register are used.
1	1	**Write mode 3**. The CPU data is rotated then logically ANDed with the contents of the Bit Mask register (GR08) and then treated as the addressed data's bit mask, while the contents of the Set/Reset register is treated as the color value. A '0' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the corresponding pixel in the processor latches. A '1' on the data bus (mask) causes the corresponding pixel in the addressed byte to be set to the color value specified in the Set/Reset register. The Enable Set/Reset register is ignored. The Data Rotate is used. This write mode can be used to fill an area with a single color and pattern.

2 Reserved (0)

3 Read Mode

0 The CPU reads data from one of the planes as selected in the Read Map Select register.

1 The CPU reads the 8-bit result of the logical comparison between all eight pixels in the four display planes and the contents of the Color Compare and Color Don't Care registers. The CPU reads a logical 1 if a match occurs for each pixel and logical 0 if a mis-match occurs. In 16-bit read cycles, this operation is repeated on the lower and upper bytes.

(Continued on following page)

4 Odd/Even Mode

0 All CPU addresses sequentially access all planes

1 Even CPU addresses access planes 0 and 2, while odd CPU addresses access planes 1 and 3. This option is useful for compatibility with the IBM CGA memory organization.

6-5 Shift Register Mode

These two bits select the data shift pattern used when passing data from the four memory planes through the four video shift registers. If data bits 0-7 in memory planes 0-3 are represented as M0D0-M0D7, M1D0-M1D7, M2D0-M2D7, and M3D0-M3D7 respectively, then the data in the serial shift registers is shifted out as follows:

65	Last Bit Shifted Out			Shift Direction →				1st Bit Shifted Out	Output to:
00:	M0D0	M0D1	M0D2	M0D3	M0D4	M0D5	M0D6	M0D7	Bit 0
	M1D0	M1D1	M1D2	M1D3	M1D4	M1D5	M1D6	M1D7	Bit 1
	M2D0	M2D1	M2D2	M2D3	M2D4	M2D5	M2D6	M2D7	Bit 2
	M3D0	M3D1	M3D2	M3D3	M3D4	M3D5	M3D6	M3D7	Bit 3
01:	M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	Bit 0
	M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	Bit 1
	M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	Bit 2
	M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	Bit 3
1x:	M3D0	M3D4	M2D0	M2D4	M1D0	M1D4	M0D0	M0D4	Bit 0
	M3D1	M3D5	M2D1	M2D5	M1D1	M1D5	M0D1	M0D5	Bit 1
	M3D2	M3D6	M2D2	M2D6	M1D2	M1D6	M0D2	M0D6	Bit 2
	M3D3	M3D7	M2D3	M2D7	M1D3	M1D7	M0D3	M0D7	Bit 3

Note: If the Shift Register is not loaded every character clock (see SR01 bits 2&4) then the four 8-bit shift registers are effectively 'chained' with the output of shift register 1 becoming the input to shift register 0 and so on. This allows one to have a large monochrome (or 4 color) bit map and display one portion thereof.

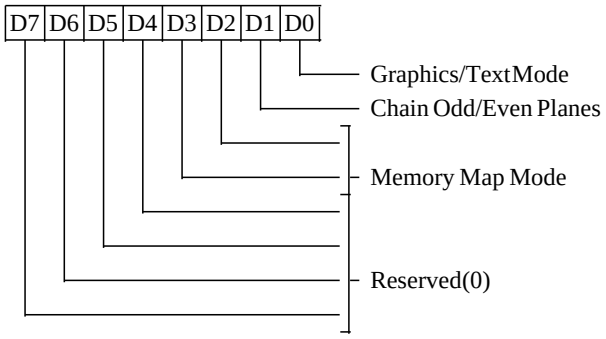
Note: If XR28 bit-4 is set (8-bit video path), GR05 bit-6 must be set to 0:

0x and XR28 bit-4=1:	M3D0	M2D0	M1D0	M0D0	Bit 0
	M3D1	M2D1	M1D1	M0D1	Bit 1
	M3D2	M2D2	M1D2	M0D2	Bit 2
	M3D3	M2D3	M1D3	M0D3	Bit 3
	M3D4	M2D4	M1D4	M0D4	Bit 4
	M3D5	M2D5	M1D5	M0D5	Bit 5
	M3D6	M2D6	M1D6	M0D6	Bit 6
	M3D7	M2D7	M1D7	M0D7	Bit 7

7 Reserved (0)

MISCELLANEOUS REGISTER (GR06)

Read/Write at I/O Address 3CFh
Index 06h
Group 1 Protection



0 Graphics/Text Mode

0 TextMode
1 Graphics mode

1 Chain Odd/Even Planes

This mode can be used to double the address space into display memory.

1 CPU address bit A0 is replaced by a higher order address bit. The state of A0 determines which memory plane is to be selected:

A0 = 0: select planes 0 and 2
A0 = 1: select planes 1 and 3

0 A0 not replaced

3-2 Memory Map Mode

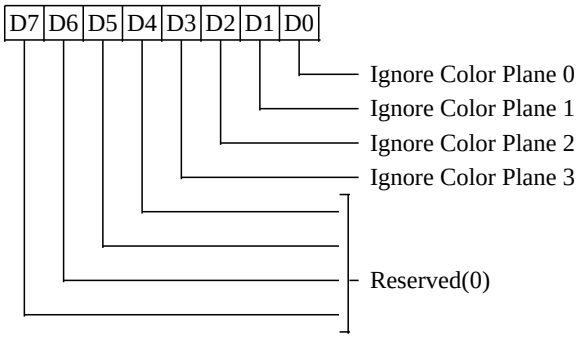
These bits control the mapping of the display memory into the CPU address space as follows (also used in extended modes):

Bit 3	Bit 2	CPU Address
0	0	A0000h-BFFFFh
0	1	A0000h-AFFFFh
1	0	B0000h-B7FFFh
1	1	B8000h-BFFFFh

7-4 Reserved (0)

COLOR DON'T CARE REGISTER (GR07)

Read/Write at I/O Address 3CFh
Index 07h
Group 1 Protection



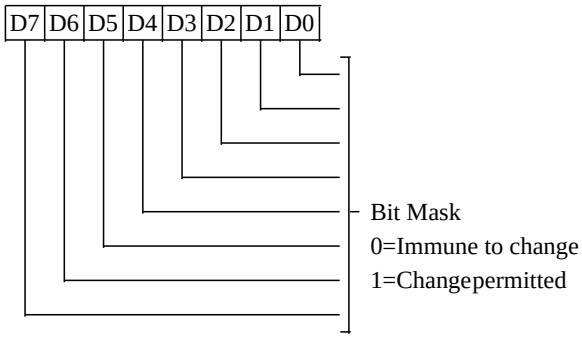
3-0 Ignore Color Plane (3-0)

0 This causes the corresponding bit of the Color Compare register to be a don't care during a comparison.

1 The corresponding bit of the Color Compare register is enabled for color comparison. This register is active in Read Mode 1 only.

7-4 Reserved (0)

BIT MASK REGISTER (GR08)
Read/Write at I/O Address 3CFh
Index 08h
Group 1 Protection



7-0 Bit Mask

This bit mask is applicable to any data written by the CPU, including that subject to a rotate, logical function (AND, OR, XOR), Set/Reset, and No Change. In order to execute a proper read-modify-write cycle into displayed memory, each byte must first be read (and latched by the VGA), the Bit Mask register set, and the new data then written. The bit mask applies to all four planes simultaneously.

0 The corresponding bit in each of the four memory planes is written from the corresponding bit in the latches

1 Unrestricted manipulation of the corresponding data bit in each of the four memory planes is permitted

Attribute Controller and VGA Color Palette Registers

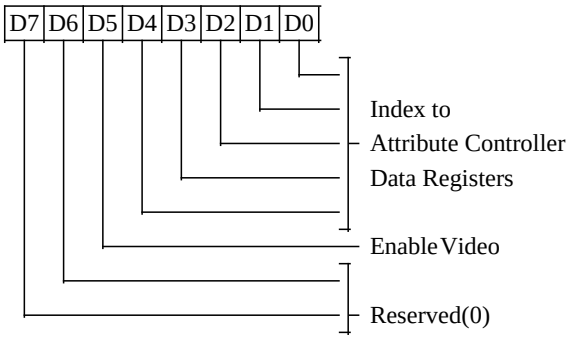
Register Mnemonic	Register Name	Index	Access	I/O Address	Protect Group	Page
ARX	Attribute Index (for 3C0/3C1h)	–	R/W	3C0h	1	89
AR00-AR0F	Attribute Controller Color Data	00-0Fh	R/W	3C0h/3C1h	1	90
AR10	Mode Control	10h	R/W	3C0h/3C1h	1	90
AR11	Overscan Color	11h	R/W	3C0h/3C1h	1	91
AR12	Color Plane Enable	12h	R/W	3C0h/3C1h	1	91
AR13	Horizontal Pixel Panning	13h	R/W	3C0h/3C1h	1	92
AR14	Pixel Pad	14h	R/W	3C0h/3C1h	1	92
DACMASK	Color Palette Pixel Mask	–	R/W	3C6h	6	93
DACSTATE	Color Palette State	–	R	3C7h	–	93
DACRX	Color Palette Read-Mode Index	–	W	3C7h	6	94
DACX	Color Palette Index (for 3C9h)	–	R/W	3C8h	6	94
DACDATA	Color Palette Data	00-FFh	R/W	3C9h	6	94

In regular VGA mode, all Attribute Controller registers are located at the same byte address (3C0h) in the CPU I/O space. An internal flip-flop controls the selection of either the Attribute Index or Data Registers. To select the Index Register, an I/O Read is executed to address 3BAh/3DAh (Input Status Register 1) to clear this flip-flop. After the Index Register has been loaded by an I/O Write to address 3C0h, this flip-flop toggles, and the Data Register is ready to be accessed. Every I/O Write to address 3C0h toggles this flip-flop. The flip-flop does not have any effect on the reading of the Attribute Controller registers. The Attribute Controller index register is always read back at address 3C0h, the data register is always read back at address 3C1h.

An option is provided to allow the Attribute Controller Index register to be mapped to 3C0h and the Data register to 3C1h to allow word I/O accesses. Another option allows the Attribute Controller to be both read and written at either 3C0h or 3C1h (EGA compatible mode). These optional mappings are selected by 'CPU Interface Register 1' (XR02[4-3]) and are not standard VGA capabilities.

The VGA color palette is used to further modify the video color output following the attribute controller color registers. The color palette logic is contained on-chip; extension register XR06 is provided to control various optional capabilities. DAC logic is provided on-chip to convert the final video output of the color palette to analog RGB outputs for use in driving a CRT display. Output comparator logic is also provided on-chip to duplicate the SENSE function (see Status Register 0 readable at 3C2h).

ATTRIBUTE INDEX REGISTER (ARX)
Read/Write at I/O Address 3C0h
Group 1 Protection



4-0 Attribute Controller Index

These bits point to one of the internal registers of the Attribute Controller.

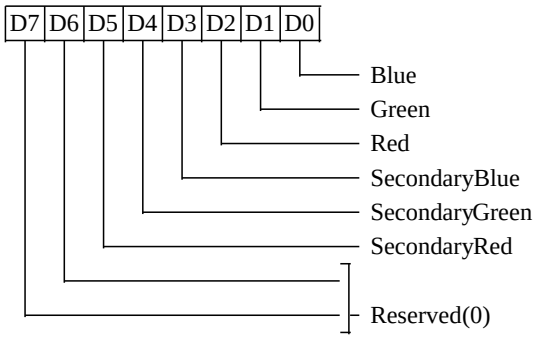
5 Enable Video

0 Disable video, allowing the Attribute Controller Color registers to be accessed by the CPU

1 Enable video, causing the Attribute Controller Color registers (AR00-AR0F) to be inaccessible to the CPU

7-6 Reserved (0)

ATTRIBUTE CONTROLLER COLOR REGISTERS (AR00-AR0F)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 00-0Fh
Group 1 Protection or XR63 bit-6

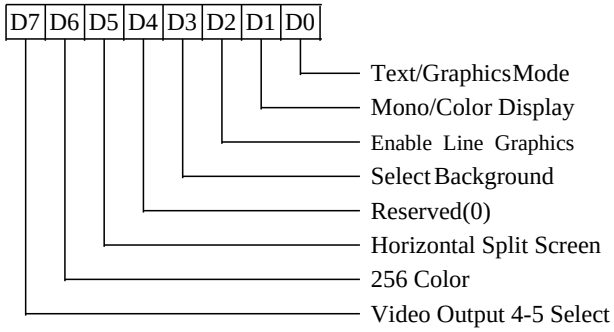


5-0 Color Value

These bits are the color value in the respective attribute controller color register as pointed to by the attribute index register.

7-6 Reserved (0)

ATTRIBUTE CONTROLLER MODE CONTROL REGISTER (AR10)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 10h
Group 1 Protection



0 Text/Graphics Mode

0 Select text mode
1 Select graphics mode

1 Monochrome/Color Display

0 Select color display attributes
1 Select mono display attributes

2 Enable Line Graphics Character Codes

This bit is dependent on bit 0 of the Override register.

0 Make the ninth pixel appear the same as the background

1 For special line graphics character codes (0C0h-0DFh), make the ninth pixel identical to the eighth pixel of the character. For other characters, the ninth pixel is the same as the background.

3 Enable Blink/Select Background Intensity

The blinking counter is clocked by the VSYNC signal. The Blink frequency is defined in the Blink Rate Control Register (XR60).

0 Disable Blinking and enable text mode background intensity

1 Enable the blink attribute in text and graphics modes.

4 Reserved (0)

5 Split Screen Horizontal Panning Mode

0 Scroll both screens horizontally as specified in the Pixel Panning register

1 Scroll horizontally only the top screen as specified in the Pixel panning register

6 256 Color Output Assembler

0 6-bits of video (translated from 4-bits by the internal color palette) are output every dot clock

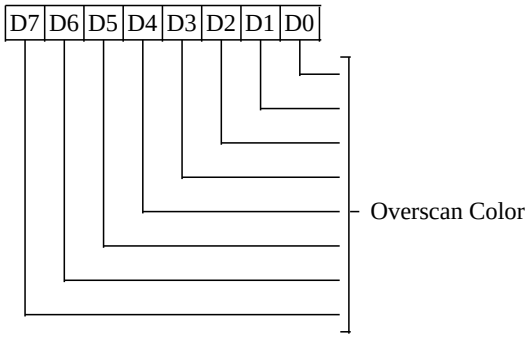
1 Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot clock (256 color mode).

7 Video Output 5-4 Select

0 Video bits 4 and 5 are generated by the internal Attribute Controller color paletteregisters

1 Video bits 4 and 5 are the same as bits 0 and 1 in the Pixel Pad register (AR14)

OVERSCAN COLOR REGISTER (AR11)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 11H
Group 1 Protection

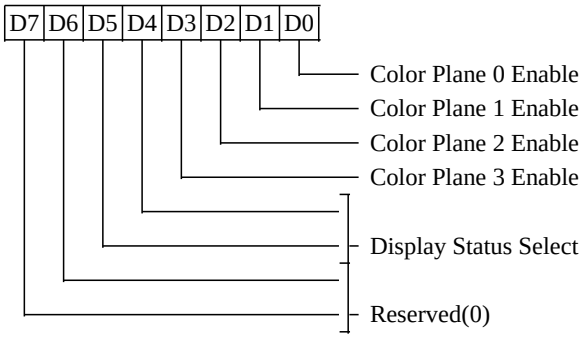


7-0 Overscan Color

These 8 bits define the overscan (border) color value. For monochrome displays, these bits should be zero.

The border color is displayed in the interval after Display Enable End and before Blank Start (end of display area; i.e. right side and bottom of screen) and between Blank End and Display Enable Start (beginning of display area; i.e. left side and top of screen).

COLOR PLANE ENABLE REGISTER (AR12)
Read at I/O Address 3C1h
Write at I/O Address 3C0/1h
Index 12h
Group 1 Protection



3-0 Color Plane (3-0) Enable

0 Force the corresponding color plane pixel bit to 0 before it addresses the colorpalette

1 Enable the plane data bit of the corresponding color plane to pass

5-4 Display Status Select

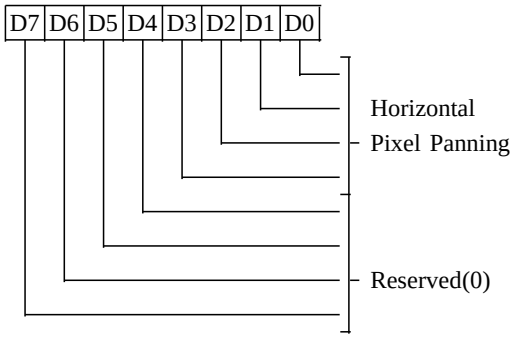
These bits select two of the eight color outputs to be read back in the Input Status Register 1 (port 3BAh or 3DAh). The output color combinations available on the status bits are as follows:

		Status Register 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

7-6 Reserved (0)

ATTRIBUTE CONTROLLER HORIZONTAL PIXEL PANNING REGISTER (AR13)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 13h
Group 1 Protection



3-0 Horizontal Pixel Panning

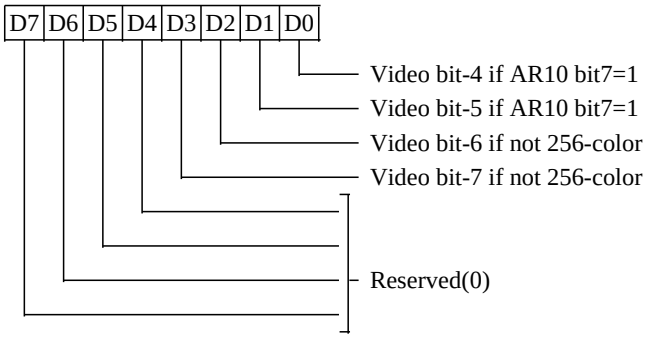
These bits select the number of pixels to shift the display horizontally to the left. Pixel panning is available in both text and graphics modes. In 9 pixel/character text mode, the output can be shifted a maximum of 9 pixels. In 8 pixel/character text mode and all graphics modes a maximum shift of 8 pixels is possible. In 256-color mode (output assembler AR10 bit-6 = 1), bit 0 of this register must be 0 which results in only 4 panning positions per display byte. In Shift Load 2 and Shift Load 4 modes, register CR08 provides single pixel resolution for panning. Panning is controlled as follows:

	Number of Pixels Shifted		
AR13	9-dot mode	8-dot mode	256-color mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

7-4 Reserved (0)

ATTRIBUTE CONTROLLER PIXEL PAD REGISTER (AR14)

Read at I/O Address 3C1h
Write At I/O Address 3C0/1h
Index 14h
Group 1 Protection



1-0 Video Bits 5-4

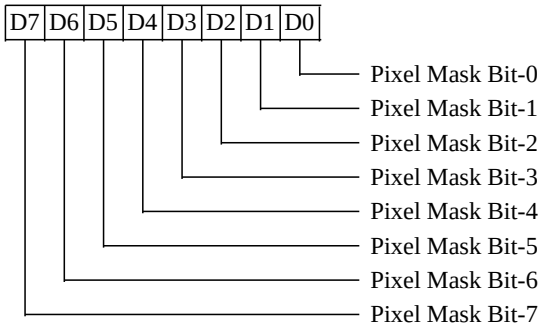
These bits are output as video bits 5 and 4 when AR10 bit-7 = 1. They are disabled in the 256 color mode.

3-2 Video Bits 7-6

These bits are output as video bits 7 and 6 in all modes except 256-color mode.

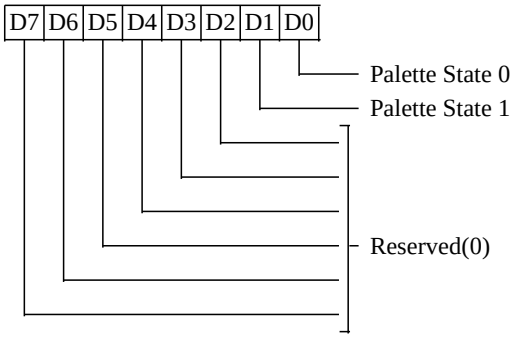
7-4 Reserved (0)

COLOR PALETTE
PIXEL MASK REGISTER (DACMASK)
Read/Write at I/O Address 3C6h
Group 6 Protection



The contents of this register are logically ANDed with the 8 bits of video data coming into the color palette. Zero bits in this register therefore cause the corresponding address input to the color palette to be zero. For example, if this register is programmed with 7, only color palette registers 0-7 would be accessible; video output bits 3-7 would be ignored and all color values would map into the lower 8 locations in the color palette.

COLOR PALETTE
STATE REGISTER (DACSTATE)
Read only at I/O Address 3C7h



1-0 Palette State 1-0

Status bits indicate the I/O address of the last CPU write to the Color Palette:

00 The last write was to 3C8h (write mode)

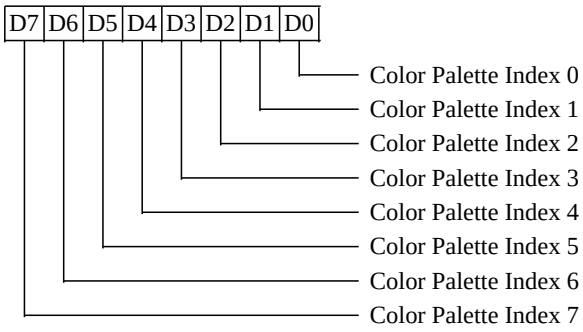
11 The last write was to 3C7h (read mode)

7-2 Reserved (0)

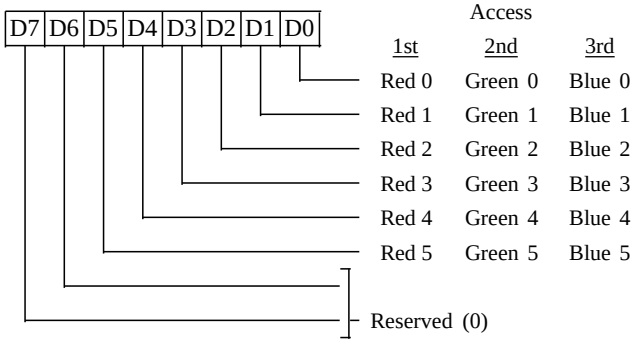
To allow saving and restoring the state of the video subsystem, this register is required since the color palette index register is automatically incremented differently depending on whether the index is written at 3C7h or 3C8h.

COLOR PALETTE
READ-MODE INDEX REGISTER (DACRX)
Write only at I/O Address 3C7h
Group 6 Protection

COLOR PALETTE
INDEX REGISTER (DACX)
Read/Write at I/O Address 3C8h
Group 6 Protection



COLOR PALETTE
DATA REGISTERS (DACDATA 00-FF)
Read/Write at I/O Address 3C9h Index 00h-FFh
Group 6 Protection



The palette index register is used to point to one of 256 palette data registers. Each data register is 18 bits in length (6 bits each for red, green, and blue), so the data values must be read as a sequence of 3 bytes. After writing the index register (3C7h or 3C8h), data values may be read from or written to the color palette data register port (3C9h) in sequence: first red, then green, then blue, then repeat for the next location if desired (the index is incremented automatically by the palette logic).

The index may be written at 3C7h and may be read or written at 3C8h. When the index value is written to either port, it is written to both the index register and a 'save' register. The save register (not the index register) is used by the palette logic to point at the current data register. When the index value is written to 3C7h (**readmode**), it is written to both the index register and the save register, then the index register is automatically incremented. When the index value is written to 3C8h (**writemode**), the automatic incrementing of the index register does not occur.

After the third of the three sequential data reads from (or writes to) 3C9h is completed, the save and index registers are both automatically incremented by the palette logic. This allows the entire palette (or any subset) to be read (written) by writing the index of the first color in the set, then sequentially reading (writing) the values for each color, without having to reload the index every three bytes.

The state of the RGB sequence is not saved; the user must access each three bytes in an uninterruptible sequence (or be assured that interrupt service routines will not access the palette index or data registers). When the index register is written (at either port), the RGB sequence is restarted. Data reads and writes may be intermixed; either reads or writes increment the palette logic's RGB sequence counter.

The palette's save register always contains a value one less than the readable index value if the last index write was to the 'read mode' port. The state is saved of which port (3C7h or 3C8h) was last written; that information is returned on reads from 3C7h.

Extension Registers

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XRX	--	Extension Index	--	R/W	3D6h	- x x x x x x x	97
XR00	Misc	Chip Version (65540: v=0; 65545: v=1)	00h	RO	3D7h	1 1 0 1 v r r r	97
XR01	Misc	Configuration	01h	RO	3D7h	d d d d d d d d	98
XR02	Misc	CPU Interface Control 1	02h	R/W	3D7h	0 0 0 0 0 0 0 0	99
XR03	Misc	CPU Interface Control 2	03h	R/W	3D7h	- - - - - - 0 x	100
XR04	Misc	Memory Control 1	04h	R/W	3D7h	- - 0 - - 0 0 0	101
XR05	Misc	Memory Control 2	05h	R/W	3D7h	0 0 0 0 0 0 0 0	102
XR06	Misc	Palette Control	06h	R/W	3D7h	0 0 0 0 0 0 0 0	103
XR0E	Misc	Text Mode Control	0Eh	R/W	3D7h	0 0 0 0 0 0 - -	106
XR28	Misc	Video Interface	28h	R/W	3D7h	0 0 0 0 - - 0 -	117
XR29	Misc	Half Line Compare	29h	R/W	3D7h	x x x x x x x x	117
XR70	Misc	Setup / Disable Control	70h	R/W	3D7h	0 - - - - - - -	150
XR72	Misc	External Device I/O	72h	R/W	3D7h	0 0 0 0 0 0 0 •	151
XR73	Misc	DPMS Control	73h	R/W	3D7h	0 0 - - 0 0 0 0	152
XR7D	Misc	Diagnostic (65545 Only)	7Dh	R/W	3D7h	0 - - - - - - -	152
XR7F	Misc	Diagnostic	7Fh	R/W	3D7h	0 0 x x x x 0 0	153
XR07	Mapping	I/O Base (65545 Only)	07h	R/W	3D7h	1 1 1 1 0 1 0 0	104
XR08	Mapping	Linear Addressing Base	08h	R/W	3D7h	x x x x x x x x	104
XR0B	Mapping	CPU Paging	0Bh	R/W	3D7h	- - 0 0 • 0 0 0	105
XR0C	Mapping	Start Address Top	0Ch	R/W	3D7h	- - - - - - x x	105
XR10	Mapping	Single/Low Map	10h	R/W	3D7h	x x x x x x x x	108
XR11	Mapping	High Map	11h	R/W	3D7h	x x x x x x x x	108
XR0F	Software Flags	Software Flags 0	0Fh	R/W	3D7h	x x x x x x x x	107
XR2B	Software Flags	Software Flags 1	2Bh	R/W	3D7h	0 0 0 0 0 0 0 0	118
XR44	Software Flags	Software Flags 2	44h	R/W	3D7h	x x x x x x x x	127
XR45	Software Flags	Software Flags 3	45h	R/W	3D7h	x x x x x x x x	127
XR14	Compatibility	Emulation Mode	14h	R/W	3D7h	0 0 0 0 h h 0 0	109
XR15	Compatibility	Write Protect	15h	R/W	3D7h	0 0 0 0 0 0 0 0	110
XR1F	Compatibility	Virtual EGA Switch	1Fh	R/W	3D7h	0 - - - x x x x	115
XR7E	Compatibility	CGA/Hercules Color Select	7Eh	R/W	3D7h	- - x x x x x x	153
XR30	Clock	Clock Divide Control	30h	R/W	3D7h	• • • • x x x x	121
XR31	Clock	Clock M-Divisor	31h	R/W	3D7h	• x x x x x x x	122
XR32	Clock	Clock N-Divisor	32h	R/W	3D7h	• x x x x x x x	122
XR33	Clock	Clock Control	33h	R/W	3D7h	0 0 0 0 • 0 0 0	123
XR3A	MultiMedia	Color Key 0	3Ah	R/W	3D7h	x x x x x x x x	124
XR3B	MultiMedia	Color Key 1	3Bh	R/W	3D7h	x x x x x x x x	124
XR3C	MultiMedia	Color Key 2	3Ch	R/W	3D7h	x x x x x x x x	125
XR3D	MultiMedia	Color Key Mask 0	3Dh	R/W	3D7h	x x x x x x x x	125
XR3E	MultiMedia	Color Key Mask 1	3Eh	R/W	3D7h	x x x x x x x x	126
XR3F	MultiMedia	Color Key Mask 2	3Fh	R/W	3D7h	x x x x x x x x	126
XR40	BitBLT	BitBLT Configuration (65545 Only)	40h	R/W	3D7h	- - - - - - x x	127

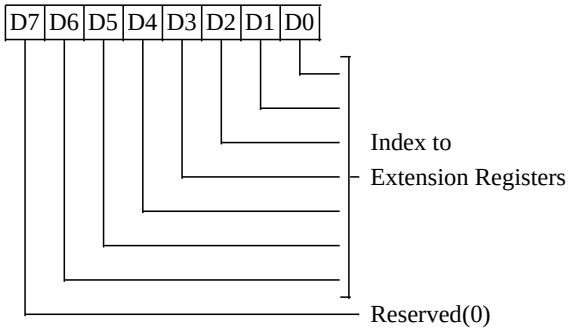
Reset Codes:
x = Not changed by reset (indeterminate on power-up)
d = Set from the corresponding data bus pin on trailing edge of reset
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0 or 1 by trailing edge of reset

Extension Registers (Continued)

Register Mnemonic	Register Group	Extension Register Name	Index	I/O Access	Address	State After Reset	Page
XR0D	Alternate	Auxiliary Offset	0Dh	R/W	3D7h	- - - - - - x x	106
XR16	Alternate	Vertical Overflow	16h	R/W	3D7h	• 0 • 0 • 0 0 0	111
XR17	Alternate	Horizontal Overflow	17h	R/W	3D7h	• 0 0 0 0 0 0 0	111
XR18	Alternate	Alternate Horizontal Display End	18h	R/W	3D7h	x x x x x x x x	112
XR19	Alternate	Alternate Horizontal Sync Start	19h	R/W	3D7h	x x x x x x x x	112
XR1A	Alternate	Alternate Horizontal Sync End	1Ah	R/W	3D7h	x x x x x x x x	113
XR1B	Alternate	Alternate Horizontal Total	1Bh	R/W	3D7h	x x x x x x x x	113
XR1C	Alternate	Alternate H Blank Start / H Panel Size	1Ch	R/W	3D7h	x x x x x x x x	114
XR1D	Alternate	Alternate Horizontal Blank End	1Dh	R/W	3D7h	0 x x x x x x x	114
XR1E	Alternate	Alternate Offset	1Eh	R/W	3D7h	x x x x x x x x	115
XR24	Alternate	Alternate Maximum Scan Line	24h	R/W	3D7h	• • • x x x x x	116
XR25	Alternate	Alternate Text Mode / H Virtual Panel Size	25h	R/W	3D7h	x x x x x x x x	116
XR26	Alternate	Alternate Horizontal Sync Start Register	26h	R/W	3D7h	x x x x x x x x	116
XR64	Alternate	Alternate Vertical Total	64h	R/W	3D7h	x x x x x x x x	145
XR65	Alternate	Alternate Overflow	65h	R/W	3D7h	x x x • • x x x	145
XR66	Alternate	Alternate Vertical Sync Start	66h	R/W	3D7h	x x x x x x x x	146
XR67	Alternate	Alternate Vertical Sync End	67h	R/W	3D7h	• • • • x x x x	146
XR2C	Flat Panel	FLM Delay	2Ch	R/W	3D7h	x x x x x x x x	118
XR2D	Flat Panel	LP Delay (Comp Enabled)	2Dh	R/W	3D7h	x x x x x x x x	119
XR2E	Flat Panel	LP Delay (Comp Disabled)	2Eh	R/W	3D7h	x x x x x x x x	119
XR2F	Flat Panel	LP Width	2Fh	R/W	3D7h	x x x x x x x x	120
XR4F	Flat Panel	Panel Format 2	4Fh	R/W	3D7h	x x • • • x x x	128
XR50	Flat Panel	Panel Format 1	50h	R/W	3D7h	x x x x x x x x	129
XR51	Flat Panel	Display Type	51h	R/W	3D7h	0 0 0 • 0 0 0 0	130
XR52	Flat Panel	Power Down Control	52h	R/W	3D7h	0 0 0 0 0 0 0 1	131
XR53	Flat Panel	Panel Format 3	53h	R/W	3D7h	• 0 0 0 0 0 x 0	132
XR54	Flat Panel	Panel Interface	54h	R/W	3D7h	x x x x x x x x	133
XR55	Flat Panel	Horizontal Compensation	55h	R/W	3D7h	x x x • • x x x	134
XR56	Flat Panel	Horizontal Centering	56h	R/W	3D7h	x x x x x x x x	135
XR57	Flat Panel	Vertical Compensation	57h	R/W	3D7h	x x x x x x x x	136
XR58	Flat Panel	Vertical Centering	58h	R/W	3D7h	x x x x x x x x	137
XR59	Flat Panel	Vertical Line Insertion	59h	R/W	3D7h	x x x • x x x x	137
XR5A	Flat Panel	Vertical Line Replication	5Ah	R/W	3D7h	• • • • x x x x	138
XR5B	Flat Panel	Panel Power Sequencing Delay	5Bh	R/W	3D7h	1 0 0 0 0 0 0 1	138
XR5C	Flat Panel	Activity Indicator Control	5Ch	R/W	3D7h	0 x • x x x x x	139
XR5D	Flat Panel	FP Diagnostic	5Dh	R/W	3D7h	0 0 0 0 0 0 0 0	140
XR5E	Flat Panel	M (ACDCLK) Control	5Eh	R/W	3D7h	x x x x x x x x	141
XR5F	Flat Panel	Power Down Mode Refresh	5Fh	R/W	3D7h	x x x x x x x x	141
XR60	Flat Panel	Blink Rate Control	60h	R/W	3D7h	1 0 0 0 0 0 1 1	142
XR61	Flat Panel	SmartMap™ Control	61h	R/W	3D7h	x x x x x x x x	143
XR62	Flat Panel	SmartMap™ Shift Parameter	62h	R/W	3D7h	x x x x x x x x	144
XR63	Flat Panel	SmartMap™ Color Mapping Control	63h	R/W	3D7h	x 1 x x x x x x	144
XR68	Flat Panel	Vertical Panel Size	68h	R/W	3D7h	x x x x x x x x	147
XR6C	Flat Panel	Programmable Output Drive	6Ch	R/W	3D7h	• • 0 0 0 0 d •	147
XR6E	Flat Panel	Polynomial FRC Control	6Eh	R/W	3D7h	1 0 1 1 1 1 0 1	148
XR6F	Flat Panel	Frame Buffer Control	6Fh	R/W	3D7h	0 0 0 0 0 0 0 0	149

Reset Codes:
x = Not changed by reset (indeterminate on power-up)
d = Set from the corresponding data bus pin on trailing edge of reset
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Reserved (read/write, reset to 0)
0/1 = Reset to 0 or 1 by trailing edge of reset

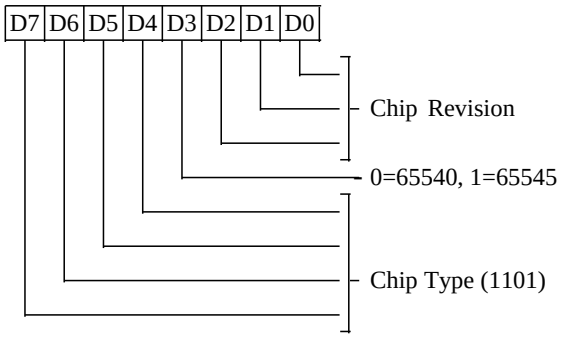
EXTENSION INDEX REGISTER (XRX)
Read/Write at I/O Address 3D6h



6-0 Index value used to access the extension registers

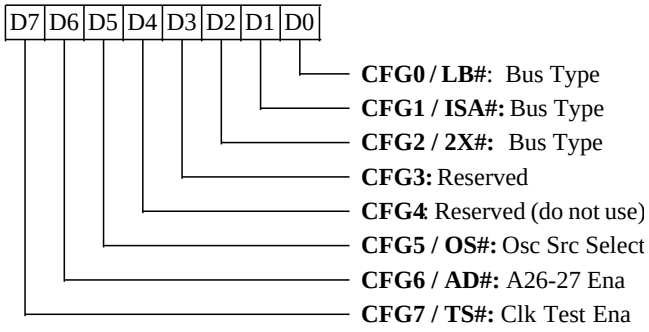
7 Reserved (0)

CHIPS VERSION REGISTER (XR00)
Read only at I/O Address 3D7h
Index 00h



7-0 **Chip Version** - 65540 Chip Versions start at D0h and are incremented for every silicon step. 65545 Chip Versions start at D8h and are incremented for every silicon step.

CONFIGURATION REGISTER (XR01)
Read only at I/O Address 3D7h
Index 01h



These bits latch the state of memory address bus A (AA bus) bits 0-7 on the rising edge of RESET#. The state of bits 0-7 after RESET# effect chip internal logic as indicated below. During RESET#, internal pullups are enabled for AA[7:0] and hence the status of these bits will be high if no external pull-down resistors are present on these pins.

This register is not related to the Virtual EGA Switch register (XR1F).

2-0 CFG2:0 - CPU Bus Type

2 2X#	1 ISA#	0 LB#	Bus Type
L	L	L	Reserved
L	L	H	Reserved
L	H	L	Reserved
L	H	H	CPU Direct (2x LCLK) (pin-23=CRESET)
H	L	L	Reserved
H	L	H	ISA Bus
H	H	L	PCI Bus (65545 only)
H	H	H	VL-Bus (1x clk) (pin-23=RDYRTN#)

3 CFG3-Reserved

The pin corresponding to this bit has no internal hardware function so may be used for sampling external conditions at reset.

4 CFG4-Reserved

The pin corresponding to this bit must be sampled high on reset so this bit will always read back 1.

5 CFG5 - Oscillator Source Select

0 External Oscillator drives XTALI (pin 203)
1 Internal Oscillator (series resonant crystal connected to XTALI and XTALO)

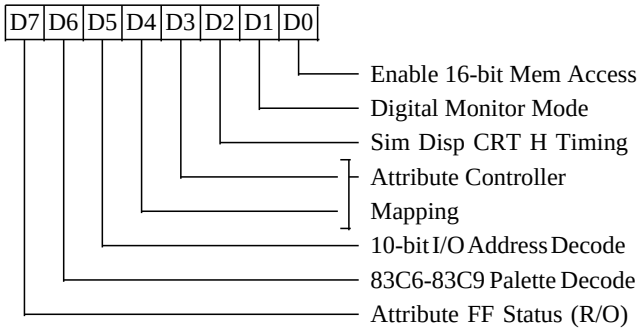
6 CFG 6 - A26-A27 Enable

0 Pin 53 is A26 (ignore for ISA & PCI)
Pin 54 is A27 (ignore for ISA & PCI)
1 Pin 53 is ACTI
Pin 54 is ENABKL

7 CFG7 - Internal Clock Test Mode

0 Enable internal clock test mode. Output MCLK on pin-30 (A25) and VCLK on pin 29 (A24)
1 Normal operation: ROMCS# generated in ISA bus mode

CPU INTERFACE CTRL REGISTER 1 (XR02)
Read/Write at I/O Address 3D7h
Index 02h



0 8/16-bit CPU Memory Access
- 0 8-bit CPU memory access (default)
- 1 16-bit CPU memory access

1 Digital Monitor Clock Mode
- 0 Normal (clk 0-1=25,28 MHz) (default)
- 1 Digital Monitor (clk 0-1=14,16MHz) 14MHz = 56MHz ÷ 4 or 28MHz ÷ 2 16MHz = 50MHz ÷ 3

2 SimultaneousDisplayCRTHTimingSelect
- 0 Use XR19,1A,1B for H parameters
- 1 Use CR04,05,00 for H parameters

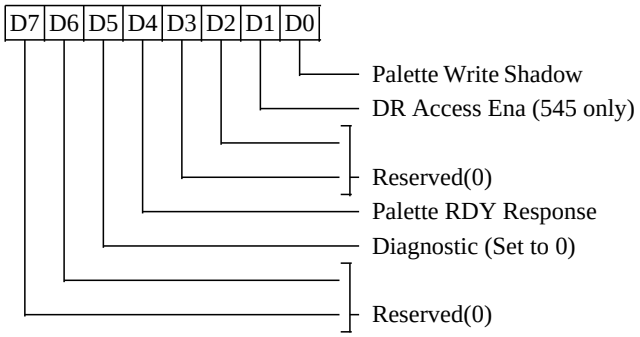
4-3 AttributeControllerMapping
- 00 Write Index and Data at 3C0h. (8-bit access only) (default - VGA mapping)
- 01 Write Index at 3C0h and Data at 3C1h (8-bit or 16-bit access). Attribute flip-flop (bit-7) is always reset in this mode (16-bit mapping)
- 10 Write Index and Data at 3C0h/3C1h (8-bit access only) (EGA mapping)
- 11 Reserved

5 I/O Address Decoding
- 0 Decode all 16 bits of I/O address (default)
- 1 Decode only lower 10 bits of I/O address. This affects addresses 3B4-3B5h, 3B8h, 3BAh, 3BFh, 3C0-3C2h, 3C4-3C5h, 3CE-3CFh, 3D4-3D5h, and 3D8-3DAh.

6 Palette Address Decoding
- 0 External palette registers can be accessed only at 3C6h-3C9h (default)
- 1 External palette regs can be accessed at 3C6h-3C9h & 83C6h-83C9h

7 Attribute Flip-Flop Status (read only)
0 = Index, 1 = Data

CPU INTERFACE CTRL REGISTER 2 (XR03)
Read/Write at I/O Address 3D7h
Index 03h



0 Palette Write Shadow

0 Chip responds normally to Palette Write accesses (LDEV# is returned for VL-Bus and DEVSEL# is returned for PCI bus)

1 Palette write commands are executed internally but the chip does not respond externally (LDEV# is not returned for VL-Bus and DEVSEL# is not returned for PCI bus). This conforms to both VL-Bus and PCI bus "Palette Shadowing" requirements as it forces the access to be passed on to the ISA bus where add-in cards may be shadowing the VGA color palette data. This bit should normally be set to 1.

1 DR Register Access Enable

0 32-Bit DRxx register access Disabled (Default)

1 DRxx registers accessible at I/O port defined by XR07.

3-2 Reserved (0)

4 ISA Bus Palette Access RDY Response

0 Hold off the CPU using RDY for palette accesses (read or write to 3C6-3C9h).

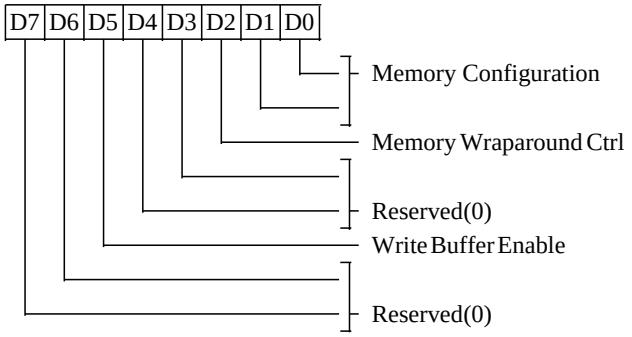
1 Do not hold off the CPU using RDY for palette accesses (read or write to 3C6-3C9h)

The internal RAMDAC has a minimum specification for time between accesses. A faster CPU is more likely to violate this specification, so it is normally required to add delay between accesses in software. This bit may be set to 0 to effectively create a CPU-transparent delay, however this is not compatible with some systems: some systems ignore RDY for palette accesses, so for those systems, this bit must be set to 1.

5 Diagnostic (R/W but should be set to 0)

7-6 Reserved (0)

MEMORY CONTROL REGISTER 1 (XR04)
Read/Write at I/O Address 3D7h
Index 04h



1-0 Memory Configuration

00 32-bit memory data path. Memory data bus is on MAD15-0 & MBD15-0 (DRAMs A and B). If frame acceleration is enabled and embedded frame buffer is selected, the data will be stored in both DRAMs A and B. An external frame buffer can be enabled on DRAM C with this setting.

01 16-bit data path (DRAM A only). The memory data bus is on MAD15-0. If frame acceleration is enabled and embedded frame buffer is selected, the data will be restricted to storage in DRAM A only. An external frame buffer can be enabled on DRAM C with this setting.

10 32-bit memory data path. Memory data bus is on MAD15-0 & MCD15-0 (DRAMs A & C). DRAM C cannot be used as an external frame buffer with this setting, but programming can select between this setting and '01' to switch the function of DRAM C between use as display memory and use as an external frame buffer.

11 Reserved

DRAM A must always be present and if that is the only DRAM present, setting 01 must be used. DRAM B may optionally be present and if it is, setting 00 may be used (either 00 or 01 may be programmed with DRAMs A & B physically present). If all three DRAMs are present, setting 00 would normally be used (00, 01, and 10 are all allowable). Setting 10 would be used where only two DRAMs (A and C) are physically present (this field is set to 10 to use both DRAMs as 1MB of display memory and set to 01 to use DRAM A as 512KB of display memory and DRAM C as an external frame buffer).

2 Memory Wraparound Control

This bit enables bits 16-17 of the CRT Controller address counter (default = 0 on reset).

0 Disable CRTC addr counter bits 16-17
1 Enable CRTC addr counter bits 16-17

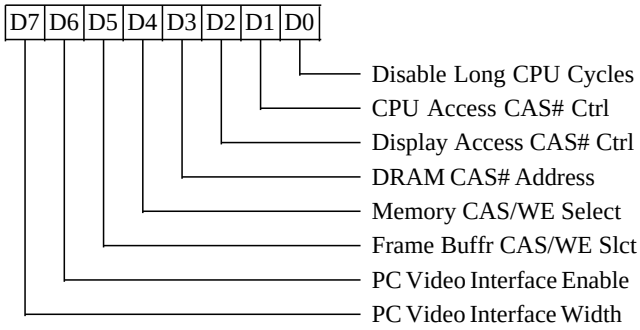
4-3 Reserved (0)

5 CPU Memory Write Buffer

0 Disable CPU memory write buffer (default)
1 Enable CPU memory write buffer

7-6 Reserved (0)

MEMORY CONTROL REGISTER 2 (XR05)
Read/Write at I/O Address 3D7h
Index 05h



0 Disable Long CPU Cycles

0 Enable long CPU cycles (default on RESET). This puts as many CPU cycles as possible into one RAS cycle.
1 Disable long CPU cycles.

1 CPU-Mem Access CAS# Cycle Ctrl (545)
2 Display Mem Access CAS# Cycle Ctrl (545)

Bit-1 affects accesses to display memory initiated by the 65545 for display refresh. Bit-2 affects CPU accesses to display memory in the 65545. Both bits are defined as follows:

0 3-MCLK CAS# cycle (2 low, 1 high) for all read or write accesses (default)
1 4-MCLK CAS# cycle (3 low, 1 high) for all read accesses and for the first CAS# cycle of page-mode write accesses (following cycles are 2L/1H)

These bits may be set to create looser memory timing (e.g., for 3.3V operation, to allow use of cheaper DRAMs, etc.). 4-MCLK CAS cycles are not supported in the 65540.

3 Asymmetric Address for DRAMs A & B

0 Symmetric 256Kx16 DRAM is used (9-bit RAS/CAS addresses) (default)
1 Asymmetric 256Kx16 DRAM is used (10-bit RAS/8-bit CAS address)

Asymmetric address DRAMs should not be used (and this bit should not be set to one) if AA9 is used as a 32KHz clock input (see XR33 bit-6) or if 24-bit PC-Video interface is enabled (see bit-7 of this register). See also XR6F bit-2 (address symmetry control for DRAM C).

4 CAS# / WE# Select for DRAMs A & B

0 2-CAS# / 1-WE# 256Kx16 DRAM configuration is used (default)
1 1 CAS# and 2 WE# 256Kx16 DRAM configuration is used

5 CAS# / WE# Select for DRAM C

This bit is effective when XR6F[7]=1.

0 2 CAS# and 1 WE# configuration 256Kx16 DRAM is used (default)
1 1 CAS# and 2 WE# configuration 256Kx16 DRAM is used

6 PC Video Interface Enable

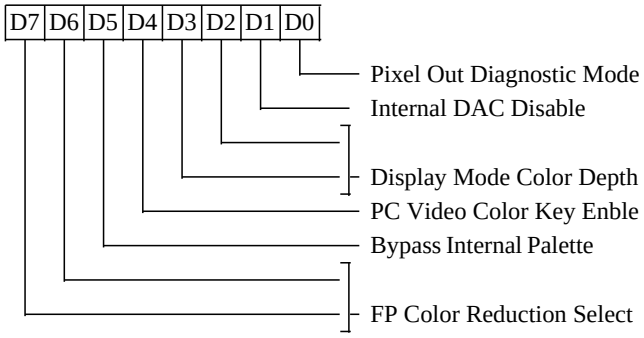
0 Disable PC Video Interface (default)
1 Enable PC Video interface on DRAM 'C' pins (MCD15-0, RASC#, CASCH#, CASCL#, and WEC#). If bit-7 of this register is set to 1, OEC#, AA9, ACTI, ENABKL, and CA8-9 also serve as PC Video Interface pins. An external frame buffer cannot be used in this configuration.

7 PC Video Interface Control

0 18-bit PC Video interface
1 24-bit PC Video interface

Note: When this bit is set to 1, AA9, ENABKL, ACTI pins are used for video inputs therefore they lose their alternate functions. When this bit is set to 1, a 24-bit panel interface is also available (CA0-7 become P16-23). This bit should not be set to 1 if the AD# (A26-27 enable) or EC# (external clock) configuration bits are asserted low at reset (since this enables ACTI and ENABKL to perform alternate functions).

PALETTE CONTROL REGISTER (XR06)
Read/Write at I/O Address 3D7h
Index 06h



0 Pixel Data Pin Diagnostic Output Mode

0 Normal operation. Pixel data (P15:0) pins output flat panel pixel data (default on Reset).
1 Output CRT pixel data on pixel data pins P0-7 and output various internal signals on pixel data pins P8-15 for diagnostic purposes.

1 Internal DAC Disable

This bit affects the DAC analog outputs.

0 Enable internal DAC (default on Reset). DAC analog outputs (R, G, B) will be active and HSYNC and VSYNC signals are driven (Default on reset).
1 Disable internal DAC. The DAC analog outputs (R, G, B) will be 3-stated. Setting this bit forces power down of the internal DAC. HSYNC and VSYNC are forced inactive if XR5D[6] is 0 and will be driven if XR5D[6] is 1.

3-2 Display Mode Color Depth

00 4 or 8 bits-per-pixel (default on reset)
01 16 bpp (5-5-5) (Targa compatible)
10 24 bpp (true color)
11 16 bpp (5-6-5) (XGA compatible)

4 PC Video Color Key Enable

0 Disable PC Video Overlay (default on reset)
1 Enable PC Video Overlay on color key

5 Bypass Internal VGA Palette

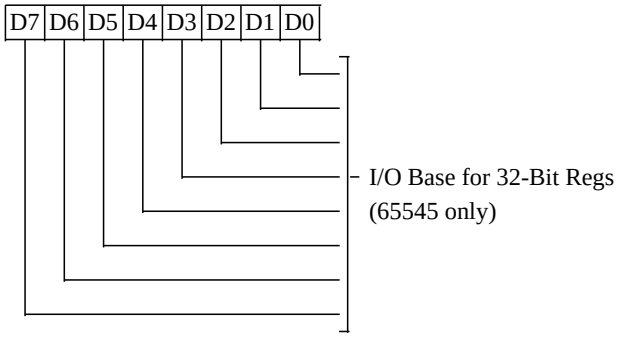
0 Use internal VGA palette (Default on reset).
1 Bypass internal VGA palette which will be powered down if DAC is disabled.

7-6 Color Reduction Select

These bits are effective in flat panel mode. These bits select the algorithm used to reduce 24-bit or 18-bit color data to 8-bit or 6-bit color data for monochrome panels.

00 NTSC weighting algorithm (default on reset)
01 Equivalent weighting algorithm
10 Green only
11 Color (no reduction). This setting should be used when driving color panels.

I/O BASE REGISTER (XR07)
Read/Write at I/O Address 3D7h
Index 07h



7–0 I/O Base for 32-Bit Registers (65545 only)

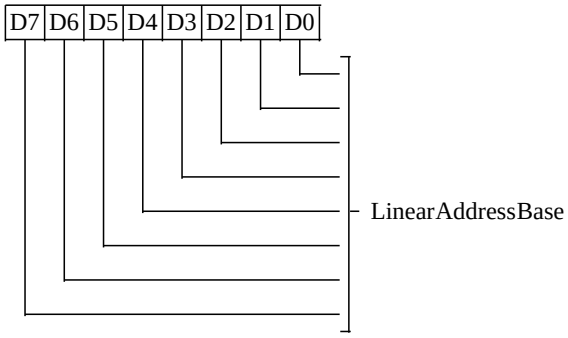
In ISA and VL-Bus configuration, these bits determine the I/O range for the Doubleword Hardware Cursor & BitBLT registers (DRxx). The value programmed here is matched against CPU addresses A15 & A8-2. Address A9 must equal 1 and A14-10 select one of 32 DR registers. For example, a programmed value of 074h (011101 00b) would result in this DR register mapping:

DRxx:		nxxx xx1n nnnn nn00b
DR00:	03D0h =	0000 0011 1101 0000b
DR01:	07D0h =	0000 0111 1101 0000b
DR02:	0BD0h =	0000 1011 1101 0000b
DR03:	0FD0h =	0000 1111 1101 0000b
DR04:	13D0h =	0001 0011 1101 0000b
DR05:	17D0h =	0001 0111 1101 0000b
DR06:	1BD0h =	0001 1011 1101 0000b
DR07:	1FD0h =	0001 1111 1101 0000b
DR08:	23D0h =	0010 0011 1101 0000b
DR09:	27D0h =	0010 0111 1101 0000b
DR0A:	2BD0h =	0010 1011 1101 0000b
DR0B:	2FD0h =	0010 1111 1101 0000b
DR0C:	33D0h =	0011 0011 1101 0000b

The DRxx registers are enabled for access by setting XR03[1]. They are disabled following Reset. The programmer should write this register before enabling access to the DRxx registers.

In PCI bus configuration, this register is ignored. The PCI Configuration IOBASE register is used to determine the base address for the 32-bit registers in the PCI I/O space. Note that for PCI bus configuration only, the 32-bit registers may also be memory mapped: MBASE defines a 2MB memory space with frame buffer memory mapped into the lower megabyte and the 32-bit registers mapped into the upper megabyte.

LINEARADDRESSINGBASEREGISTER(XR08)
Read/Write at I/O Address 3B7h/3D7h
Index 08h



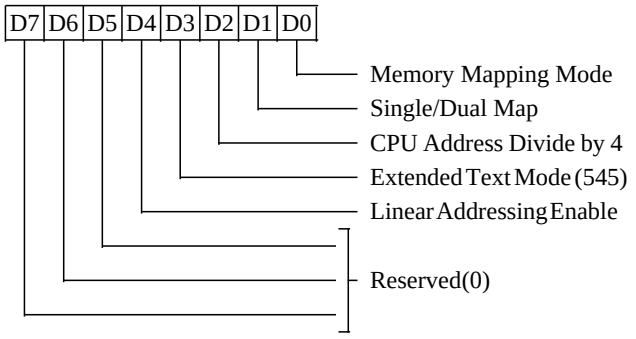
7-0 Linear Address Base

In VL-Bus configuration, if linear addressing is enabled (XR0B[4]=1), these 8 bits are compared to A[27:20] to determine the base address of the 1MB of display memory in the 256MB VL-Bus address space (normally the VL address space is 4GB, but only 28 bits of address are decoded by the chip). For example, if the video memory is to be placed at 12MB (0C00000-0CFFFFFh), this register should be programmed to '00001100b'. Note that as a result, programming this register to 0 is typically not useful.

If A26-27 are not available (used for ACTI and ENABKL if Configuration Register XR01 bit-6 = 1) then bits 6-7 of this register are ignored and only A20-25 are compared against bits 0-5 of this register to determine the base address for the linear frame buffer in the VL-Bus / 486 CPU memory space. Similarly, if A25 and/or A24 are not available (see configuration bits 3, 4, and 7), bits 5 and/or 4 are also ignored. In ISA bus configuration, address inputs A24-27 are never available, so bits 4-7 of this register are ignored and A20-23 are compared against bits 0-3 of this register to determine the base address for the linear frame buffer in the 16MB ISA memory space.

In PCI bus configuration, this register is ignored. The PCI Configuration MBASE register is used to determine the base address for the linear frame buffer in the 4GB (full 32-bit address) PCI memory address space.

CPU PAGING REGISTER (XR0B)
Read/Write at I/O Address 3D7h
Index 0Bh



0 Memory Mapping Mode

0 Normal Mode (VGA compatible) (default on Reset)
1 Extended Mode (mapping for > 256 KByte memory configurations)

1 CPU Single/Dual Mapping

0 CPU uses only a single map to access the extended video memory space (default on Reset)
1 CPU uses two maps to access the extended video memory space. The base addresses for the two maps are defined in the Low Map Register (XR10) and High Map Register (XR11).

2 CPU Address Divide by 4

0 Disable divide by 4 for CPU addresses (default on Reset)
1 Enable divide by 4 for CPU addresses. This allows the video memory to be accessed sequentially in mode 13. In addition, all video memory is available in mode 13 by setting this bit.

3 Extended Text Mode (65545 only)

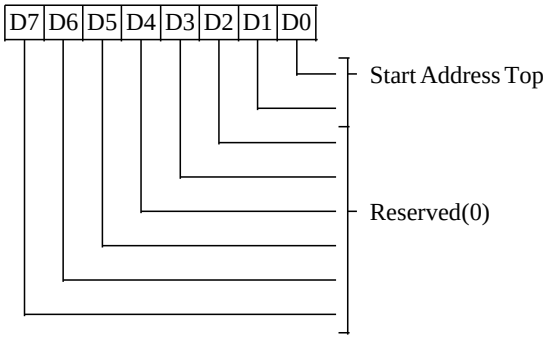
Set to enable text font 'scrambling' in plane 2. Setting this bit improves text mode performance in single-DRAM configurations (with the proper BIOS support for font load/reload functions). This bit should be set in single DRAM configurations only. This bit is supported in the 65545 only; it should be programmed to 0 in the 65540.

4 Linear Addressing Enable

0 Standard VGA (A0000 - BFFFF) memory space decoded on-chip using A17-19 (default on Reset)
1 Linear Addressing Enabled. See XR08 (Linear Addressing Base) for base address selection. Ignored in PCI bus configuration (see DEVCTL).

7-5 Reserved (0)

START ADDRESS TOP REGISTER (XR0C)
Read/Write at I/O Address 3D7h
Index 0Ch



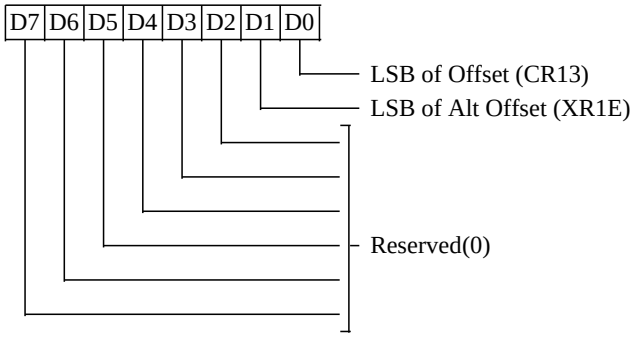
1-0 Start Address Top

These bits defines the high order bits for the Display Start Address when 512 KBytes or more of memory is used (see XR04 bits 1–0).

7-2 Reserved (0)

AUXILIARY OFFSET REGISTER (XR0D)

Read/Write at I/O Address 3D7h
Index 0Dh



0 Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the regular Offset register (CR13).

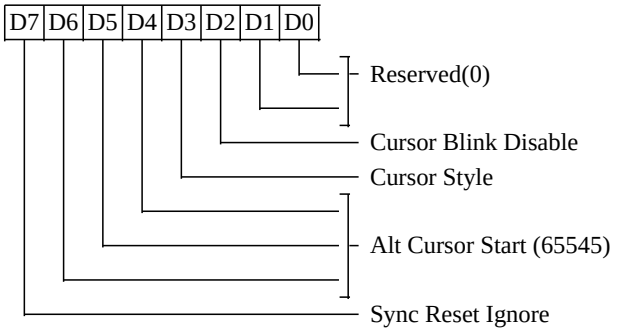
1 Alternate Offset Register LSB

This bit provides finer granularity to the display memory address offset when word and doubleword modes are used. This bit is used with the Alternate Offset register (XR1E).

7-2 Reserved (0)

TEXT MODE CONTROL REGISTER (XR0E)

Read/Write at I/O Address 3D7h
Index 0Eh



This register is effective for both CRT and flat panel text modes.

1-0 Reserved (0)

2 Cursor Mode

0 Blinking (default on Reset).
1 Non-blinking

3 Cursor Style

0 Replace (default on Reset)
1 Exclusive-Or

6-4 Alternate Cursor Start (65545 Only)

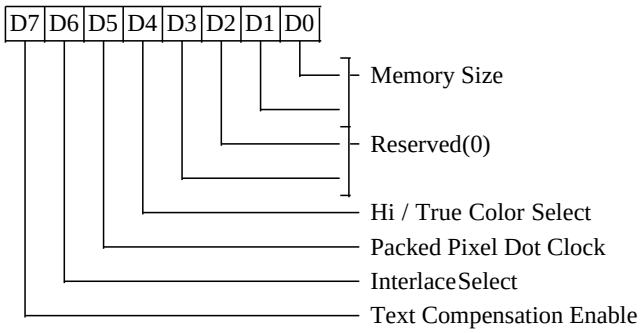
When the alternate CRTC registers are active, this field may be set to specify the Cursor Start Scan Line instead of CR0A bits 0-4 (this field specifies alternate bits 0-2 with bits 3-4 assumed to be 0).

VGA software typically changes the shape of the cursor frequently between underline and block styles. This field allows the cursor style to be fixed (typically to 'block' for improved readability on panels).

7 Synchronous Reset Ignore

When this bit is set, the chip will ignore SR00 bit-1 (Synchronous Reset) and will remain in normal operation. Synchronous reset is a holdover from the original VGA which is no longer required. VGA software, however, performs synchronous resets frequently, creating the possibility for display memory corruption if the chip is left in the synchronous reset state for too long. The 65540 / 545 display memory sequencer does not need to be periodically reset, so this bit is provided to prevent potential display memory corruption problems. For absolute VGA compatibility, this bit may be set to 0.

SOFTWARE FLAGS REGISTER 0 (XR0F)
Read/Write at I/O Address 3D7h
Index 0Fh



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

1-0 Memory Size

00 256KB
01 512KB
1x 1MB

2-3 Reserved (0)

4 Hi Color / True Color

0 Current mode is not hi-/true-color mode
1 Current mode is hi-color / true-color mode

5 Packed-Pixel Mode Dot Clock

0 Use default dot clock in packed-pixel modes
1 Use 40MHz dot clock in packed-pixel modes

This bit is used for high resolution panels in panel mode only.

6 Interlace Select

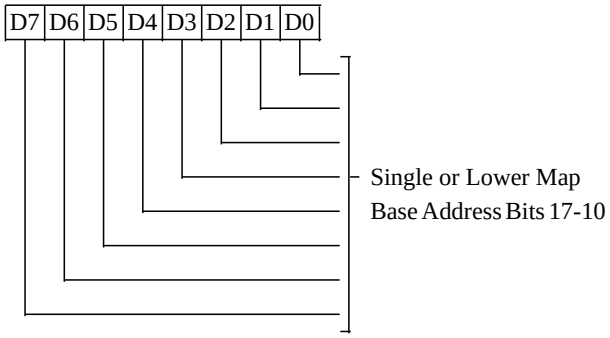
0 Set mode 24h, 34h, 72h/75h or 7Eh interlaced
1 Set mode 24h, 34h, 72h/75h or 7Eh non-interlaced

7 Text Compensation Enable/Disable

0 Tall font disabled
1 Tall font enabled

See also XR2B, XR44, XR45 for definition of other software flags registers.

SINGLE/LOW MAP REGISTER (XR10)
Read/Write at I/O Address 3D7h
Index 10h



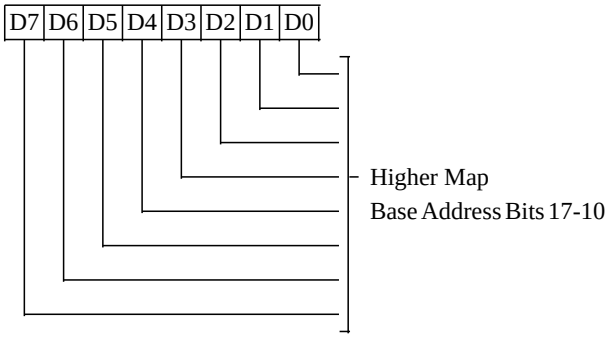
This register effects CPU memory address mapping.

7-0 Single / Low Map Base Address Bits 17-10

These bits define the base address in single map mode (XR0B bit-1 = 0), or the lower map base address in dual map mode (XR0B bit-1 = 1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. In case of dual mapping, this register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 Bits 3-2	Low Map	
00	A0000-AFFFF	
01	A0000-A7FFF	
10	B0000-B7FFF	Single mapping only
11	B8000-BFFFF	Single mapping only

HIGH MAP REGISTER (XR11)
Read/Write at I/O Address 3D7h
Index 11h



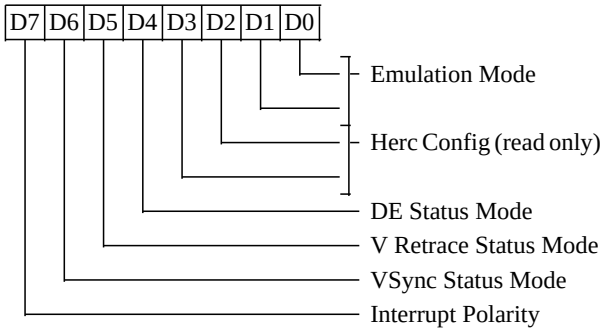
This register effects CPU memory address mapping.

7-0 High Map Base Address Bits 17-10

These bits define the Higher Map base address in dual map modes (XR0B bit-1=1). The memory map starts on a 1K boundary in planar modes and on a 4K boundary in packed pixel modes. This register controls the CPU window into display memory based on the contents of GR06 bits 3-2 as follows:

GR06 bits 3-2	High Map
00	B0000-BFFFF
01	A8000-AFFFF
10	Don't care
11	Don't care

EMULATION MODE REGISTER (XR14)
Read/Write at I/O Address 3D7h
Index 14h



1-0 Emulation Mode

00 VGA mode (default on Reset)
01 CGA mode
10 MDA/Herculesmode
11 EGA mode

3-2 Hercules Configuration Register (3BFh) readback (read only)

4 Display Enable Status Mode

0 Select Display Enable status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on reset). Normally used for CGA, EGA, and VGA modes.

1 Select HSync status to appear at bit 0 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

5 Vertical Retrace Status Mode

0 Select VerticalRetrace status to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh) (default on Reset). Normally used for CGA, EGA, and VGA modes.
1 Select Video to appear at bit 3 of Input Status register 1 (I/O Address 3BAh/3DAh). Normally used for MDA / Hercules mode.

6 VSync Status Mode

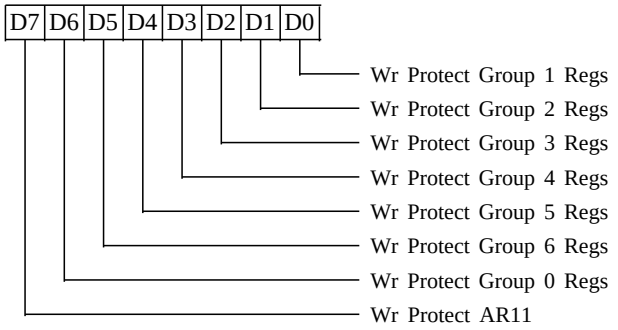
0 Prevent VSync status from appearing at bit 7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for CGA, EGA, and VGA modes.
1 Enable VSync status to appear as bit-7 of Input Status Register 1 (I/O Address 3BAh/3DAh). Normally used for MDA/Hercules mode.

7 Interrupt Output Function

This bit controls the function of the interrupt output pin (IRQ):

Interrupt State	Bit-7=0	Bit-7=1
Disabled	3-state	3-state
Enabled, Inactive	3-state	Low
Enabled, Active	3-state	High

WRITE PROTECT REGISTER (XR15)
Read/Write at I/O Address 3D7h
Index 15h



This register controls write protection for various groups of registers as shown. 0 = unprotected (default on Reset), 1= protected.

0 Write Protect Group 1 Registers

This bit affects the Sequencer registers (SR00-04), Graphics Controller registers (GR00-08), and Attribute Controller registers (AR00-14).

Note that AR11 is also protected by bit-7 which is ORed with this bit.

1 Write Protect Group 2 Registers

This bit affects CR09 bits 0-4, CR0A, and CR0B.

2 Write Protect Group 3 Registers

This bit affects CR07 bit-4, CR08, CR11 bits 5-4, CR13, CR14, CR17 bits 0-1 and bits 3-7, and CR18.

3 Write Protect Group 4 Registers

This bit affects CR09 bits 5-7, CR10, CR11 bits 0-3 and bits 6-7, CR12, CR15, CR16, and CR17 bit-2.

4 Write Protect Group 5 Registers

This bit affects the Miscellaneous Output register (3C2h) and the Feature Control register(3BAh/3DAh).

5 Write Protect Group 6 Registers

This bit affects the VGA color palette registers (3C6h-3C9h). If this bit is set, all VGA color palette registers are write protected.

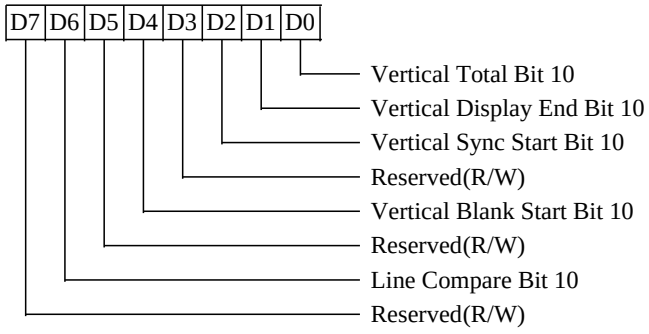
6 Write Protect Group 0 Registers

This bit affects CR0-7 (except CR07 bit-4). This bit is logically ORed with CR11 bit-7.

7 Write Protect AR11

This bit is ORed with bit-0, therefore writing to AR11 is possible only if both bit-0 and bit-7 are 0. This feature is used for write protection of the overscan color. This is important in order to keep application software from changing the border color while still permitting the attribute controller to be changed for the addressable portion of the display. Overscan is increasingly becoming an ergonomics requirement and this bit will ensure software compatibility.

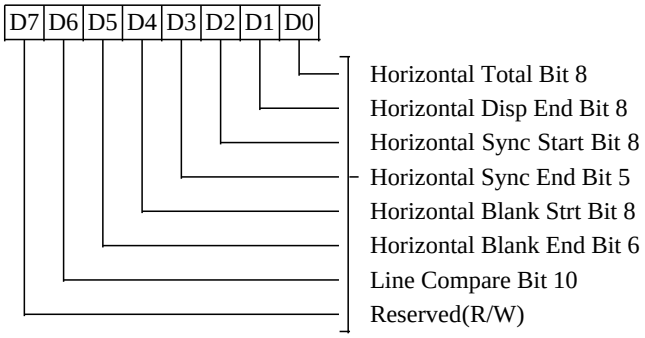
VERTICAL OVERFLOW REGISTER (XR16)
Read/Write at I/O Address 3D7h
Index 16h



This register is used for both normal and alternate vertical parameters.

0 Vertical Total Bit-10
1 Vertical Display End Bit-10
2 Vertical Sync Start Bit-10
3 Reserved (R/W)
4 Vertical Blank Start Bit-10
5 Reserved (R/W)
6 Line Compare Bit-10
7 Reserved (R/W)

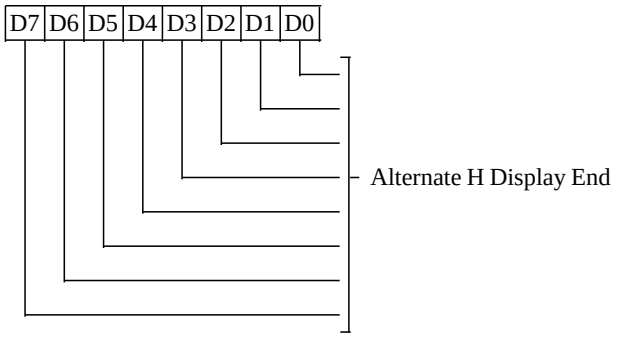
HORIZONTAL OVERFLOW REGISTER (XR17)
Read/Write at I/O Address 3D7h
Index 17h



This register is used for both normal and alternate horizontal parameters.

0 Horizontal Total Bit-8
1 Horizontal Display End Bit-8
2 Horizontal Sync Start Bit-8
3 Horizontal Sync End Bit-5
4 Horizontal Blank Start Bit-8
5 Horizontal Blank End Bit-6
6 Line Compare Bit-10
7 Reserved (R/W)

ALTERNATE HORIZONTAL DISPLAY END REGISTER (XR18)
Read/Write at I/O Address 3D7h
Index 18h



This register is used in flat panel and CRT CGA text and graphics modes, and Hercules graphics mode.

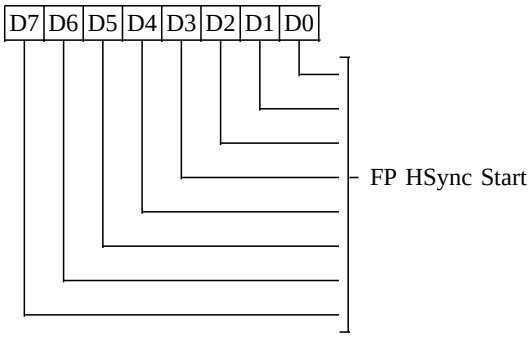
7-0 Alternate Horizontal Display End

This register specifies the number of characters displayed per scan line, similar to CR01.

Programmed Value = Actual Value – 1

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

ALTERNATE HORIZONTAL SYNC START REGISTER (XR19)
Read/Write at I/O Address 3D7h
Index 19h



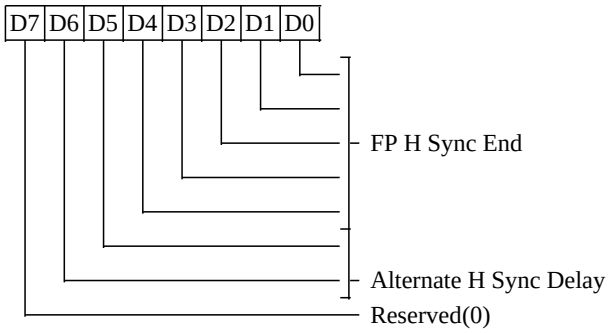
This register is used in all flat panel modes with horizontal compression disabled, to set the horizontal sync start. This register is also used in CRT CGA text and graphics modes, and Hercules graphics mode.

7-0 Alternate Horizontal Sync Start

These bits specify the beginning of the HSync in terms of character clocks from the beginning of the display scan. Similar to CR04.

Programmed Value = Actual Value – 1

ALTERNATE HORIZONTAL SYNC END REGISTER (XR1A)
Read/Write at I/O Address 3D7h
Index 1Ah



This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

4-0 Alternate Horizontal Sync End

Lower 5 bits of the character clock count which specifies the end of horizontal sync. Similar to CR05. If the horizontal sync width desired is N clocks, then programmed value is:

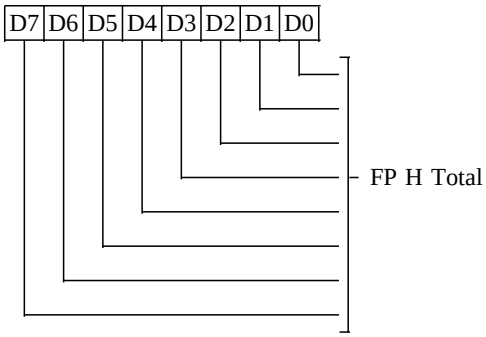
(N + Contents of XR19) ANDed with 01F Hex

6-5 CRT Alternate Horizontal Sync Delay

See CR05 for description

7 Reserved (0)

ALTERNATE HORIZONTAL TOTAL REGISTER (XR1B)
Read/Write at I/O Address 3D7h
Index 1Bh



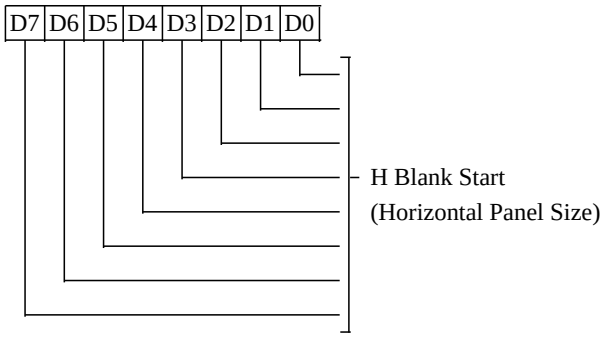
This register is used in all flat panel modes with horizontal compression disabled, CRT CGA text and graphics modes, and Hercules graphics mode.

7-0 Alternate Horizontal Total

This register contents are the total number of character clocks per line. Similar to CR00.

Programmed Value = Actual Value – 5

ALTERNATE HORIZONTAL BLANK START/ HORIZONTAL PANEL SIZE REGISTER (XR1C)
Read/Write at I/O Address 3D7h
Index 1Ch



The value in this register is the Horizontal Panel Size in all Flat Panel Modes. In CRT mode, it is used for CGA text and graphics and Hercules graphics modes.

7-0 FP Horizontal Panel Size

Horizontal panel size is programmed in terms of number of 8-bit (graphics/text) or 9-bit (text) characters. For double drive flat panels the actual horizontal panel size must be a multiple of two character clocks.

Programmed Value = Actual Value – 1

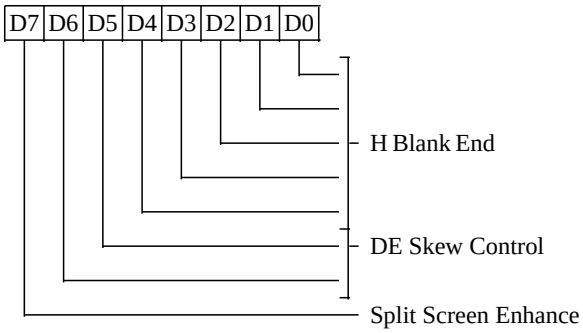
or

7-0 CRT Alternate Horizontal Blank Start

See CR02 for description

Programmed Value = Actual Value – 1

ALTERNATE HORIZONTAL BLANK END REGISTER (XR1D)
Read/Write at I/O Address 3D7h
Index 1Dh



Bits 0-6 of this register are used in CRT CGA text and graphics modes and CRT Hercules graphics mode. Bit 7 of this register is used for all CRT and flat panel modes.

4-0 CRT Alternate Horizontal Blank Start

See CR03 for description

6-5 CRT Alternate Display Enable Skew Control

See CR03 for description

7 Line Compare Fix

This bit affects all CRT and FP text modes. This bit is 0 on reset.

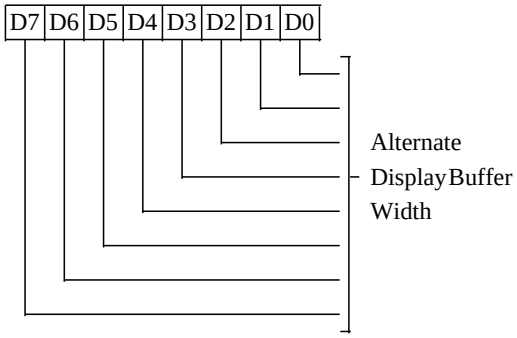
0 Internal Line Compare (split screen) flag is not delayed so that the Vertical Row Counter is reset too early which in text mode causes the first scanline of the first character row following split screen to be skipped (not displayed). This is IBM VGA compatible.

1 Internal Line Compare (split screen) flag is delayed so that the Vertical Row Counter is reset properly which in text mode causes the first scanline of the first character row following split screen to be displayed.

Note: This register is used in emulation modes only. It is not used in CRT or flat panel VGA modes.

ALTERNATE OFFSET REGISTER (XR1E)

Read/Write at I/O Address 3D7h
Index 1Eh



This register is used in all flat panel modes, CRT CGA text and graphics modes and Hercules graphics mode.

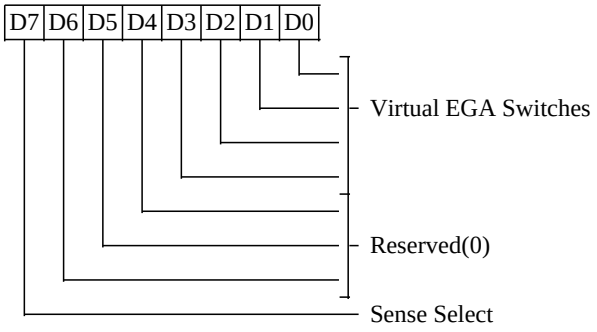
7-0 Alternate Offset

See CR13 for description

Programmed Value = Actual Value – 1

VIRTUAL EGA SWITCH REGISTER (XR1F)

Read/Write at I/O Address 3D7h
Index 1Fh



3-0 Virtual Switch Register

If bit-7 is '1', then one of these four bits is read back in Input Status Register 0 (3C2h) bit 4. The selected bit is determined by Miscellaneous Output Register (3C2h) bits 3-2 as follows:

Misc 3-2	XR1F Bit Selected
00	bit-3
01	bit-2
10	bit-1
11	bit-0

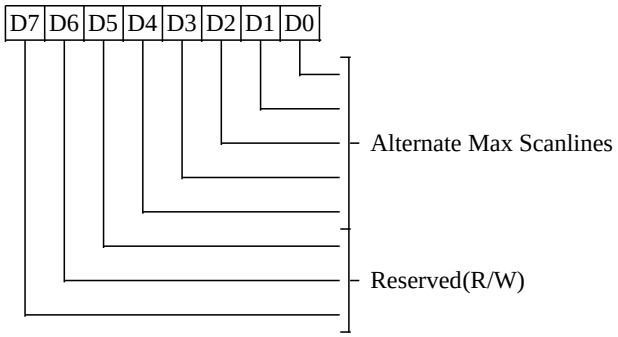
6-4 Reserved (0)

7 Sense Select

0 Select the output of the internal RGB comparator (Sense) for readback in Input Status Register 0 bit-4 (default on Reset).

1 Select one of bits 3-0 for readback in Input Status Register 0 bit-4.

ALTERNATE MAXIMUM SCANLINE REGISTER (XR24)
Read/Write at I/O Address 3D7h
Index 24h



This register is used in flat panel text mode when TallFont is enabled during vertical compensation.

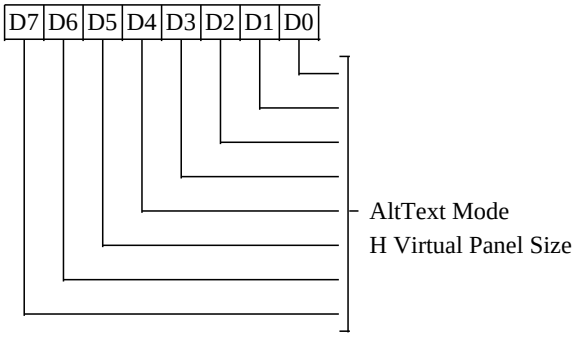
4-0 Alternate Maximum Scanlines (AMS)

Programmed Value = number of scanlines minus one per character row of TallFont

Double scanned lines, inserted lines, and replicated lines are not counted.

7-5 Reserved (R/W)

ALTERNATE TEXT MODE/HORIZONTAL VIRTUAL PANEL SIZE REGISTER (XR25)
Read/Write at I/O Address 3D7h
Index 25h

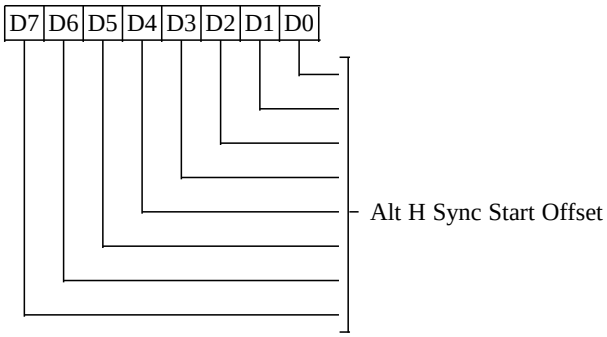


This register is used in flat panel 9-dot text modes.

7-0 Alternate Text Mode Horizontal Virtual Panel Size

Programmed Value = 9/8 [XR1C + 1] – 1

ALTERNATE HORIZONTAL SYNC START OFFSET REGISTER (XR26)
Read/Write at I/O Address 3D7h
Index 26h



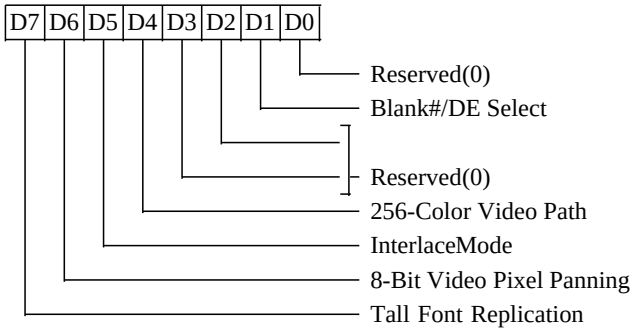
This register is used in flat panel mode.

7-0 Horizontal Sync Start Offset

This value is added to CR04 (Horizontal Sync Start) when XR02 bit 2 is set to '1'.

VIDEO INTERFACE REGISTER (XR28)

Read/Write at I/O Address 3D7h
Index 28h



0 Reserved (0)

1 Blank/Display Enable Select

This bit is effective in CRT mode only. In flat panel mode, XR54 bit-1 controls BLANK# functionality.

0 BLANK# controls color palette blanking (default on reset)
1 Display Enable controls color palette blanking

Note: This bit also controls the functionality of pins 68 or 69 when BLANK# / DE is selected for output instead of the default function (M is normally output on pin 69 and LP is normally output on pin 68 but this can be changed by XR4F bits 6 and 7 respectively). See also XR54 bits 0 and 1.

3-2 Reserved (0)

4 256-Color Video Path

This bit is effective for both CRT and flat panel in 256-color modes other than mode 13 (i.e., Super VGA modes).

0 4-bit video data path (default on reset)
1 8-bit video data path (horizontal pixel panning is controlled by bit-6)

Note: GR05 bit-5 must be 0 if this bit is set

5 Interlace Video

This bit is effective only for CRT graphics mode. This bit should be programmed to 0 for flat panel. In interlace mode XR29 holds the half-line positioning of VSync for odd frames.

0 Non-interlaced video (default on reset)
1 Interlacedvideo

6 8-Bit Video Pixel Panning

This bit is effective for both CRT and flat panel when the 8-bit video data path is selected (bit-4 = 1).

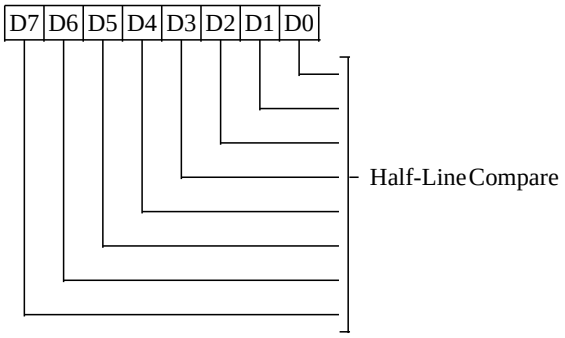
0 AR13 bits 2-1 are used to control pixel panning (default on Reset)
1 AR13 bits 2-0 are used to control pixel panning

7 Tall Font Replication

0 Tall font replicates lines 1, 9 and 12
1 Tall font replicates line 0 twice and line 15 once

HALF LINE COMPARE REGISTER (XR29)

Read/Write at I/O Address 3D7h
Index 29h

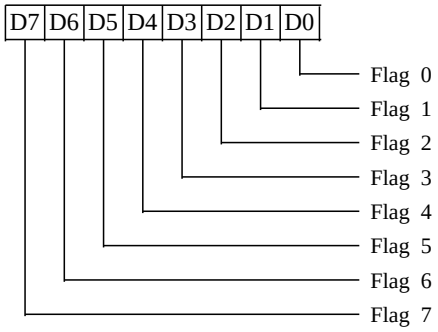


In Interlaced mode CRT operation, this register is used to generate the Half Line Compare Signal.

7-0 CRT Half-Line Value

In CRT interlaced video mode this value is used to generate the 'half-line compare' signal that controls the positioning of the VSync for odd frames.

SOFTWARE FLAGS REGISTER 1 (XR2B)
Read/Write at I/O Address 3D7h
Index 2Bh



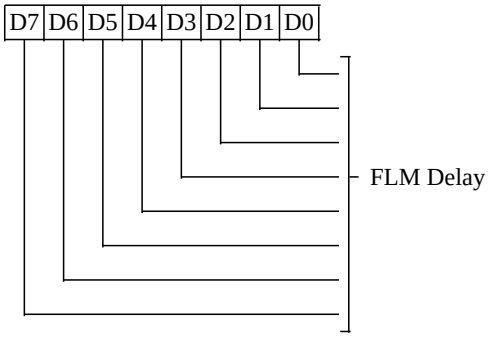
This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

7-0 Display Mode

These bits are used by the BIOS to store the current display mode number.

See also XR0F, XR44, XR45 for definition of other software flags registers.

FLM DELAY REGISTER (XR2C)
Read/Write at I/O Address 3D7h
Index 2Ch



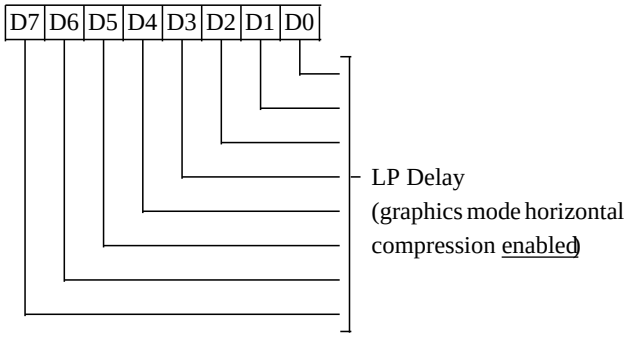
This register is used only in flat panel mode when XR2F bit-7=0. The First Line Marker (FLM) signal is generated from an internal FP VSync active edge with a delay specified by this register. The FLM pulse width is always one line for SS panels and two lines for DD panels.

7-0 FLM Delay (VDelay)

These bits define the number of HSyncs between the internal VSync and the rising edge of FLM.

LP DELAY REGISTER (CMPR ENABLED) (XR2D)

Read/Write at I/O Address 3D7h
Index 2Dh



This register is used only in flat panel mode when XR2F bit-6 = 0 and graphics mode horizontal compression is enabled. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-5 and the value in this register. The LP pulse width is specified in register XR2F.

7-0 LP Delay

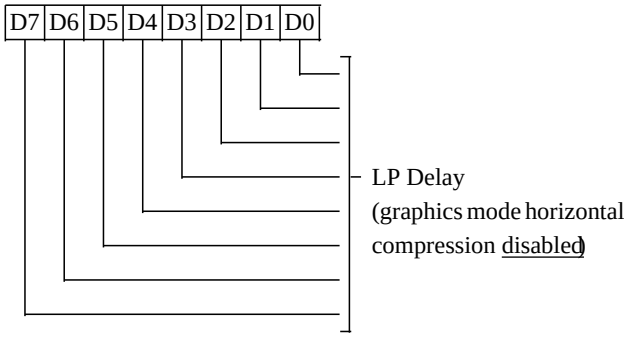
These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel mode with 9-dot text mode forced to 8-dot text. The msb (bit 8) of this parameter is XR2F bit-5.

Programmed Value = Actual Value – 1

Note: For DD panels without frame acceleration, the programmed value should be doubled.

LP DELAY REGISTER (CMPR DISABLED) (XR2E)

Read/Write at I/O Address 3D7h Index 2Eh



This register is used only in flat panel mode when XR2F bit-6 = 0 and 9-dot text mode is used. The LP output is generated from the FP Blank inactive edge with a delay specified by XR2F bit-4 and the value in this register. The LP pulse width is specified in register XR2F.

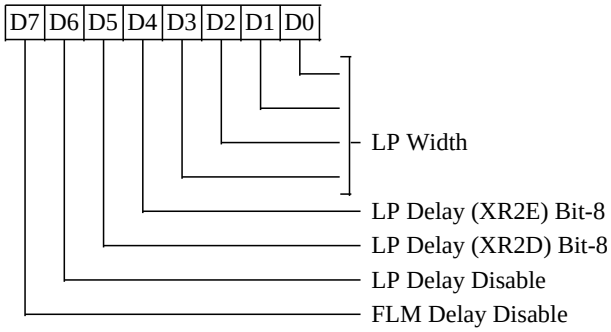
7-0 LP Delay

These bits define the number of character clocks between the FP Blank inactive edge and the rising edge of the LP output in flat panel 9-dot text modes. The msb (bit 8) of this parameter is XR2F bit-4.

Programmed Value = Actual Value – 1

Note: For DD panels without frame acceleration, the programmed value should be doubled.

LP WIDTH REGISTER (XR2F)
Read/Write at I/O Address 3D7h
Index 2Fh



This register is used only in flat panel mode. This register together with XR2D or XR2E defines the LP output pulse in flat panel mode.

3-0 LP Width (HWidth)

These bits define the width of LP output pulse in terms of number of character (8-dot only) clocks in flat panel mode.

Programmed Value = Actual Value – 1

4 LP Delay (XR2E) Bit 8

This bit is the msb of the LP Delay parameter for 9-dot text modes.

5 LP Delay (XR2D) Bit 8

This bit is the msb of the LP Delay parameter for graphics mode with horizontal compression disabled.

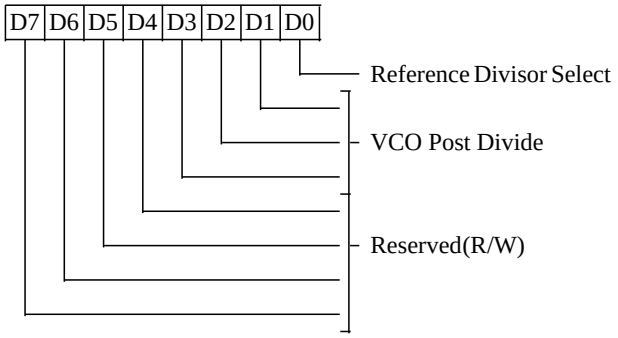
6 LP Delay Disable

0 LP Delay Enable: XR2D and XR2F bit-5 (or XR2E and XR2F bit-4) are used to delay the LP active edge with respect to the FP Blank inactive edge.
1 LP Delay Disable: LP active edge will coincide with the FP Blank inactive edge.

7 FLM Delay Disable

0 FLM Delay Enable: XR2C is used to delay the external FLM active edge with respect to the internal FP VSync active edge.
1 FLM Delay Disable: the external FLM active edge will coincide with the internal FLM active edge.

CLOCK DIVIDE CONTROL REGISTER (XR30)
Read/Write at I/O Address 3D7h
Index 30h



The three clock data registers (XR30-XR32) are programmed with the loop parameters to be loaded into the clock synthesizer. The Memory and Video clock VCO's both have programmable registers. Which of the VCO's is currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to this register is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data is written to registers XR30, and XR31 followed by a write to XR32. The completion of the write to XR32 causes data from all three registers is transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

0 Reference Divisor Select

Selects the reference pre-scale factor:

0 Divide by 4
1 Divide by 1

3–1 Post Divisor Select

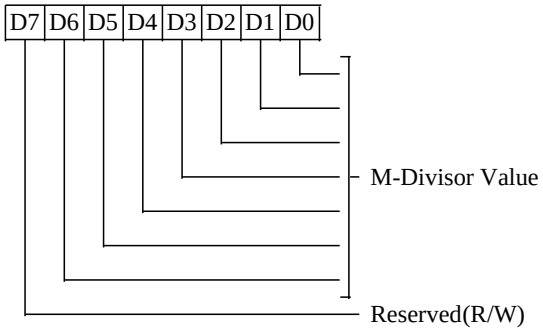
Selects the post-divide factor:

000 Divide by 1
001 Divide by 2
010 Divide by 4
011 Divide by 8
100 Divide by 16
101 Divide by 32
110 Divide by 64
111 Divide by 128

7–4 Reserved (R/W)

CLOCK M-DIVISOR REGISTER (XR31)

Read/Write at I/O Address 3D7h
Index 31h



The three clock data registers (XR30-XR32) are programmed with the loop parameters to be loaded into the clock synthesizer. The Memory and Video clock VCO's both have programmable registers. Which of the VCO's is currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to this register is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data is written to registers XR30, and XR31 followed by a write to XR32. The completion of the write to XR32 causes data from all three registers is transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

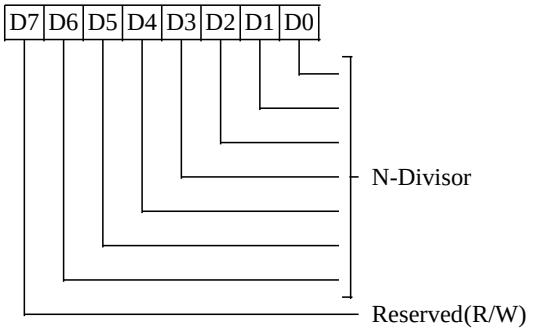
6–0 VCO M-Divisor

M-Divisor value calculated for the desired output frequency.

7 Reserved (R/W)

CLOCK N-DIVISOR REGISTER (XR32)

Read/Write at I/O Address 3D7h
Index 32h



The three clock data registers (XR30-XR32) are programmed with the loop parameters to be loaded into the clock synthesizer. The Memory and Video clock VCO's both have programmable registers. Which of the VCO's is currently selected for programming is determined by the Clock Register Program Pointer (XR33[5]).

The data written to this register is calculated based on the reference frequency, the desired output frequency, and characteristic VCO constraints as described in the Functional Description.

Data is written to registers XR30, and XR31 followed by a write to XR32. The completion of the write to XR32 causes data from all three registers is transferred to the VCO register file simultaneously. This prevents wild fluctuations in the VCO output during intermediate stages of a clock programming sequence.

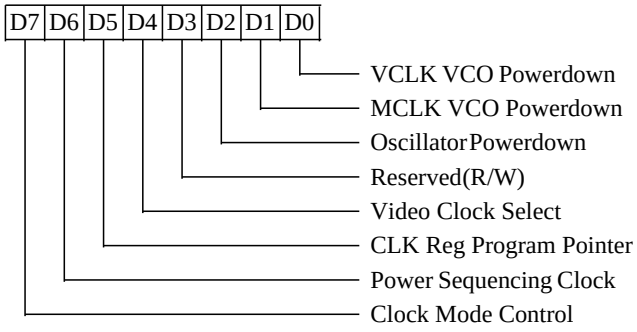
6–0 VCO N-Divisor

N-Divisor value calculated for the desired output frequency.

7 Reserved (R/W)

CLOCK CONTROL REGISTER (XR33)

Read/Write at I/O Address 3D7h
Index 33h



0 VCLK VCO Powerdown

0 VCLK VCO Enabled (default)
1 VCLK VCO Disabled

This bit is only effective if XR01[4] = 1.

1 MCLK VCO Powerdown

0 MCLK VCO Enabled (default)
1 MCLK VCO Disabled

This bit is only effective if XR01[4] = 1.

2 Oscillator Powerdown

0 OSC Enabled (default)
1 OSC Disabled

This bit is only effective if XR01[5] = 1 and XR33[6] = 1.

3 Reserved (R/W)

4 Video Clock Select

0 If XR01[4] = 1 (internal clock source), use output of VCLK VCO as video clock otherwise if XR04[4] = 0, use RCLK input as video clock (default).

1 If XR01[4] = 1 (internal clock source), use output of MCLK VCO divided by 2 as the video clock; otherwise if XR01[4]=0, then use MCLK input divided by 2 as the video clock.

5 Clock Register Program Pointer

This bit determines which of the VCO's is being programmed. Following a write to XR32 the data contained in XR32:30 is synchronously transferred to the appropriate VCO counter latch.

0 VCLK VCO selected
1 MCLK VCO selected

6 Power Sequencing Reference Clock

0 Use RCLK (reference clock) divided by 384 as panel power sequencing reference clock and Standby Mode display memory refreshes. For RCLK=14.31818 MHz, panel power sequencing clock would be 37.5 KHz (default).

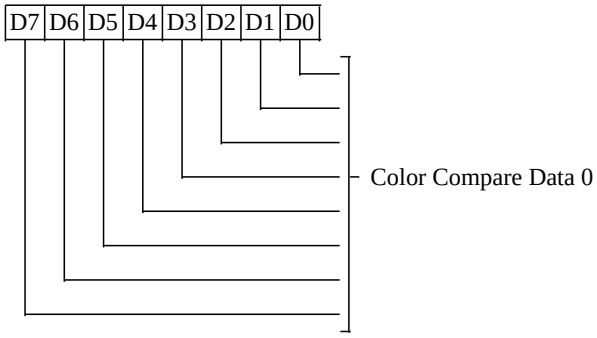
1 Use AA9 pin as 32 KHz clock input for panel power sequencing reference clock and Standby Mode display memory refreshes. Asymmetric DRAM option (XR05[3]=1) should not be enabled in this case.

7 Clock Mode Control

0 Clock 0 and Clock 1 default to 25.175 and 28.322 MHz respectively.

1 Clock 0 and Clock 1 default to 31.5 MHz and 35.5 MHz.

COLOR KEY REGISTER 0 (XR3A)
Read/Write at I/O Address 3D7h
Index 3Ah

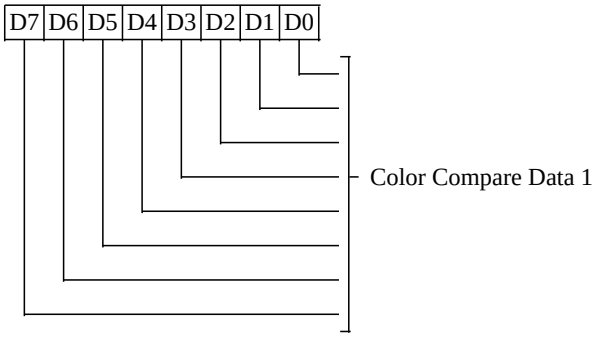


7-0 Color Compare Data 0

These bits are compared to the least significant 8 bits of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MCD15:0, CASCH# and CASCL# pins (and CA8-9, ACTI, ENABKL, AA9, and OEC# if 24-bit external video input is enabled (XR05[7]=1)). The logical masking and compare operations are described in the functional description.

The color comparison occurs before the RAMDAC. In 4BPP and 8BPP modes using palette LUT data, the LUT index is used in the comparison, not the 18BPP LUT data.

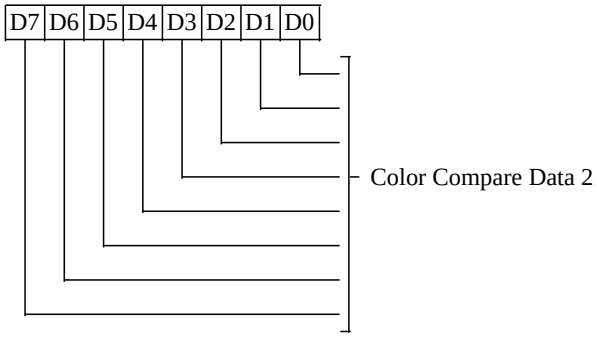
COLOR KEY REGISTER 1 (XR3B)
Read/Write at I/O Address 3D7h
Index 3Bh



7-0 Color Compare Data 1

These bits are compared to bits 15:8 of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MCD15:0, CASCH# and CASCL# pins (and CA8-9, ACTI, ENABKL, AA9, and OEC# if 24-bit external video input is enabled (XR05[7]=1)). The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP and 8BPP modes. This is accomplished by setting Color Mask Register 1 (XR3E) = 0FFh.

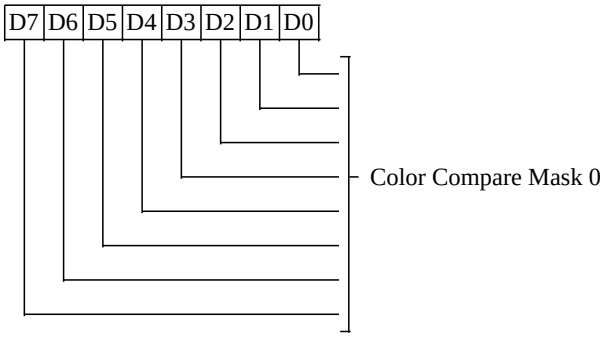
COLOR KEY REGISTER 2 (XR3C)
Read/Write at I/O Address 3D7h
Index 3Ch



7-0 Color Compare Data 2

These bits are compared to bits 23:16 of the background video stream. If a match occurs on all enabled bits (see Color Compare Mask Register XR3D) and the key is enabled (XR06[4]), external video is sent to the screen. External video is input on the MCD15:0, CASCH#, and CASCL# pins (and CA8-9, ACTI, ENABKL, AA9, and OEC# if 24-bit external video input is enabled (XR05[7]=1)). The logical masking and compare operations are described in the functional description. This register should be masked from participating in the comparison in 4BPP, 8BPP and 16BPP modes. It should only be used in 24BPP modes. This is accomplished by setting Color Mask Register 2 (XR3F) = 0FFh.

COLOR KEY MASK REGISTER 0 (XR3D)
Read/Write at I/O Address 3D7h
Index 3Dh

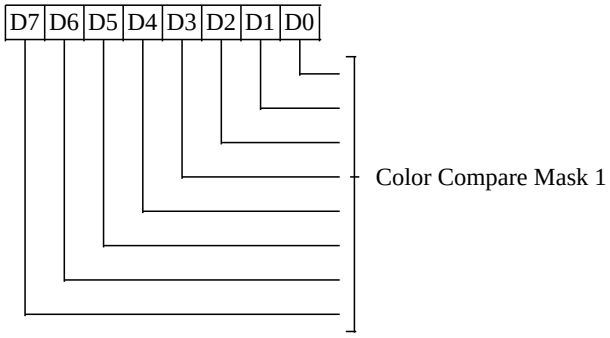


7-0 Color Compare Mask 0

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

COLOR KEY MASK REGISTER 1 (XR3E)
Read/Write at I/O Address 3D7h
Index 3Eh

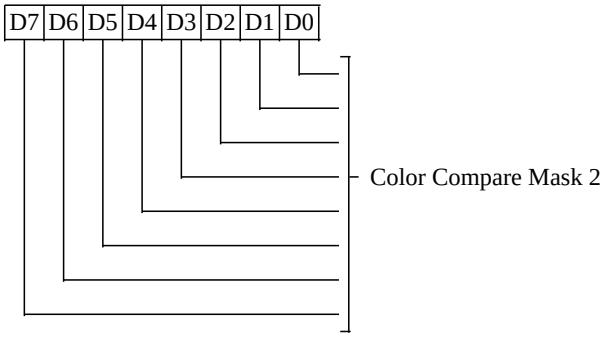


7-0 Color Compare Mask 1

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

COLOR KEY MASK REGISTER 2 (XR3F)
Read/Write at I/O Address 3D7h
Index 3Fh

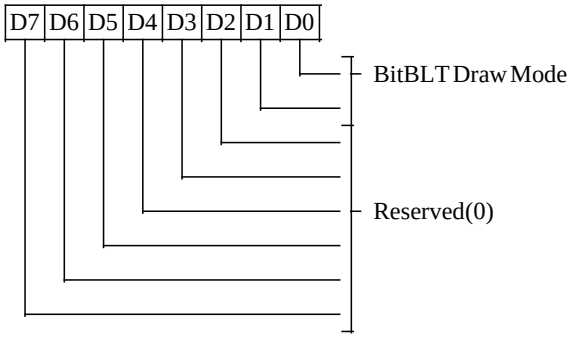


7-0 Color Compare Mask 2

This register is used to select which bits of the background video data stream are used in the comparison with the Color Compare Data 23:0. This register controls bits 7:0.

0 Data does participate in compare operation
1 Data does not participate in compare operation (masked)

BitBLTCONFIGREGISTER(XR40) (65545Only)
Read/Write at I/O Address 3D7h
Index 40h



1–0 BitBLT Draw Mode (65545 only)

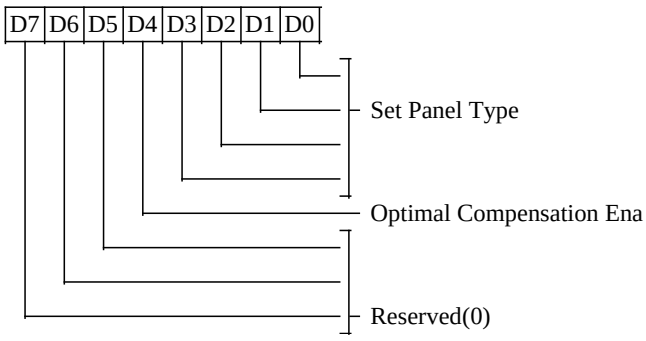
The 65545 supports two color depths in its drawing engine:

00 Reserved
01 8BPP
10 16BPP
11 Reserved

Note: 24BPP is handled in 8BPP mode. There is no nibble mode access for 4BPP modes.

7–2 Reserved (0)

SOFTWARE FLAGS REGISTER 2 (XR44)
Read/Write at I/O Address 3D7h
Index 44h



This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

3-0 Set Panel Type (40K BIOS Only)

00 Panel #1
01 Panel #2
02 Panel #3
03 Panel #4
04 Panel #5
05 Panel #6
06 Panel #7
07 Panel #8
08-0F Reserved

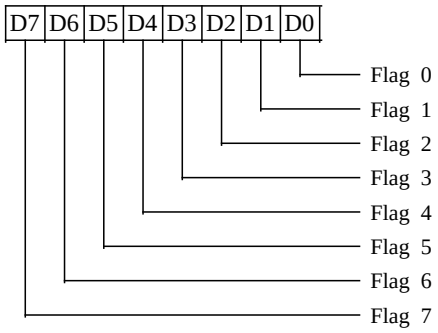
4 Optimal Compensation Enable

0 Disableoptimalcompensation
1 Enableoptimalcompensation

7-5 Reserved (0)

See also XR0F, XR2B, XR45 for definition of other software flags registers.

SOFTWARE FLAGS REGISTER 3 (XR45)
Read/Write at I/O Address 3D7h
Index 45h

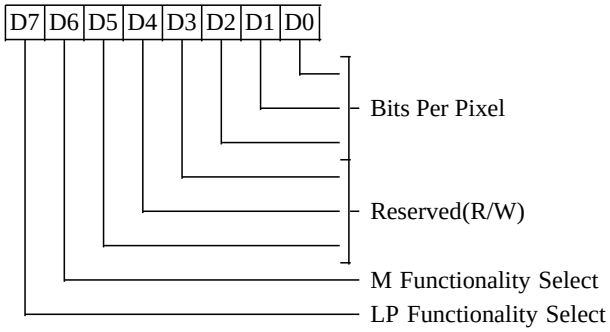


This register contains eight read-write bits which have no internal hardware function. All bits are reserved for use by BIOS and driver software. For reference, the functions of the bits of this register are currently defined as follows:

7-0 Flags (Reserved)

See also XR0F, XR2B, XR44 for definition of other software flags registers.

PANEL FORMAT REGISTER 2 (XR4F)
Read/Write at I/O Address 3D7h
Index 4Fh



This register is used only in flat panel mode.

2-0 Bits Per Pixel Selection

The value in this field, along with the dither and FRC settings, determines gray / color levels produced:

No FRC

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61
101	5	32	125
110	6	64	253
111	8	256	n/a

2-Frame FRC
(Color TFT or Monochrome Panels)

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
010	1	3	9
011	2	5	25
100	3	15	57
101	4	31	121

16-Frame FRC
(Color or Monochrome STN Panels)

	# of msbs Used to Generate Gray / Color Levels	Gray / Color Levels without Dithering	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61

The setting programmed into this field determines how many most-significant color-bits / pixel are used to generate flat panel video data. In general, 8 bits of monochrome data or 8 bits/color of RGB color data enter the flat panel logic for every dot clock. Not all of these bits, however, are used to generate output colors / gray scales, depending on the type of panel used, graphics / text mode, and the gray-scaling algorithm chosen (the actual number of bits used is indicated in the table above). If the VGA palette is used then a maximum of 6 bits/pixel (bits 7-2) (setting '110') should be used. If the VGA palette is bypassed then a maximum of 8 bits/pixel (bits 7-0) (setting '111) may be used. With 2-frame and 16-frame FRC, settings not listed in the tables above are undefined. Also note that settings which achieve higher gray / color levels may not necessarily produce acceptable display quality on some (or any) currently available panels. This document contains recommended settings for various popular panels that Chips & Technologies has found to produce acceptable results with those panels. Customers may modify these settings to achieve a better match with their requirements.

3-5 Reserved (R/W)

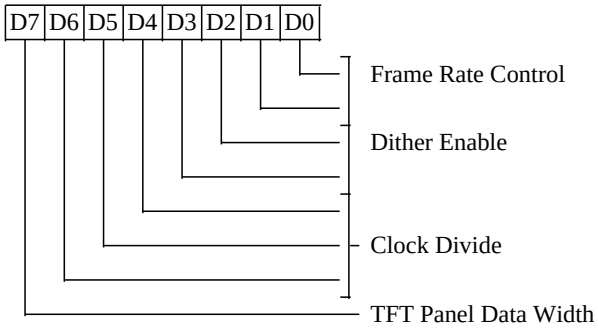
6 M Pin Select

0 M signal goes to the M pin (default on reset)
1 FP Display Enable (FP Blank#) signal goes to the M pin. Polarity is controlled by XR54[0].

7 LP Pin Select

0 FP HSync (LP) signal goes to the LP pin. Polarity is controlled by XR54[6] (default on reset).
1 FP Display Enable (FP Blank#) signal goes to the LP pin. Polarity is controlled by XR54[0].

PANEL FORMAT REGISTER 1 (XR50)
Read/Write at I/O Address 3D7h
Index 50h



This register is used only in flat panel mode.

1-0 Frame Rate Control (FRC)

FRC is gray scale simulation on a frame-by-frame basis to generate shades of gray or color on panels that do not support generation of gray / color levels internally.

00 No FRC. This setting may be used with all panels, especially for panels which can generate shades of gray / color internally.
01 16-frame FRC. This setting may be used for Color STN or Monochrome panels. One to four bits/pixel output to the panel are possible and therefore this setting is used only with panels which do not support internal gray scaling. This setting is used to simulate 16 gray / color levels per pixel. The bits per pixel are specified by XR4F[2-0]; valid values are 001, 010, 011, and 100.
10 2-frame FRC. This setting may be used for Color TFT or Monochrome panels. One to four bits/pixel output to the panel are possible and therefore this setting can also be used with panels that support internal gray scaling. Number of input bits used (specified in XR4F[2-0]) are one more than the number of output bits. Therefore, valid values for XR4F[2-0] are 010, 011, 100, and 101.
11 Reserved

3-2 Dither Enable

00 Disabledithering
01 Enable dithering for 256-color modes (AR10 bit-6 = 1 or XR28 bit 4 = 1)
10 Enable dithering for all modes
11 Reserved

6-4 Clock Divide (CD)

These bits specify the frequency ratio between the dot clock and the flat panel shift clock (SHFCLK) signal.

000 Shift Clock Freq = Dot Clock Freq. This setting is used to output 1 pixel per shift clock with a maximum of 8 bpp (bits/pixel) for single drive monochrome panels. For double drive color panels, this setting is used to output 2 2/3 4-bit pack pixels. FRC and dithering may be enabled.

001 Shift Clk Freq = 1/2 Dot Clock Freq. This setting is used to output 2 pixels per shift clock with a maximum of 8 bits/pixel for single drive monochrome panels and 4 bpp for single drive color panels. For double drive color panels, this setting is used to output 5-1/3 4-bit pack pixels. FRC and dithering can be enabled.

010 Shift Clk Freq = 1/4 Dot Clock Freq. This setting is used to output 4 pixels per shift clock with a maximum of 4 bpp for single drive mono panels and 2 bits/pixel for single drive color panels. For single drive color panels this setting is used to output 5-1/3 4-bit pack pixels. For double drive monochrome panels, this setting is used to output 8 pixels per shift clock with 1 bit/pixel. FRC and dithering can be enabled.

011 Shift Clk Freq = 1/8 Dot Clock Freq. This setting is used to output 8 pixels per shift clock with a maximum of 2 bpp for single drive mono panels and 1 bit/pixel for single drive color panels. For double drive mono panels, this setting is also used to output 16 pixels per shift clock with 1 bit/pixel. FRC and dithering can be enabled.

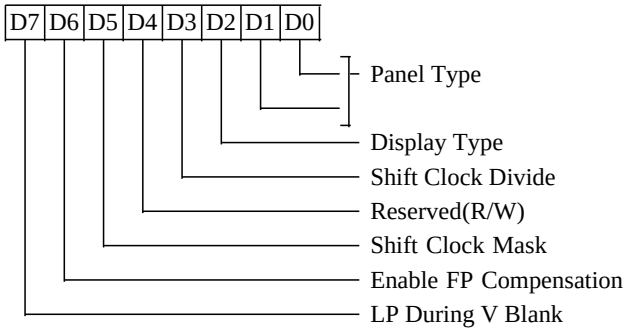
100 Shift Clk Freq = 1/16 Dot Clock Freq. This setting is used to output 16 pixels per shift clock with maximum of 1 bit/pixel for single drive monochrome panels. Dithering can also be enabled.

7 TFT Panel Data Width

This bit is effective only when TFT (active matrix) panels are used (XR50 bits 1-0=10).

0 16-bit color TFT interface (565 RGB)
1 24-bit color TFT interface (888 RGB)

DISPLAY TYPE REGISTER (XR51)
Read/Write at I/O Address 3D7h
Index 51h



1-0 Panel Type (PT)

These bits are effective for flat panel only.

00 Single Panel Single Drive (SS)
01 Reserved
10 Reserved
11 Dual Panel Double Drive (DD)

2 Display Type (DT)

This bit is effective for CRT and flat panel. This bit also controls the BLANK# output.

0 CRT display (default on reset)
BLANK# outputs CRT Blank
1 FP (Flat Panel) display
BLANK# outputs FP Blank

Note: There is no pin dedicated to output of BLANK#. Therefore this bit is ignored if BLANK# is not selected to be output on either the M or LP output pins.

3 Shift Clock Divide

This bit is effective for flat panel only.

0 Shift Clock to Dot Clock relationship expressed by XR50[6-4].
1 In this mode, the Shift Clock is further divided by 2 and different video data is valid on the rising and falling edges of Shift Clock.

4 Reserved (R/W)

5 Shift Clock Mask (SM)

This bit is effective for flat panel only.

0 Allow shift clock output to toggle outside the display enable interval
1 Force the shift clock output low outside the display enable interval

6 Enable FP Compensation (EFCP)

This bit is effective for flat panel only. It enables flat panel horizontal and vertical compensation depending on panel size, current display mode, and contents of the compensation registers.

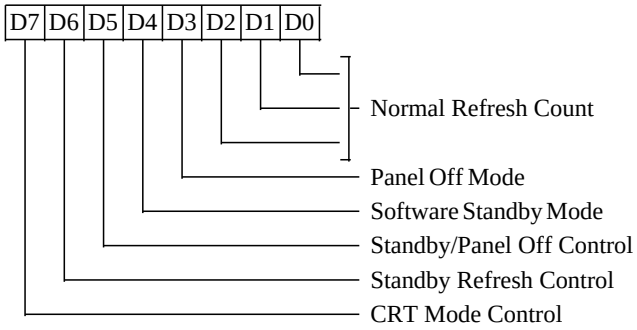
0 Disable FP compensation
1 Enable FP compensation

7 LP During Vertical Blank

This bit should be set only for SS panels which require FP HSync (LP) to be active during vertical blank time when XR54 bit-1 = 0 (e.g., Plasma / EL panels). This bit should be reset when using non-SS panels or when XR54 bit-1 = 1.

0 FP HSync (LP) is generated from internal FP Blank inactive edge
1 FP HSync (LP) is generated from internal FP Horizontal Blank inactive edge

POWER DOWN CONTROL REGISTER (XR52)
Read/Write at I/O Address 3D7h
Index 52h



2-0 FP Normal Refresh Count

These bits specify the number of memory refresh cycles to be performed per scanline. A minimum value of 1 should be programmed in this register.

3 Panel Off Mode

This bit provides a software alternative to enter Panel Off mode. Note that Panel Off mode will be effective in both CRT and flat panel modes of operation.

0 Normal mode (default on reset)
1 Panel Off mode

In Panel Off mode, the CRT / FP display memory interface is inactive but CPU interface and display memory refresh are still active. The internal RAMDAC is also inactive.

4 Software Standby Mode

This bit provides an alternative way to enter the Standby mode. When this bit is set, the chip enters Standby mode. To exit Standby mode, when this bit is set, the STNDBY# pin must be asserted and then reasserted. This bit will also be reset when the STNDBY# pin goes active (low).

0 Normal Mode (default on reset)
1 Standby Mode

5 Standby and Panel Off Control

This bit is effective in Flat Panel Mode during Standby and Panel Off modes (XR52[3] = 1 or (XR52[4] = 1 or STNDBY#, pin 178 is active (low)).

0 Video data and/or flat panel control signals are driven inactive (default on reset).
1 Video data and flat panel control signals pins are tri-stated with a weak internal pull-down.

Note: XR61 bit-7 controls the inactive level for video data in text mode; XR63 bit-7 controls the inactive level for video data in graphics mode:

0 = low when inactive
1 = high when inactive

Note: This bit does not affect the HSYNC and VSYNC pins. In Standby and Panel Off modes, HSYNC and VSYNC will be driven low.

6 Standby Refresh Control

This bit is effective only in Standby mode (STNDBY# pin low). Standby mode is effective for both CRT and flat panel modes. In Standby mode, CPU interface to display memory and internal registers is inactive. The CRT / FP display memory interface, video data and timing signals, and internal RAMDAC are inactive (all CRT and flat panel video control and data pins are 3-stated). Display memory refresh is controlled by this bit.

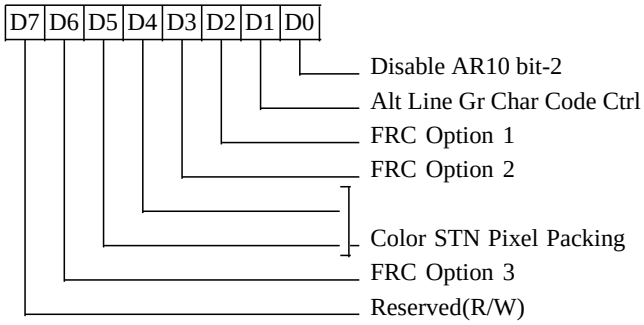
0 Self-Refresh DRAM support.
1 Display memory refresh frequency is derived from the 32KHz input or RCLK (14.31818MHz Reference Clock) divided per the value in XR5F.

7 CRT Mode Control

This bit is effective in CRT mode only (non-simultaneous CRT and flat panel) (XR51 bit-2 = 0).

0 Video data and flat panel control signals are 3-stated with weak internal pull-down (default on reset).
1 Video data and flat panel control signals are inactive.

PANEL FORMAT REGISTER 3 (XR53)
Read/Write at I/O Address 3D7h
Index 53h



0 Disable AR10 Bit-2

0 Use AR10 bit-2 for Line Graphics control (default on Reset).
1 Use XR53 bit-1 instead of AR10 bit-2 for Line Graphics control

1 AlternateLineGraphicsCharacterControl

This bit is effective only if bit-0 = 1.

0 Ninth pixel of line graphics character is set to the background color
1 Ninth pixel of line graphics character is identical to the eighth pixel

2 FRC Option 1 (always program to 1)

3 FRC Option 2 (always program to 1)

5-4 Color STN Pixel Packing

This field determines the type of pixel packing (the RGB pixel output sequence) for color STN panels. These bits should be programmed only when color STN panels are used. These bits must be programmed to 00 for monochrome panels or color TFT panels.

00 3-bit Pack. XR50 bits 6-4 can be 000, 001, or 010.
01 4-bit Pack. For SS Color STN panels, XR50 bits 6-4 can be 000, 001, or 010. For DD panels, XR50 bits 6-4 may be set to 000 or 001.
10 Reserved
11 Extended 4-bit Pack. XR50 bits 6-4 must be programmed to 001. This setting may be used for 8-bit interface Color STN SS panels only.

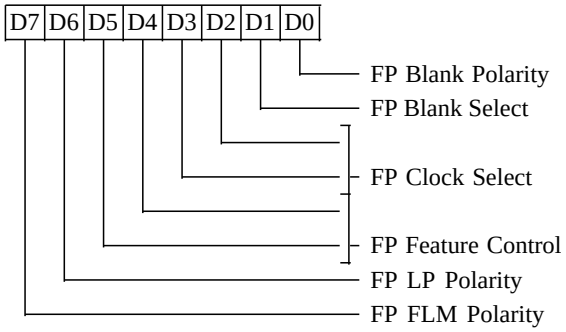
6 FRC Option 3

This bit affects 2-frame FRC only

0 FRC data changes every frame
1 FRC data changes every other frame

7 Reserved (R/W)

PANEL INTERFACE REGISTER (XR54)
Read/Write at I/O Address 3D7h
Index 54h



This register is used only in flat panel modes.

0 FP Blank Polarity

This bit controls the polarity of the BLANK# pin in flat panel mode. In CRT mode, XR28 bit-0 controls polarity of the BLANK# pin.

0 Positive polarity
1 Negative polarity

1 FP Blank Select

This bit controls the BLANK# pin output in flat panel mode. In CRT mode, XR28 bit-1 controls the BLANK# output. This bit also affects operation of the flat panel video logic, generation of the FP HSync (LP) pulse signals, and masking of the Shift Clock.

0 The BLANK# pin outputs both FP Vertical and Horizontal Blank. In 480-line DD panels, this option will generate exactly 240 FP HSync (LP) pulses.
1 The BLANK# pin outputs only FP Horizontal Blank. During FP Vertical Blank, the flat panel video logic will be active, the FP HSync (LP) pulse will be generated, and Shift Clock can not be masked. Note however that Shift Clock can still be masked during FP Horizontal Blank.

Note: The signal polarity selected by bit-0 is applicable for either selection.

3-2 FP Clock Select Bits 1-0

Select flat panel dot clock source. These bits are used instead of Miscellaneous Output Register (MSR) bits 3-2 in flat panel mode. See description of MSR bits 3-2.

5-4 FP Feature Control Bits 1-0

Select flat panel dot clock source. These bits are used instead of Feature Control Register (FCR) bits 1-0 in flat panel mode. See description of FCR bits 1-0.

6 FP HSync (LP) Polarity

This bit controls the polarity of the flat panel HSync (LP) pin.

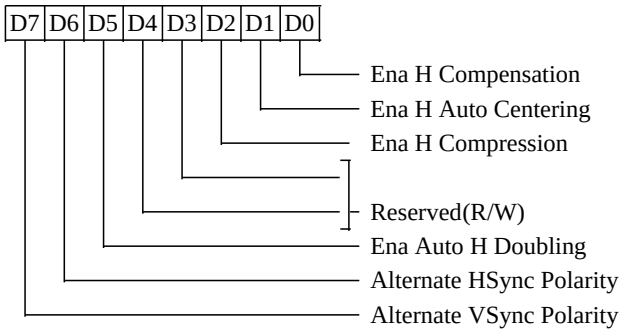
0 Positive polarity
1 Negative polarity

7 FP VSync (FLM) Polarity

This bit controls the polarity of the flat panel VSync (FLM) pin.

0 Positive polarity
1 Negative polarity

HORIZONTAL COMPENSATION REGISTER (XR55)
Read/Write at I/O Address 3D7h
Index 55h



This register is used only in flat panel modes when flat panel compensation is enabled (XR51 bit-6 = 1).

0 EnableHorizontalCompensation(EHCP)

0 Disablehorizontalcompensation
1 Enablehorizontalcompensation

1 Enable Automatic Horizontal Centering (EAHC) (effective only if bit-0 is 1)

0 Enable non-automatic horizontal centering. The Horizontal Centering Register is used to specify the left border. If no centering is desired then the Horizontal Centering Register can be programmed to 0.
1 Enable automatic horizontal centering. Horizontal left and right borders will be computed automatically.

2 EnableTextModeHorizontalCompression (ETHC)(this bit is effective only if bit-0 is 1 in flat panel text mode). Setting this bit will turn on text mode horizontal compression regardless of horizontal display width or horizontal panel size.

0 Text mode horizontal compression off
1 Text mode horizontal compression on. 8-dot text mode is forced when 9-dot text mode is specified (SR01 bit-0 = 0 or Hercules text).

Note: This bit affects the horizontal pixel panning logic. When text mode horizontal compression is active, programming 9-bit panning will result in 8-bit panning.

4-3 Reserved (R/W)

5 Enable Automatic Horizontal Doubling (EAHD)(this bit is effective if bit-0 is 1)

0 Disable Automatic Horizontal Doubling. Horizontal doubling will only be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation.
1 Enable Automatic Horizontal Doubling. Horizontal doubling will be performed for flat panels when SR01 bit-3 = 1 in any emulation mode or when 3B8/3D8 bit-0 & 3B8/3D8 bit-4 = 0 in CGA emulation or when the Horizontal Display width (CR01) is equal to or less than half of the Horizontal Panel Size (XR18).

6 Alternate CRT HSync Polarity

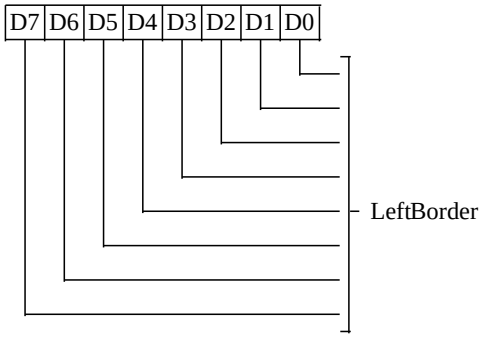
0 Positive
1 Negative

7 Alternate CRT VSync Polarity

0 Positive
1 Negative

Note: bits 6 and 7 above are used in flat panel mode (XR51 bit-2 = 1) instead of MSR bits 6 and 7). This is primarily used for simultaneous CRT / Flat Panel display.

HORIZONTALCENTERINGREGISTER(XR56)
Read/Write at I/O Address 3D7h
Index 56h

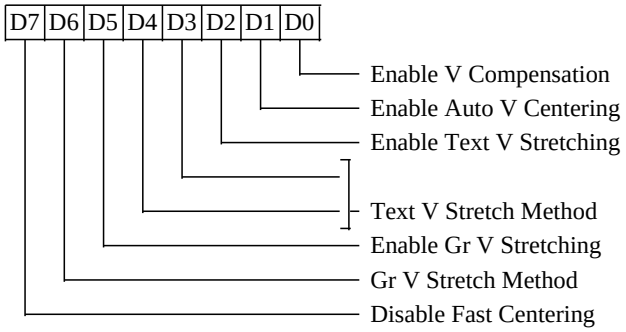


This register is used only in flat panel modes when non-automatic horizontal centering is enabled.

7-0 Horizontal Left Border (HLB)

Programmed Value (in character clocks)
= Width of Left Border – 1

VERTICAL COMPENSATION REGISTER (XR57)
Read/Write at I/O Address 3D7h
Index 57h



This register is used only in flat panel modes when flat panel compensation is enabled.

0 Enable Vertical Compensation (EVCP)

0 Disable vertical compensation
1 Enable vertical compensation

1 Enable Automatic Vertical Centering (EAVC)

This bit is effective only if bit-0 is 1.

0 Enable non-automatic vertical centering. The Vertical Centering Register is used to specify the top border. If no centering is desired then the Vertical Centering Register can be programmed to 0.
1 Enable automatic vertical centering. Vertical top and bottom borders will be computed automatically.

2 Enable Text Mode Vertical Stretching (ETVS)

This bit is effective only if bit-0 is 1.

0 Disable text mode vertical stretching; graphics mode vertical stretching is used if enabled.
1 Enable text mode vertical stretching

4-3 Text Mode Vertical Stretching (TVS1-0)

These bits are effective if bits 2 and 0 are 1.

00 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, DS, LI.
01 Double Scanning (DS) and Line Insertion (LI) with the following priority: DS+LI, LI, DS.
10 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, DS, TF.
11 Double Scanning (DS) and TallFont (TF) with the following priority: DS+TF, TF, DS.

5 Enable Vertical Stretching (EVS)

This bit is effective only if bit-0 is 1.

0 Disable vertical stretching
1 Enable vertical stretching

6 Vertical Stretching (VS)

Vertical Stretching can be enabled in both text and graphics modes. This bit is effective only if bits 5 and 0 are 1.

0 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, DS, LR.
1 Double Scanning (DS) and Line Replication (LR) with the following priority: DS+LR, LR, DS.

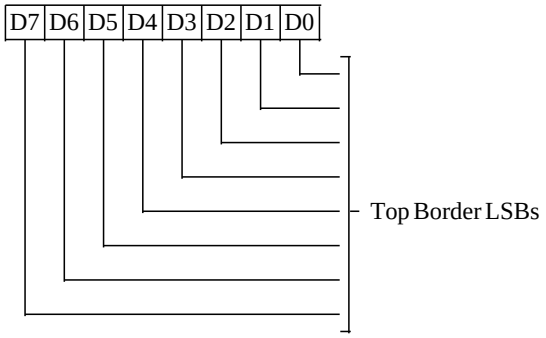
7 Disable Fast Centering

This bit is effective only if XR58[1-0] = 11.

0 Enable Fast Centering
1 Disable Fast Centering

VERTICAL CENTERING REGISTER (XR58)

Read/Write at I/O Address 3D7h
Index 58h



This register is used only in flat panel modes when non-automatic vertical centering is enabled.

7-0 Vertical Top Border LSBs (VTB7-0)

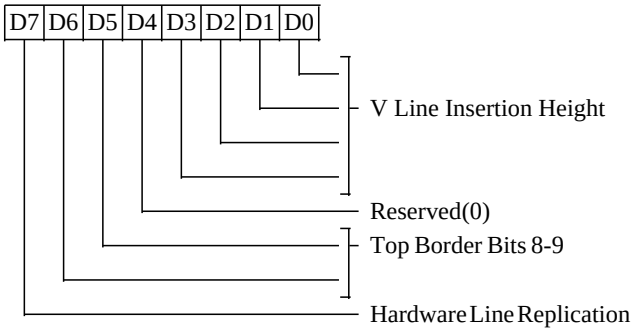
Programmed value:

Top Border Height (in scan lines) – 1

This register contains the eight least significant bits of the programmed value of the Vertical Top Border (VTB). The two most significant bits are in the Vertical Line Insertion Register (XR59).

VERTICAL LINE INSERTION REGISTER (XR59)

Read/Write at I/O Address 3D7h
Index 59h



This register is used only in flat panel text mode when vertical line insertion is enabled.

3-0 Vertical Line Insertion Height (VLIH3-0)

Programmed Value:

Number of Insertion Lines – 1

The value programmed in this register - 1 is the number of lines to be inserted between the rows. Insertion lines are never double scanned even if double scanning is enabled. Insertion lines use the background color.

4 Reserved (0)

6-5 Vertical Top Border MSBs (VTB9-8)

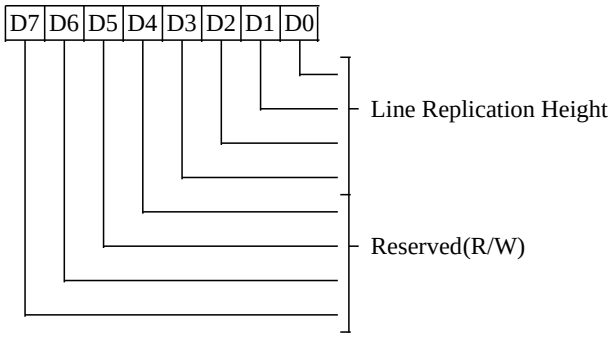
This register contains the two most significant bits of the programmed value of the Vertical Top Border (VTB). The eight least significant bits are in the Vertical Centering Register (XR58).

7 Hardware Line Replication

This bit is effective in text mode when Line Replication is selected (XR57[2] = 1). Hardware line replication, when enabled, replicates lines to display a 19-line character from a 16-line font as specified in XR28 bit-7.

0 Normal text mode line replication
1 Hardware line replication is enabled

VERTICAL LINE REPLICATION REGISTER (XR5A)
Read/Write at I/O Address 3D7h
Index 5Ah



This register is used only in flat panel text or graphics modes when vertical line replication is enabled.

3-0 Vertical Line Replication Height (VLRH)

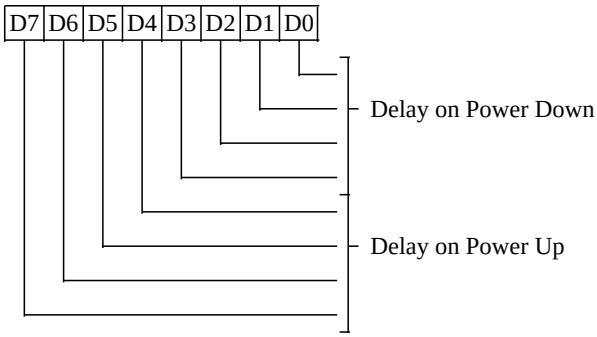
Programmed Value = Number of Lines Between Replicated Lines – 1

Double scanned lines are also counted.

In other words, if this field is programmed with '7', every 8th line will be replicated.

7-4 Reserved (R/W)

PANEL POWER SEQUENCING DELAY REGISTER (XR5B)
Read/Write at I/O Address 3D7h
Index 5Bh



This register is used only in flat panel modes. The generation of the clock for panel power sequencing logic is controlled by XR33[6]. The delay intervals below assume a 37.5 KHz clock generated by the internal clock synthesizer. If the 32KHz input is used, the delay intervals should be scaled accordingly.

3-0 Power Down Delay

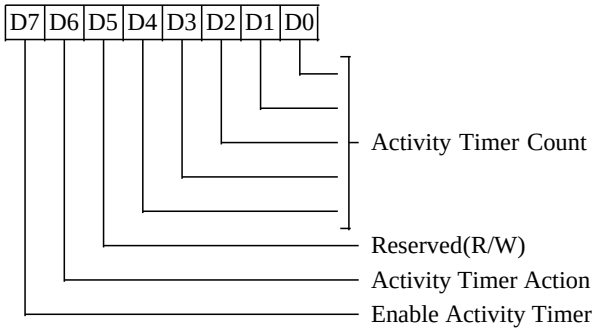
Programmable value of panel power-sequencing during power down. This value can be programmed up to 459 milliseconds in increments of 29 milliseconds. A value of 0 is undefined.

7-4 Power Up Delay

Programmable value of panel power sequencing during power up. This value can be programmed up to 54 milliseconds in increments of 3.4 milliseconds. A value of 0 is undefined.

ACTIVITY TIMER CONTROL REGISTER (XR5C)

Read/Write at I/O Address 3D7h
Index 5Ch



This register is used to control Activity timer functionality. The activity timer is an internal counter that starts counting from a value programmed into this register (see bits 0-4 below) and is reset back to that count by read or write accesses to graphics memory or I/O. If no accesses occur, the counter counts till the end of its programmed interval and activates either the ENABKL pin or Panel Off mode (as selected by bit-6 below). The timer count does not have to be reloaded once programmed and the timer enabled: any access to the chip with the timer timed out (ENABKL active or Panel Off mode active) will reset the timer and the ENABKL pin de-activated (or Panel Off mode exited, whichever is selected). The activity timer uses the same clock as power sequencing which is controlled by XR33[6]. The delay intervals below assume a 35.7 KHz clock, if an external 32KHz input is used, the delay is scaled accordingly.

4-0 Activity Timer Count

For a 35.7 KHz clock the counter granularity is approximately 25.6 seconds. The minimum programmed value of 1 results in 25.6 second delay and the maximum count of 32 results in a delay of 13.7 minutes. If the clock input on pin 154 (AA9) is other than 32 KHz, the delay should be scaled accordingly.

5 Reserved (R/W)

6 Activity Timer Action

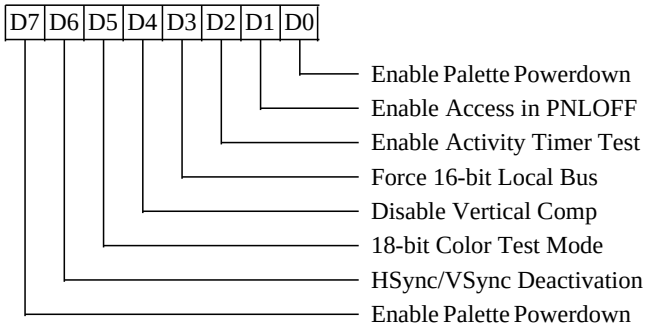
0 When the activity timer count is reached, the ENABKL pin is activated (driven low to turn the backlight off)
1 When the activity timer count is reached, Panel Off mode is entered.

7 Enable Activity Timer

0 Disable activity timer (default on reset)
1 Enable activity timer

See also XR5D bit-2.

FP DIAGNOSTIC REGISTER (XR5D)
Read/Write at I/O Address 3D7h
Index 5Dh



0 EnablePanel-OffVGAPalettePowerdown

0 Disable VGA Palette powerdown in Panel Off Mode (default on reset)
1 Enable VGA Palette powerdown in Panel Off mode

1 Enable Panel-Off VGA Palette Access

This bit is effective when bit 0=1 or bit 7=1.

0 Disable CPU access to VGA Palette in Panel Off Mode (default on reset)
1 Enable CPU access to VGA Palette in Panel Off Mode

2 Enable Activity Timer Test

0 Disable Activity Timer test mode (default on reset)
1 Enable Activity Timer test mode

3 Force 16-Bit Local Bus

This bit is effective when 32-bit local bus and 16-bit memory interface are used during font load.

0 Do not force 16-bit local bus when loading font (default on reset)
1 Force 16-bit local bus when loading font

4 Disable Vertical Compensation

0 Vertical compensation can be enabled in all cases (default on reset)
1 Disable vertical compensation if Vertical Display Enable End equals Vertical Panel Size.

5 18-bit Color TFT Test Mode

0 Disable 18-bit color TFT test mode (default on reset)
1 Enable 18-bit color TFT test mode

6 PreventHSYNCandVSYNCDeactivation

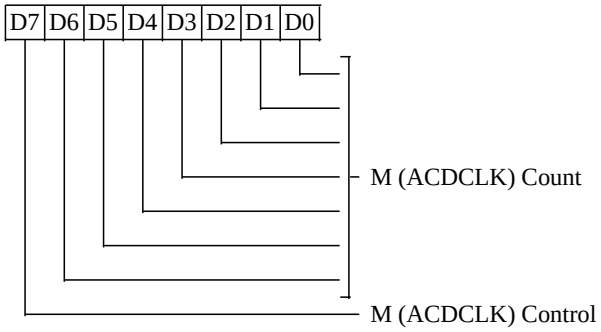
0 Allow HSYNC and VSYNC to be deactivated when XR06[1] = 1 (default on reset)
1 Prevents HSYNC and VSYNC from being deactivated when XR06[1] = 1.

7 EnablePalettePowerdowninBypassMode

0 Disable VGA palette powerdown when XR06[5]=1
1 Enable VGA palette powerdown when XR06[5]=1 and XR06[1]=1

M (ACDCLK) CONTROL REGISTER (XR5E)

Read/Write at I/O Address 3D7h
Index 5Eh



This register is used only in flat panel mode.

6-0 M (ACDCLK) Count (ACDCNT)

These bits define the number of HSyncs between adjacent phase changes on the M (ACDCLK) output. These bits are effective only when bit 7 = 0 and the contents of this register are greater than 2.

Programmed Value = Actual Value – 2

7 M (ACDCLK) Control

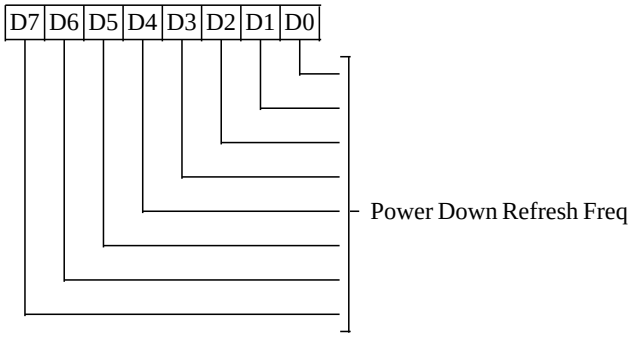
0 The M (ACDCLK) phase changes depending on bits 0-6 of this register

1 The M (ACDCLK) phase changes every frame if the frame accelerator is not used. If the frame accelerator is used, the M (ACDCLK) phase changes every other frame.

If XR4F bit-6 is programmed to one to enable flat panel DE / BLANK# to be output on the M (ACDCLK) pin, the contents of this register will be ignored.

POWER DOWN REFRESH REGISTER (XR5F)

Read/Write at I/O Address 3D7h
Index 5Fh



7-0 Power Down Refresh Frequency

These bits define the frequency of memory refresh cycles in power down (standby) mode (STNDBY# pin low). CAS-Before-RAS (CBR) refresh cycles are performed.

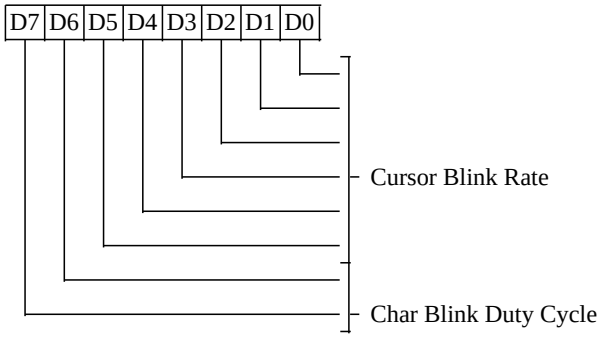
If XR52 bit-6 = 1, the interval between two refresh cycles is determined by bits 0-3 of this register per the table below. Bits 4-7 of this register are reserved for future use in this mode (and should be programmed to 0).

3 2 1 0	Approximate Refresh Interval
0 0 0 0	16 usec / cycle
0 0 0 1	47 usec / cycle
0 0 1 0	63 usec / cycle
0 0 1 1	78 usec / cycle
0 1 0 0	94 usec / cycle
0 1 0 1	109 usec / cycle
0 1 1 0	125 usec / cycle
0 1 1 1	141 usec / cycle
1 0 0 0	156 usec / cycle

These refresh intervals assume a 32 KHz clock. If the internal clock is used, the refresh interval is scaled accordingly.

If XR52 bit-6 = 0, a value of 0 causes no refresh to be performed. Self-Refresh DRAMs should be used in this case.

BLINK RATE CONTROL REGISTER (XR60)
Read/Write at I/O Address 3D7h
Index 60h



This register is used in all modes.

5-0 Cursor Blink Rate

These bits specify the cursor blink period in terms of number of VSyncs (50% duty cycle). In text mode, the character blink period and duty cycle is controlled by bits 7-6 of this register. These bits default to 000011 (decimal 3) on reset which corresponds to eight VSyncs per cursor blink period per the following formula (four VSyncs on and four VSyncs off):

Programmed Value = (Actual Value) / 2 – 1

Note: In graphics mode, the pixel blink period is fixed at 32 VSyncs per cursor blink period with 50% duty cycle (16 on and 16 off).

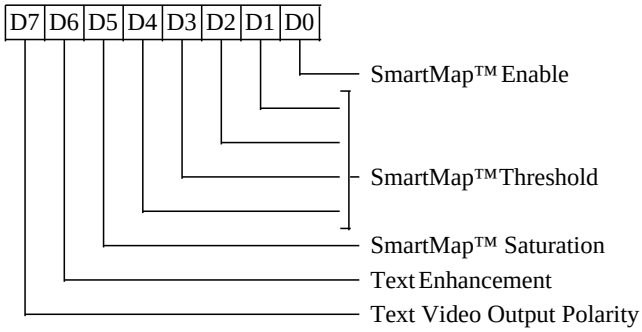
7-6 Character Blink Duty Cycle

These bits specify the character blink (also called 'attribute blink') duty cycle in text mode.

7	6	Character Blink Duty Cycle	
0	0	50%	
0	1	25%	
1	0	50%	(default on Reset)
1	1	75%	

For setting 00, the character blink period is equal to the cursor blink period. For all other settings, the character blink period is twice the cursor blink period (character blink is twice as slow as cursor blink).

SMARTMAP™ CONTROL REGISTER (XR61)
Read/Write at I/O Address 3D7h
Index 61h



This register is used in flat panel text mode only.

0 SmartMap™ Enable

0 Disable SmartMap™, use color lookup table and use internal RAMDAC palette if enabled (XR06 bit-2 = 1).

1 Enable SmartMap™, bypass both color lookup table and internal RAMDAC palette in flat panel text mode. Although color lookup table is bypassed, translation of 4 bits/pixel data to 6 bits/pixel data is still performed depending on AR10 bit-1 (monochrome / color display) as follows:

Output	AR10 bit-1 = 0	AR10 bit-1 = 1
Out0	In0	In0
Out1	In1	In1
Out2	In2	In2
Out3	In3	In0+In1+In2+In3
Out4	In3	In3
Out5	In3	In3

Note: This bit does not affect CRT text / graphics mode or flat panel graphics mode; i.e.: the color lookup table is always used, and similarly the internal RAMDAC palette is used if enabled.

4-1 SmartMap™ Threshold

These bits are used only in flat panel text mode when SmartMap™ is enabled (bit-0 = 1). They define the minimum difference between the foreground and background colors. If the difference is less than this threshold, the colors are separated by adding and subtracting the shift values (XR62) to the foreground and background colors. However, if the foreground and background color values are the same, then the color values are not adjusted.

5 SmartMap™ Saturation

This bit is used only in flat panel text mode when SmartMap™ is enabled (bit-0 = 1). It selects the clamping level after the color addition/subtraction.

0 The color result is clamped to the maximum and minimum values (0Fh and 00h respectively)

1 The color result is computed modulo 16 (no clamping)

6 Text Enhancement

This bit is used only in flat panel text mode.

0 Normal text
1 Text attribute 07h and 0Fh are reversed to maximize the brightness of the normal DOS prompt

Note: This bit should be set to 0 if XR63[6] is set to 1. Conversely, if this bit is set to 1, XR63[6] should be set to 0.

7 Text Video Output Polarity (TVP)

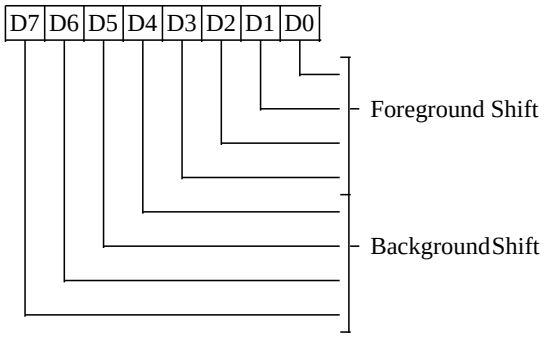
This bit is effective for flat panel text mode only.

0 Normal polarity
1 Inverted polarity

Note: Graphics video output polarity is controlled by XR63 bit-7 (GVP).

SMARTMAP™ SHIFT PARAMETER REGISTER (XR62)

Read/Write at I/O Address 3D7h
Index 62h



This register is used in flat panel text mode when SmartMap™ is enabled (XR61 bit-0 = 1).

3-0 Foreground Shift

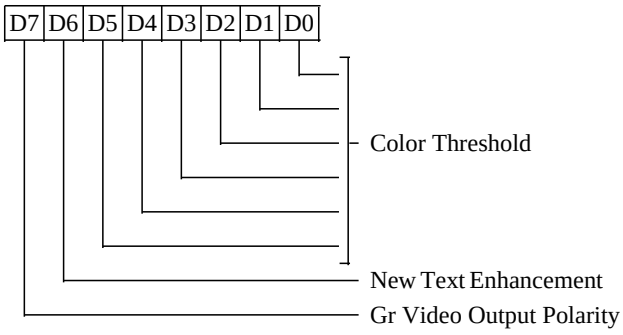
These bits define the number of levels that the foreground color is shifted when the foreground and background colors are closer than the SmartMap™ Threshold (XR61 bits 1-4). If the foreground color is "greater" than the background color, then this field is added to the foreground color. If the foreground color is "smaller" than the background color, then this field is subtracted from the foreground color.

7-4 Background Shift

These bits define the number of levels that the background color is shifted when the foreground and background colors are closer than the SmartMap™ Threshold (XR61 bits 1-4). If the background color is "greater" than the foreground color, then this field is added to the background color. If the background color is "smaller" than the foreground color, then this field is subtracted from the background color.

SMARTMAP™ COLOR MAPPING CONTROL REGISTER (XR63)

Read/Write at I/O Address 3D7h
Index 63h



5-0 Color Threshold

These bits are effective for monochrome (XR51 bit-5 = 1) single/double drive flat panel with 1 bit/pixel (XR50 bits 4-5 = 11) without FRC (XR50 bits 0-1 = 11). They specify the color threshold used to reduce 6-bit video to 1-bit video color. Color values equal to or greater than the threshold are mapped to 1 and color values less than the threshold are mapped to 0.

6 New Text Enhancement

If set this bit enables new text enhancement that does not affect the CRT display. If this bit is set to 1, the old text enhancement bit (XR61[6]) must be set to 0. Conversely, if XR61[6] is 1 then this bit should be set to 0. Reset defaults this bit to 1.

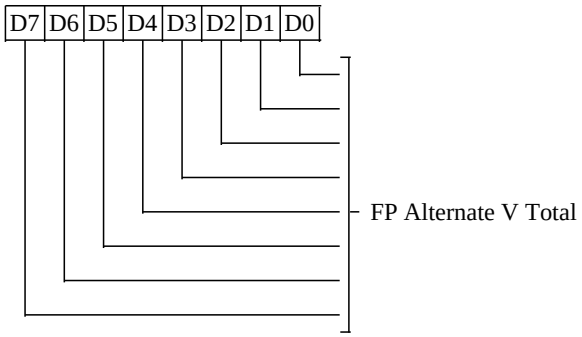
7 Graphics Video Output Polarity (GVP)

This bit is effective for CRT and flat panel graphics mode only.

0 Normal polarity
1 Inverted polarity

Note: Text video output polarity is controlled by XR61 bit-7 (TVP).

FP ALTERNATE VERTICAL TOTAL REGISTER (XR64)
Read/Write at I/O Address 3D7h
Index 64h



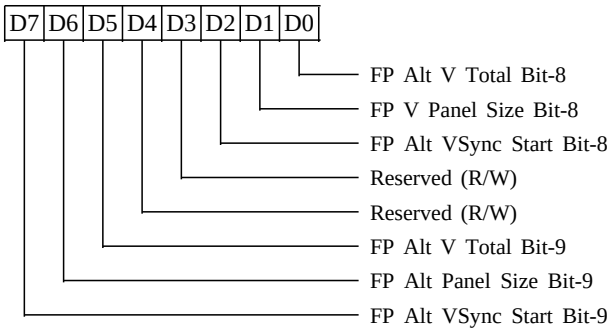
This register is used in all flat panel modes.

7-0 FP Alternate Vertical Total

The contents of this register are 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. The vertical total value specifies the total number of scan lines per frame. Similar to CR06.

Programmed Value = Actual Value – 2

FP ALTERNATE OVERFLOW REGISTER (XR65)
Read/Write at I/O Address 3D7h
Index 65h



This register is used in all flat panel modes.

0 FP Alternate Vertical Total Bit-8

1 FP Vertical Panel Size Bit-8

2 FP Alternate Vertical Sync Start Bit-8

3 Reserved (R/W)

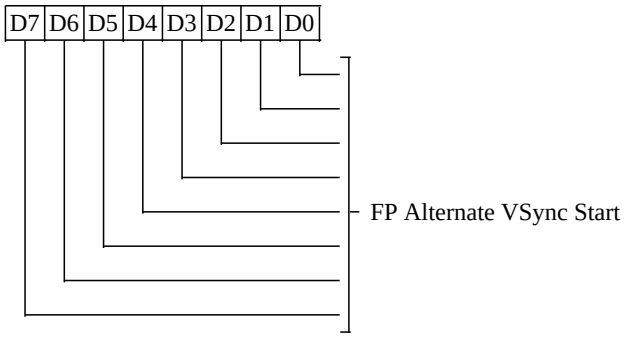
4 Reserved (R/W)

5 FP Alternate Vertical Total Bit-9

6 FP Vertical Panel Size Bit-9

7 FP Alternate Vertical Sync Start Bit-9

FP ALTERNATE VERTICAL SYNC START REGISTER (XR66)
Read/Write at I/O Address 3D7h
Index 66h



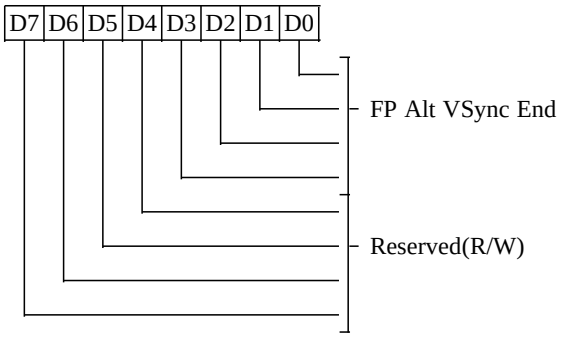
This register is used in all flat panel modes.

7-0 FP Alternate Vertical Sync Start

The contents of this register are the 8 low order bits of a 10-bit value. Bits 9 and 10 are defined in XR65. This value defines the scan line position at which vertical sync becomes active. Similar to CR10.

Programmed Value = Actual Value – 1

FP ALTERNATE VERTICAL SYNC END REGISTER (XR67)
Read/Write at I/O Address 3D7h
Index 67h



This register is used in all flat panel modes.

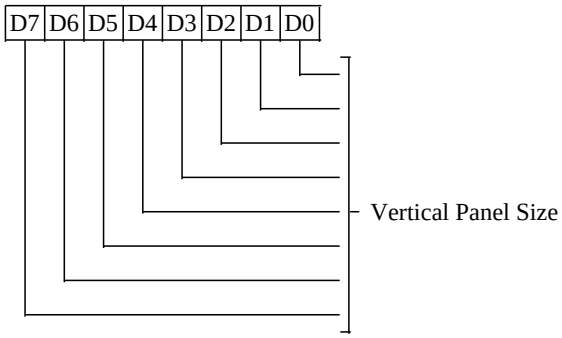
3-0 FP Alternate Vertical Sync End

The lower 4 bits of the scan line count that defines the end of vertical sync. Similar to CR11. If the vertical sync width desired is N lines, the programmed value is:

(contents of XR66 + N) ANDed with 0FH

7-4 Reserved (R/W)

VERTICAL PANEL SIZE REGISTER (XR68)
Read/Write at I/O Address 3B7h/3D7h
Index 68h



This register is used in all flat panel modes.

7-0 Vertical Panel Size

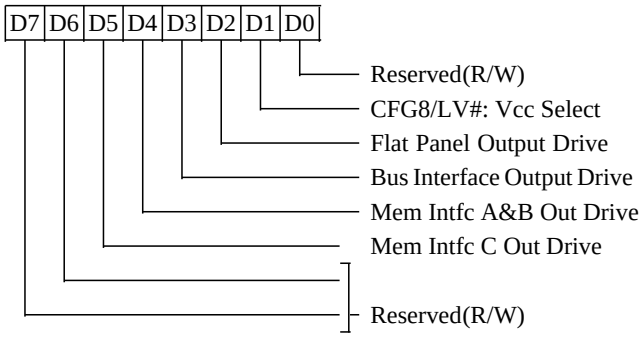
The contents of this register define the number of scan lines per frame.

Programmed Value = Actual Value – 1

Panel size bits 8-9 are defined in overflow register XR65.

Note: Programming lower drive for 3.3V operation results in lower than rated output drive. Programming higher output drive for 5V operation results in higher than rated output drive.

PROGRAMMABLEOUTPUTDRIVEREGISTER (XR6C)
Read/Write at I/O Address 3B7h/3D7h
Index 6Ch



This register is used to control the output drive of the bus, video, and memory interface pins.

0 Reserved (R/W)

1 CFG8/LV# - Internal Logic Vcc Selection

This bit determines pad input threshold. On the trailing edge of reset, this bit will latch the state of AA8 pin (CFG8).

0 VCC for internal logic (IVCC) is 3.3V
1 VCC for internal logic (IVCC) is 5V (Default)

2 Flat Panel Interface Output Drive Select

0 Lower drive (Default) (Use for DVCC=5V)
1 Higher drive (Use for DVCC=3.3V)

3 Bus Interface Output Drive Select

0 Higher drive (Default) (Use for BVCC=3.3V)
1 Lower drive (Use for BVCC=5V)

4 MemoryInterfaceA&BOutputDriveSelect

This bit affects memory interface groups A & B control pins: RASB#, CASBH#, CASBL#, WEB#, OEB#, MAD[15:0] and MBD[15:0]

0 Lower drive (Default) (Use for MVCCA/B=5V)
1 Higher drive (Use for MVCCA/B=3.3V)

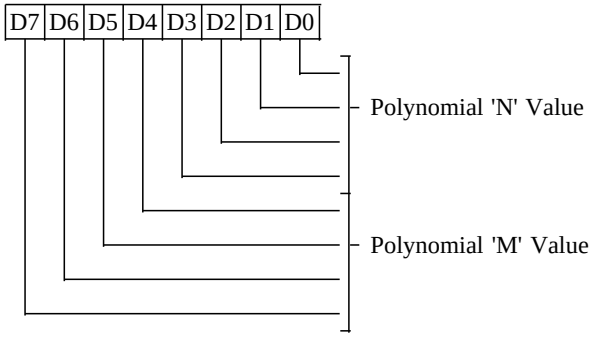
5 Memory Interface C Output Drive Select

This bit affects memory interface group C control pins: RASC#, CASCH#, CASCL#, WEC#, OEC#, and MCD15:0.

0 Lower drive (Default) (Use for MVCCC=5V)
1 Higher drive (Use for MVCCC=3.3V)

7-6 Reserved (R/W)

POLYNOMIAL FRC CONTROL REGISTER (XR6E)
Read/Write at I/O Address 3D7h
Index 6Eh



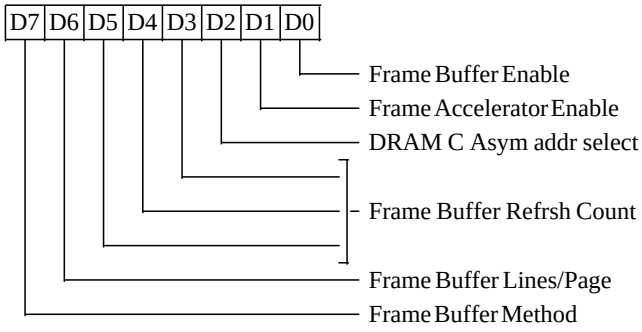
This register is effective in flat panel mode when polynomial FRC is enabled (see XR50 bits 0-1). It is used to control the FRC polynomial counters. The values in the counters determine the offset in rows and columns of the FRC count. These values are usually determined by trial and error.

3-0 Polynomial 'N' value

7-4 Polynomial 'M' value

This register defaults to '10111101' on reset.

FRAMEBUFFERCONTROLREGISTER(XR6F)
Read/Write at I/O Address 3D7h
Index 6Fh



This register is effective in flat panel mode only.

0 Frame Buffer Enable

This bit is used to enable frame buffer operation (external or embedded). Frame buffering is required for DD panel operation. For SS panel operation (LCD, Plasma or EL), frame buffering is not required so this bit should be set to 0.

0 Disable frame buffer (default)
1 Enable frame buffer

Since the 65540 and 65545 have the ability to embed frame buffer data in display memory, enabling frame buffering does not mean that an external DRAM frame buffer chip is required (see bit-7 of this register to set the frame buffer method).

1 Frame Accelerator Enable

Frame acceleration may be used for panels with vertical refresh rate specifications above 110 Hz to reduce the dot clock rate. For panels with vertical refresh rate specifications below 110 Hz, Frame Acceleration will violate panel specifications and should not be used.

This bit should be programmed to 0 when the Frame Buffer is disabled (bit-0 of this register set to 0) or for non-DD panels. If this bit is set to 1, bit-0 of this register must be set to 1 and a DD panel must be used (XR51[1-0], Panel Type, must be set to 11).

0 Disable frame accelerator (default)
1 Enable frame accelerator

2 Asymmetric Address for DRAM C

0 64Kx16 DRAM (8-bit RAS and CAS address)
1 Symmetric or Asymmetric 256Kx16 DRAM (9-bit RAS and CAS address or 10 bit RAS and 8 bit CAS addresses)

This bit is effective only if bit 7=1. Either Symmetric or Asymmetric DRAMs may be used.

5-3 Frame Buffer Refresh Count

These bits are effective only if bit 7=1.

6 Frame Buffer Lines/Page

0 1 line per DRAM page
1 2 lines per DRAM page

This bit is effective only if bit 7=1.

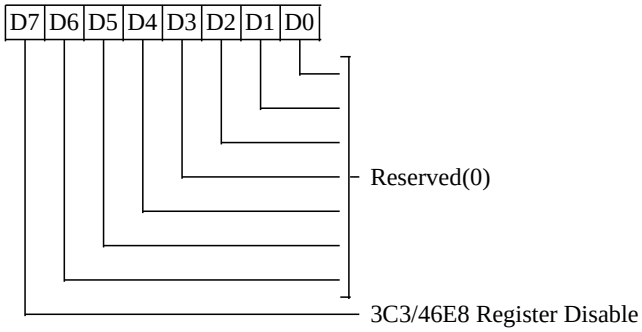
Note: 65540 only, should be programmed with 0 in the 65545.

7 Frame Buffer Method

0 Embedded Frame Buffer. Frame buffer data is stored in display memory (DRAM A or DRAMs A & B depending on the setting of XR04 bits 0-1)
1 External Frame Buffer. DRAM "C" is used exclusively for frame buffer data.

Note: This bit can be set to 1 only when XR04[1-0] (Memory Configuration) is set to either 00 (Display Memory in DRAMs A & B) or 01 (Display Memory in DRAM A).

SETUP/DISABLECONTROLREGISTER(XR70)
Read/Write at I/O Address 3D7h
Index 70h



6-0 Reserved (0)

7 3C3 / 46E8 Register Disable

0 In local bus configuration, port 3C3h works as defined to provide control of VGA disable. In ISA bus configuration, port 46E8h works as defined to provide control of VGA disable and setup mode.

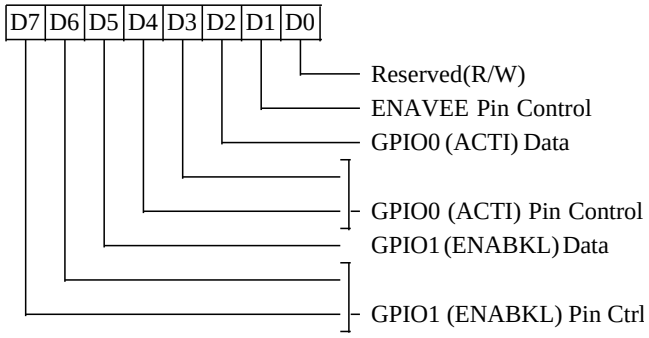
1 In local bus configuration, writes to I/O port 3C3 have no effect. In ISA bus configuration, writes to I/O port 46E8h have no effect (the VGA remains enabled and will not go into setup mode).

Note: Writes to register 46E8 are only effective in ISA bus configurations (46E8 is ignored in local bus configurations independent of the state of this bit). Writes to 3C3 are only effective in local bus configurations (3C3 is ignored in ISA bus configurations independent of the state of this bit). In PCI bus configuration (65545), this register has no effect; the chip comes up disabled except for the PCI configuration registers and the PCI configuration registers control VGA access.

Reads from ports 3C3 and 46E8h have no effect independent of the programming of this register (both 3C3 and 46E8h are write-only registers).

This register is cleared by reset.

EXTERNAL DEVICE I/O REGISTER (XR72)
Read/Write at I/O Address 3D7h
Index 72h



0 Reserved (R/W)

1 ENAVEE Pin Control

0 Pin 61 is used as Enable VEE (ENAVEE) output (default on reset)
1 Pin 61 is used as Enable Backlight (ENABKL) output

2 GPIO0 (ACTI) Data

This bit always reads back the state of the ACTI pin (pin 53). When ACTI is configured as general purpose output (XR72[4-3]=11) this bit determines the data output on ACTI pin.

4-3 GPIO0 (ACTI) Pin Control

This bit is effective only when XR01[4]=1, XR50[7]=0, and XR05[7-6]≠11.

00 Pin 53 is ACTI output (default on reset). ACTI goes high during valid VGA memory or I/O read or write operations that are recognized by the chip.
01 Reserved
10 Pin 53 is general purpose input 0 (GPIO0)
11 Pin 53 is general purpose output 0 (GPIO0)

5 GPIO1 (ENABKL) Data

This bit always reads back the status of the ENABKL pin (pin 54). When ENABKL is configured as general purpose output (XR72[7-6]=11), this bit determines the data output on the ENABKL pin.

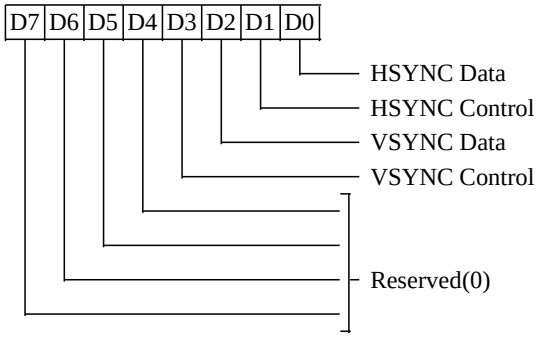
7-6 GPIO1 (ENABKL) Pin Control

This bit is effective only when XR01[4]=1, XR50[7]=0, and XR05[7-6]≠11.

00 Pin 54 is used to output ENABKL (enable backlight) (default on reset)
01 Reserved
10 Pin 54 is general purpose input 1 (GPIO1)
11 Pin 54 is general purpose output 1 (GPIO1)

See also XR5C "Activity Timer Control Register". The activity timer may be used to activate ENABKL or to evoke Panel Off mode after a specified time interval.

DPMS CONTROL REGISTER (XR73)
Read/Write at I/O Address 3D7h
Index 73h



This register is provided to allow the controller to independently shut down either or both of the HSYNC and VSYNC outputs. This capability allows the controller to signal a CRT monitor to enter power-saving states per the VESA DPMS (Display Power Management Signaling) Standard. The DPMS states are:

H	V	Power Management State
Active	Active	Normal Operation
Inactive	Active	Standby (Quick Recovery) Opt
Active	Inactive	Suspend (Max Power Savings)
Inactive	Inactive	Off (Autorecovery is optional)

0 HSYNC Data

If bit-1 of this register is programmed to 1, the state of this bit (XR73[0]) will be output on HSYNC (pin 65).

1 HSYNC Control

Determines whether bit-0 of this register or internal CRTC horizontal sync information is output on HSYNC (pin 65).

0 CRTC HSYNC is output (Default)
1 XR73[0] is output

2 VSYNC Data

If bit-3 of this register is programmed to 1, the state of this bit (XR73[2]) will be output on VSYNC (pin 64).

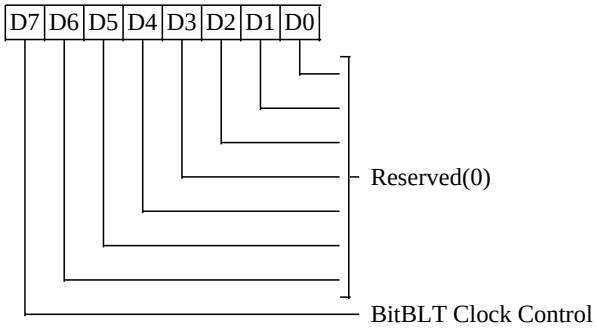
3 VSYNC Control

Determines whether bit-2 of this register or internal CRTC vertical sync information is output on VSYNC (pin 64).

0 CRTC VSYNC is output (Default)
1 XR73[2] is output

7-4 Reserved (0)

DIAGNOSTIC REGISTER (XR7D) (65545 Only)
Read/Only at I/O Address 3D7h
Index 72h

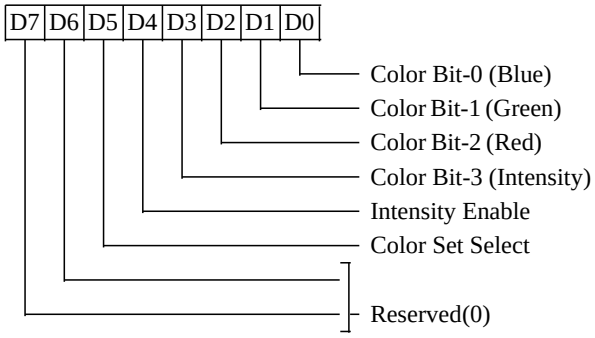


6-0 Reserved (0)

7 BitBLT Clock Control (65545 Only)

0 BitBLT logic receives a continuous running memory clock
1 The clock to the BitBLT logic is shut off

CGA/HERCCOLORSELECTREGISTER(XR7E)
Read/Write at I/O Address 3D7h
Index 7Eh

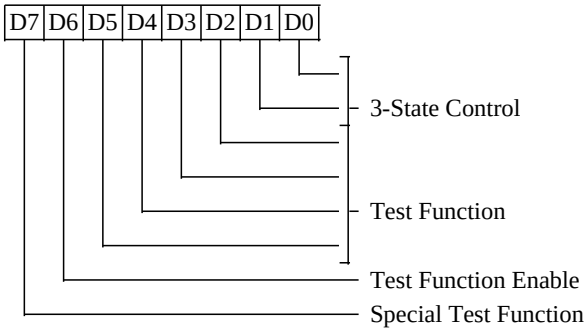


This I/O address is mapped to the same register as I/O address 3D9h. This alternate mapping effectively provides a color select register for Hercules mode. Writes to this register will change the copy at 3D9h. The copy at 3D9h is visible only in CGA emulation or when the extension registers are enabled. The copy at XR7E is visible when the extension registers are enabled.

5-0 See Register 3D9

7-6 Reserved (0)

DIAGNOSTIC REGISTER (XR7F)
Read/Write at I/O Address 3D7h
Index 7Fh



0 3-State Control Bit 0

0 Normal outputs (default on reset)
1 3-state system bus and display output pins: HSYNC, VSYNC, FLM, LP, M, SHFCLK, P0-15, LDEV#, and LRDY#.

1 3-State Control Bit 1

0 Normal outputs (default on reset)
1 3-state memory output pins: RASA#, RASB#, RASC#, CASAL#, CASAH#, CASBL#, CASBH#, CASCL#, CASCH#, WEA#, WEB#, WEC#, OEAB#, OEC#, AA0-9, and CA0-9.

5-2 Test Function

These bits are used for internal testing of the chip when bit-6 = 1.

6 Test Function Enable

This bit enables bits 5-2 for internal testing.

0 Disable test function bits (default)
1 Enable test function bits

7 Special Test Function

This bit is used for internal testing and should be set to 0 (default to 0 on reset) for normal operation.

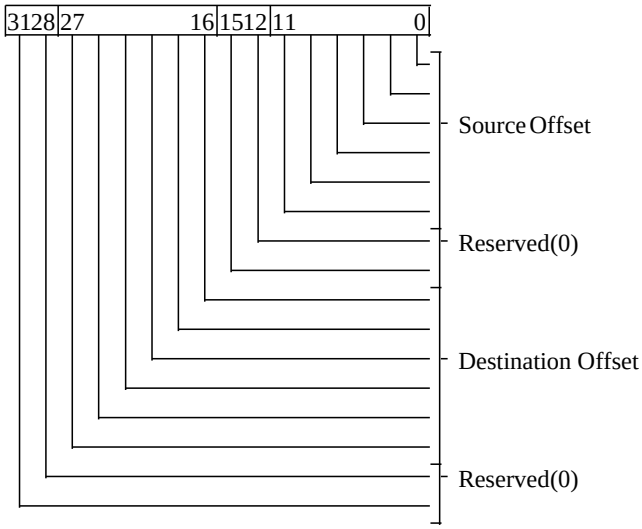
32-Bit Registers
(65545 Only)

Register Mnemonic	Register Group	Extension Register	Name	Access	Type	I/O Address	State After Reset				Page
DR00	BitBLT	BitBLT	Offset	16/32-bit	R/W	83D0-3	----xxxx	xxxxxxxx	----xxxx	xxxxxxxx	156
DR01	BitBLT	BitBLT	Pattern ROP	16/32-bit	R/W	87D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	156
DR02	BitBLT	BitBLT	BG Color	16/32-bit	R/W	8BD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	157
DR03	BitBLT	BitBLT	FG Color	16/32-bit	R/W	8FD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	157
DR04	BitBLT	BitBLT	Control	16/32-bit	R/W	93D0-3	--------	---0xxxx	xxxxxxxx	xxxxxxxx	158
DR05	BitBLT	BitBLT	Source	16/32-bit	R/W	97D0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	159
DR06	BitBLT	BitBLT	Destination	16/32-bit	R/W	9BD0-3	--------	---xxxxx	xxxxxxxx	xxxxxxxx	159
DR07	BitBLT	BitBLT	Command	16/32-bit	R/W	9FD0-3	----0000	00000000	----xxxx	xxxxxxxx	160
DR08	Cursor	Cursor	Control	16/32-bit	R/W	A3D0-3	--------	--------	••••0000	000•••00	161
DR09	Cursor	Cursor	Color 0-1	16/32-bit	R/W	A7D0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	162
DR0A	Cursor	Cursor	Color 2-3	16/32-bit	R/W	ABD0-3	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	162
DR0B	Cursor	Cursor	Position	16/32-bit	R/W	AFD0-3	x----xxx	xxxxxxxx	x----xxx	xxxxxxxx	163
DR0C	Cursor	Cursor	Base Address	16/32-bit	R/W	B3D0-3	--------	----xxxx	xxxxxx--	--------	164

Reset Codes:
x = Not changed by RESET (indeterminate on power-up)
d = Set from the corresponding pin on falling edge of RESET
h = Read-only Hercules Configuration Register Readback bits
r = Chip revision # (starting from 0000)
– = Not implemented (always reads 0)
• = Not implemented (read/write, reset to 0)
0/1 = Reset to 0 or 1 by falling edge of RESET

BitBLT OFFSET REGISTER (DR00)

Write at I/O Address 83D0–83D3h
Read at I/O Address 83D0–83D3h
Word or DoubleWord Accessible



11–0 Source Offset

This value is added to the start address of the Source BitBLT to calculate the starting position for the next line.

15–12 Reserved (0)

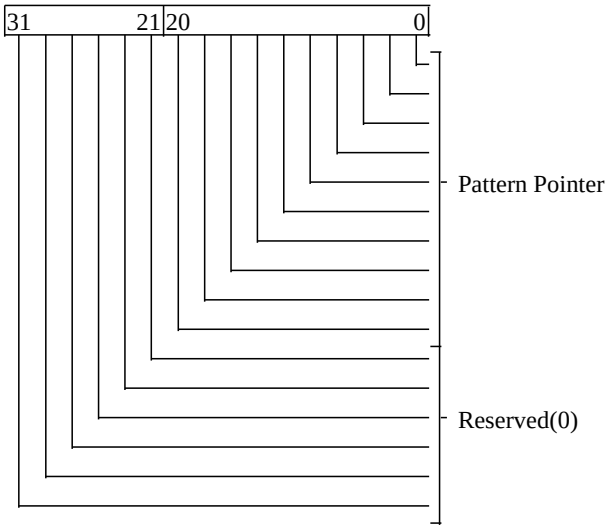
27–16 Destination Offset

This value is added to the start address of the Destination BitBLT to calculate the starting position for the next line.

31–28 Reserved (0)

BitBLT PATTERN ROP REGISTER (DR01)

Write at I/O Address 87D0–87D3h
Read at I/O Address 87D0–87D3h
Word or DoubleWord Accessible



20–0 Pattern Pointer

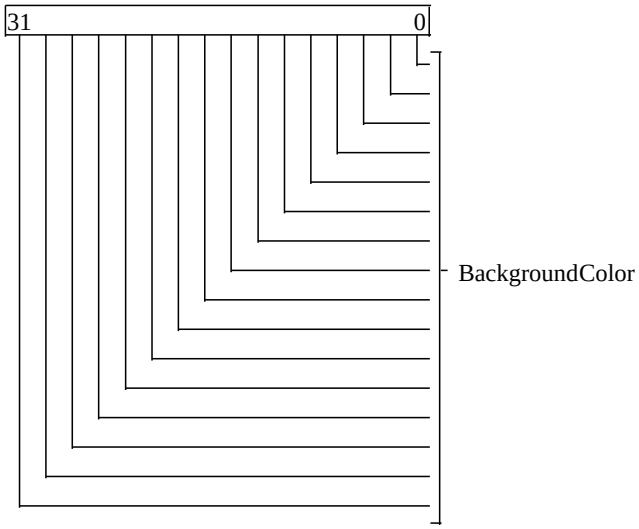
Address of Pattern Size - aligned 8 Pixel x 8 line pattern. For an 8BPP pattern (occupying 8 bits / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on a 64 byte (16 DWord) boundary. For a 16BPP pattern (occupying 16bits / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on a 128byte (32 DWord) boundary. For monochrome patterns (1 Bit / pixel * 8 pixels / line * 8 lines / pattern) the pattern must be aligned on an 8 byte (2 DWord) boundary. The lower bits of the Pattern Pointer are read/write, however the Drawing Engine forces them to zero for drawing operations.

31–21 Reserved (0)

Warning: Do not read this egister while a BitBLT is active.

BitBLT BACKGROUND COLOR REGISTER (DR02)

Write at I/O Address 8BD0–8BD3h
Read at I/O Address 8BD0–8BD3h
Word or DoubleWord Accessible



15–0 Background Color

This register contains the background color data used during opaque mono-color expansions.

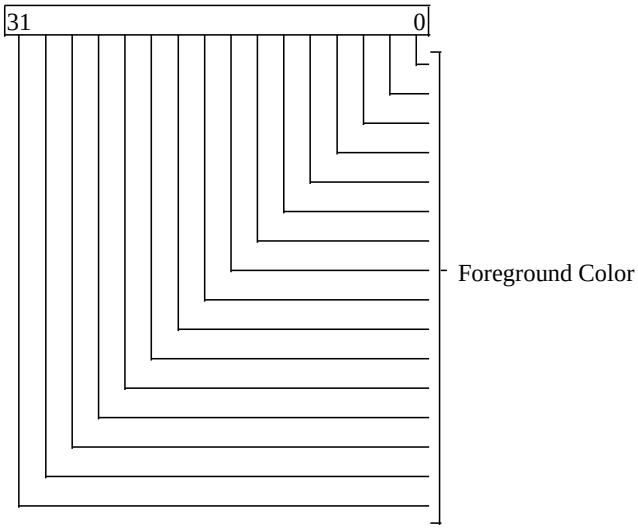
All 16 bits must be written regardless of pixel depth. If the drawing engine is operating at 8BPP, then the same data should be duplicated in bits 31:24, 23:16, 15:8, and 7:0. For 16BPP the data is duplicated twice.

31–16 Duplicate of 15-0

Warning: Only bits 15-0 are used. They are duplicated in bits 31-16 when this register is read back by the CPU.

BitBLT FOREGROUND COLOR REGISTER (DR03)

Write at I/O Address 8FD0–8FD3h
Read at I/O Address 8FD0–8FD3h
Word or DoubleWord Accessible



15–0 Foreground/Solid Color

This register contains the color data used during solid paint operations. It also is used as the foreground color during mono-color expansions.

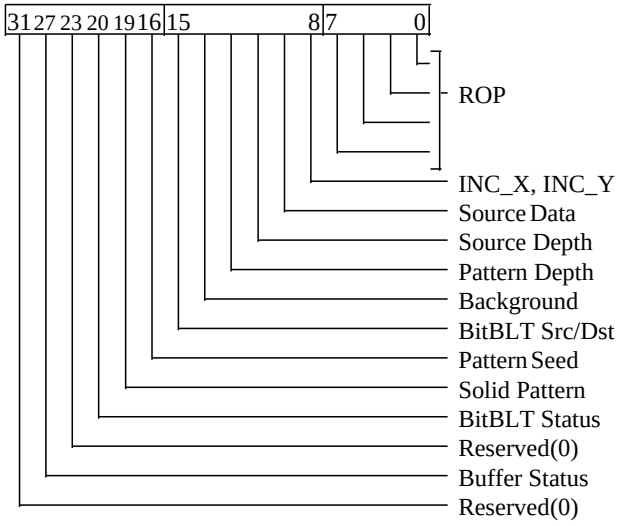
All 16 bits must be written regardless of pixel depth. If the drawing engine is operating at 8BPP, then the same data should be duplicated in bits 31:24, 23:16, 15:8, and 7:0. For 16BPP the data is duplicated twice.

31–16 Duplicate of 15-0

Warning: Only bits 15-0 are used. They are duplicated in bits 31-16 when this register is read back by the CPU.

BitBLT CONTROL REGISTER (DR04)

Write at I/O Address 93D0–93D3h
Read at I/O Address 93D0–93D3h
Word or DoubleWord Accessible



7–0 ROP

Raster Operation as defined by Microsoft Windows. All logical operations of Source, Pattern, and Destination Data are supported.

8 INC_Y

DeterminesBitBLTY-direction:

0 Decrement (Bottom to Top)
1 Increment (Top to Bottom)

9 INC_X

DeterminesBitBLTX-direction:

0 Decrement (Right to Left)
1 Increment (Left to Right)

10 Source Data

Selects variable data or color register data:

1 Source is FG Color Reg (DR03)
0 Source data selected by DR04[14]

11 Source Depth

Selects between monochrome and color source data. This allows BitBLTs to either transfer source data directly to the screen or perform a font expansion (INC_X=1 only):

0 Source is Color
1 Source is Mono (Font expansion)

12 Pattern Depth

Selects between monochrome and color pattern data. This allows the pattern register to operate either as a full pixel depth 8x8 pattern for use by the ROP, or as an 8x8 monochromepattern:

0 Pattern is Color
1 Pattern is Monochrome

13 Background

The 65540 / 545 supports both transparent and opaque backgrounds for monochrome patterns and font expansion:

0 BG is Opaque (BG Color Reg DR02)
1 BG is Transparent (Unchanged)

15–14 BitBLT Source/Destination

The 65540 / 545 only supports its local display memory as the destination for BitBLT operations. The source may be either display memory or system memory (CPU):

15	14	BitBLT Source —> Dest
0	0	Screen —> Screen (Dest)
0	1	System —> Screen (Dest)
1	0	Reserved
1	1	Reserved

18–16 Pattern Seed

Determines the starting row of the 8x8 pattern for the current BitBLT. A pattern is typically required to be destination aligned. The 65540 / 545 can determine the x-alignment from the destination address however the y-alignment must be generated by the programmer. These three bits determine which row of the pattern is output on the first line of the BitBLT. Incrementing and decrementing are controlled by bit DR04[8].

19 Solid Pattern

1 = Solid Pattern (Brush)
0 = BitmapPattern

20 BitBLT Status (Read Only)

0 BitBLT Engine Idle
1 BitBLT Active - do not write BitBLT regs

23–21 Reserved (0)

27–24 Buffer Status

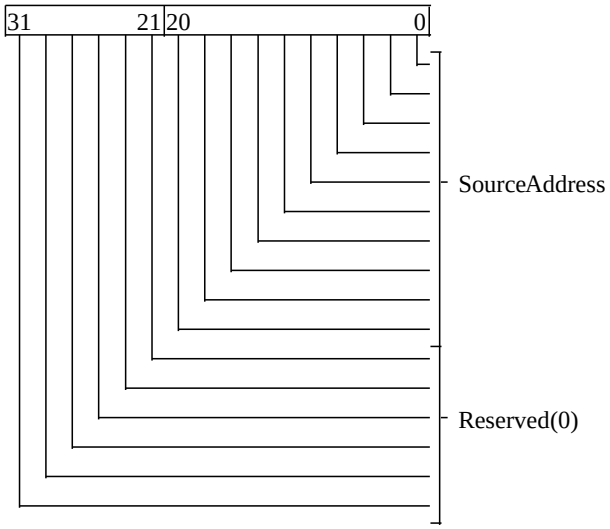
# of DWords that can be written to the chip:

0000 Buffer Full
0001 1 Space available in the queue
... ...
1111 15 Spaces available in the queue

31–25 Reserved (0)

BitBLT SOURCE REGISTER (DR05)

Write at I/O Address 97D0–97D3h
Read at I/O Address 97D0–97D3h
Word or DoubleWord Accessible



20–0 Source Address

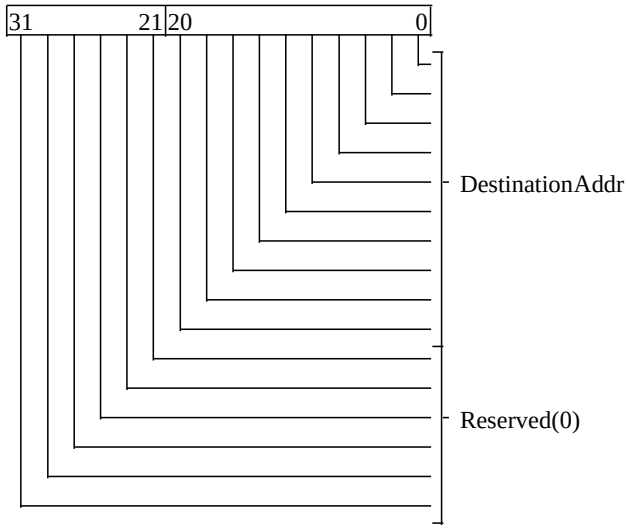
Address of Byte aligned source block.

31–21 Reserved (0)

Warning: ***Do not read this register while a BitBLT is active.***

BitBLT DESTINATION REGISTER (DR06)

Write at I/O Address 9BD0–9BD3h
Read at I/O Address 9BD0–9BD3h
Word or DoubleWord Accessible



20–0 DestinationAddress

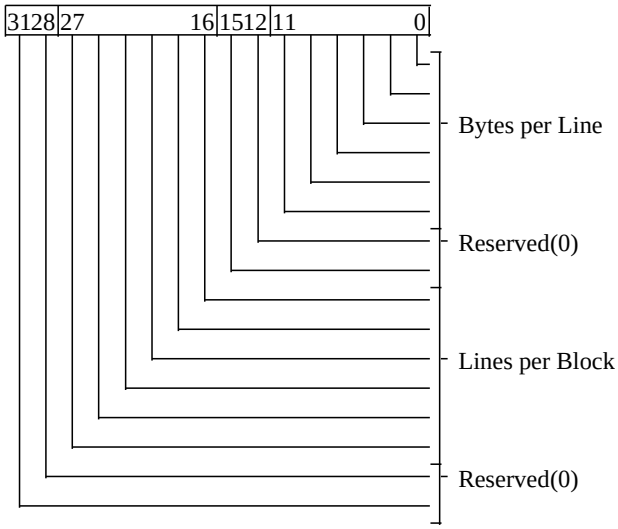
Address of Byte aligned destination block.

31–21 Reserved (0)

Warning: ***Do not read this register while a BitBLT is active.***

BitBLT COMMAND REGISTER (DR07)

Write at I/O Address 9FD0–9FD3h
Read at I/O Address 9FD0–9FD3h
Word or DoubleWord Accessible



11–0 Bytes Per Line

Number of bytes to be transferred per line

15–12 Reserved (0)

27–16 Lines Per Block

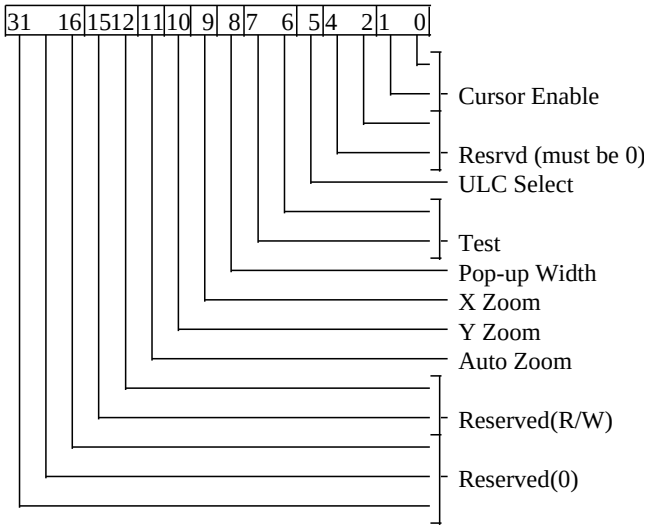
Height in lines of the block to be transferred

31–28 Reserved (0)

Warning:	***Do not attempt to perform a CPU read/write to display memory while a BitBLT is active.***

CURSOR/POP-UP CONTROL REGISTER (DR08)

Write at I/O Address A3D0–A3D3h
Read at I/O Address A3D0–A3D3h
Word or DoubleWord Accessible



1-0 Cursor / Pop-Up Menu Enable

This bit enables the hardware cursor. The cursor will be enabled/disabled in the frame following the current active frame (synchronized to vertical blank).

00 Both Disabled
01 32x32 Cursor Enable
10 64x64 Cursor Enable
11 Pop-Up Menu Enable

4–2 Reserved (R/W)

Must be programmed to 0.

5 Upper Left Corner (ULC) Select

The cursor is set relative to either the Upper Left Corner (ULC) of the active display or of the overscan region. When set relative to the active display (BLANK#) the cursor will not be visible in the overscan area. When relative to Display Enable, the cursor may appear in the overscan region. All x,y positioning is relative to the selected ULC.

0 ULC is BLANK# (x=0, y=0 corresponds to the top left of the panel)
1 ULC is Display Enable (x=0, y=0 corresponds to the top left of the image)

7-6 Test

8 Pop-Up Menu Width

0 One bpp. Menu width = 128 pixels. This also forces a height of 128 lines. CC0 and CC1 (DR09) determine menu colors.
1 Two bpp. Menu width = 64 pixels. CC0-3 (DR09 and DR0A) determine menu colors.

9 X Zoom (Manual)

0 No pixel replication.
1 Replicate pixels in the horizontal direction. No pixel replication takes place in CRT interlace mode and for 32x32 cursor.

10 Y Zoom (Manual)

0 No pixel replication.
1 Replicate pixels in the vertical direction. No pixel replication takes place in CRT mode and for 32x32 cursor.

11 Auto Zoom

0 Auto zoom off
1 Replicate pixels in high resolution modes. No pixel replication takes place in CRT interlace mode and for 32x32 cursor.

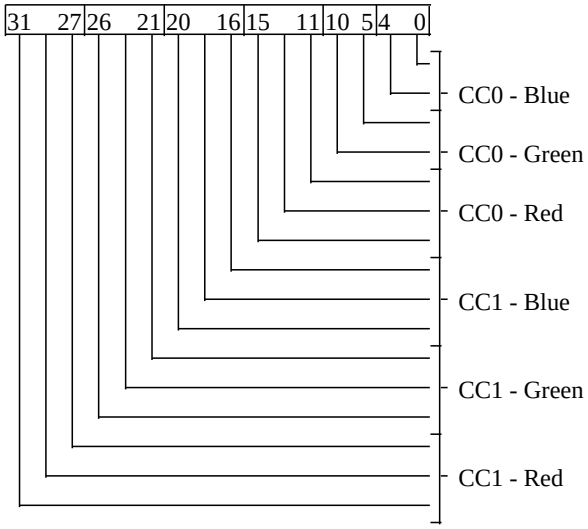
15–12 Reserved (R/W)

31–16 Reserved (0)

Refer to the Functional Description section of this document for additional information on programming of the Hardware Cursor feature.

CURSOR/POP-UPCOLOR0-1REGISTER(DR09)

Write at I/O Address A7D0–A7D3h
Read at I/O Address A7D0–A7D3h
Word or DoubleWord Accessible



Cursor Colors 0 and 1 are 16-bit high color values consisting of 5 bits of Red, 6 bits of Green, and 5 bits of Blue. Colors 0 and 1 may be accessed either as two 16-bit registers or as a single 32-bit register. A write to this register immediately affects the cursor color displayed.

4–0 CC0 - Blue

Cursor Color 0 Blue value

10–5 CC0 - Green

Cursor Color 0 Green value

15–11 CC0 - Red

Cursor Color 0 Red value

20–16 CC1 - Blue

Cursor Color 1 Blue value

26–21 CC1 - Green

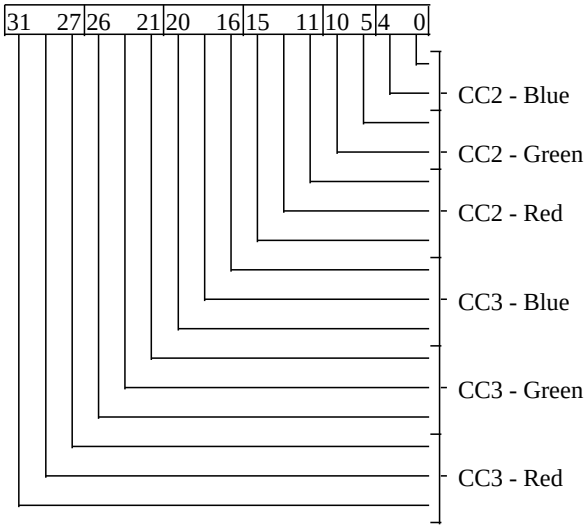
Cursor Color 1 Green value

31–27 CC1 - Red

Cursor Color 1 Red value

CURSOR/POP-UPCOLOR2-3REGISTER(DR0A)

Write at I/O Address ABD0–ABD3h
Read at I/O Address ABD0–ABD3h
Word or DoubleWord Accessible



Cursor Colors 2 and 3 are 16-bit high color values consisting of 5 bits of Red, 6 bits of Green, and 5 bits of Blue. Colors 2 and 3 may be accessed either as two 16-bit registers or as a single 32-bit register. Colors 2 and 3 are only used when the Cursor is in Pop-Up Mode. A write to this register immediately affects the cursor color displayed.

4–0 CC2 - Blue

Cursor Color 2 Blue value

10–5 CC2 - Green

Cursor Color 2 Green value

15–11 CC2 - Red

Cursor Color 2 Red value

20–16 CC3 - Blue

Cursor Color 3 Blue value

26–21 CC3 - Green

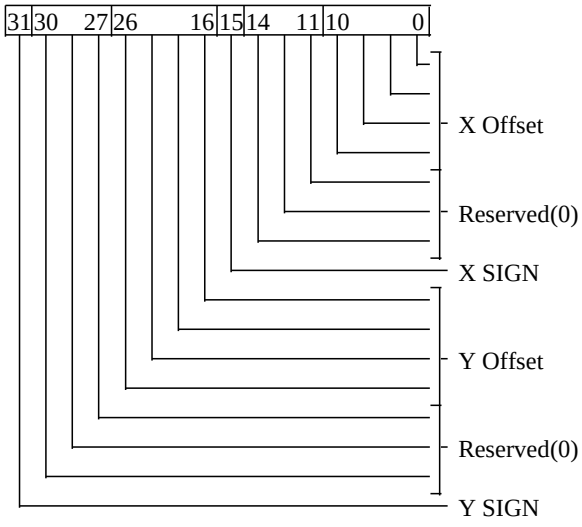
Cursor Color 3 Green value

31–27 CC3 - Red

Cursor Color 3 Red value

CURSOR/POP-UP POSITION REGISTER (DR0B)

Write at I/O Address AFD0–AFD3h
Read at I/O Address AFD0–AFD3h
Word or DoubleWord Accessible



10–0 X Offset

Cursor X-position. The cursor position is calculated as the signed offset (in pixels) between the Upper Left Corner (ULC) of the screen (as defined by BLANK#) and the Upper Left Corner of the cursor. X Offset is the magnitude portion of the signed offset of the cursor position in the horizontal axis. This magnitude in combination with the X SIGN bit (15) form the signed offset of the cursor in the X direction.

The X OFFSET and X SIGN may be written as a 16-bit quantity with bits 14-11 ignored.

The range for the ULC of the cursor is:

–2047 <= X-Position <= 2047

14–11 Reserved (0)

15 X Sign

Sign associated with the X OFFSET magnitude which together form the signed offset of the cursor in the X direction.

26–16 Y Offset

Cursor Y-position. The cursor position is calculated as the signed offset (in pixels) between the Upper Left Corner (ULC) of the screen (as defined by BLANK#) and the Upper Left Corner of the cursor. Y Offset is the magnitude portion of the signed offset of the cursor position in the vertical axis. This magnitude in combination with the Y SIGN bit (31) form the signed offset of the cursor in the Y direction.

The Y OFFSET and Y SIGN may be written as a 16-bit quantity with bits 30-27 ignored.

The range for the ULC of the cursor is:

–2047 <= Y-Position <= 2047

30–27 Reserved (0)

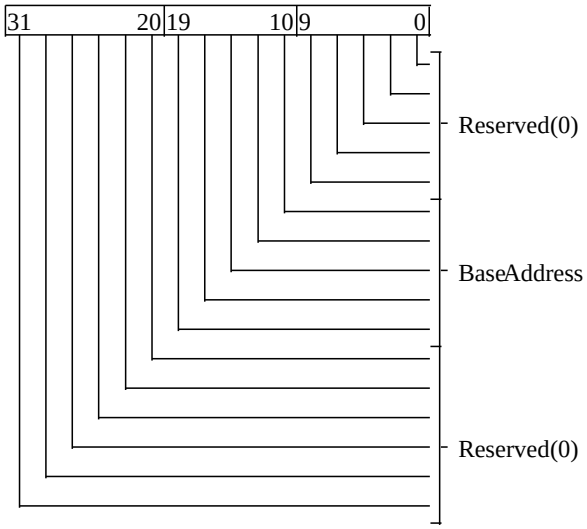
31 Y Sign

Sign associated with the Y OFFSET magnitude which together form the signed offset of the cursor in the Y direction.

In pop-up menu mode negative values are not supported.

CURSOR/POP-UP BASE ADDRESS (DR0C)

Write at I/O Address B3D0–B3D3h
Read at I/O Address B3D0–B3D3h
Word or DoubleWord Accessible



9–0 Reserved (0)

19–10 Base Address

Base address for cursor / pop-up data in display memory. Bit 10 (address lsb) should be programmed to 0 when the 128x128 pop-up menu is being displayed. Defines a byte address in display memory as seen by the CPU.

31–20 Reserved (0)

Refer to the Functional Description section of this document for additional information on programming of the Hardware Cursor feature.

System Interface

Functional Blocks

The 65540 / 545 contains 5 major functional blocks including the standard VGA core (Sequencer, Attribute controller, Graphics Controller, and CRT Controller), a BitBLT engine (65545 only), Hardware Cursor (65545 only), Palette DAC, and Clock Synthesizer. There are also other subsystems such as the bus and memory interfaces which are transparent to both the user and software programmer. While in standard VGA modes only the VGA core, Palette DAC, and clock synthesizer are active.

Bus Interface

Two major buses are directly supported by the 65540 and 65545: Industry Standard Architecture (ISA), and VESA Local Bus (VL-Bus); the 65545 also supports the PCI Bus. Direct interfaces to popular 80486DX, 80486DX2, 80486SX, and 80386DX processors are supported by both chips. Connection to 16-bit PI bus and other 32-bit system buses such as EISA and Micro Channel (MC) are possible with external logic but are not inherently supported.

ISA Interface

The 65540 / 545 operates as a 16-bit slave device on the ISA bus. It maps its display memory into the standard VGA address range (0A0000-0BFFFFh). The VGA BIOS ROM is decoded in the 32KByte space at 0C0000-0C7FFFh (an output is available on the ROMCS# pin for ROM chip selection). Address lines LA23:17 are required for decoding MEMCS16# hence these addresses are latched internally by ALE. The remaining addresses (SA16:0) are accepted from the system without internal latching. The 65540 / 545 supports 16-bit memory and I/O cycles. Whenever possible the 65540 / 545 executes zero wait state memory cycles by asserting ZWS#. It does not generate MEMCS16# or ZWS# on ROM accesses. Memory may be mapped as a single linear frame buffer anywhere in the 16 MByte ISA memory space on a 512K/1MByte boundary (depending on the amount of display memory installed - see XR0B[4]). The 16-bit bus extension signals MEMR# and MEMW# are used for memory control since mapping above the 1MByte boundary is permitted. For ISA compatibility the IRQ pin operates as an active high level-triggered interrupt.

VL-Bus Interface

The 65540 / 545 operates as a 32-bit target on the VL-Bus. It has an optimized direct pin-to-pin connection for all VL-Bus signals to eliminate external components. Up to 28 bits of the 32-bit VL-Bus address may be decoded on-chip permitting location of the linear frame buffer anywhere in a 256MByte address space. Optionally, the upper 4 address bits may be decoded externally to support the full 32-bit, 4GB VL-Bus address space. Zero wait state read accesses are not permitted, however, the 65540 / 545 will terminate a read cycle in the second T2 if the data is available. Burst cycles are not supported.

Direct Processor Interface

The 65540 / 545 can interface directly to all 32-bit x86-architecture processors. Its full non-multiplexed 28-bit address makes it simple to connect to the CPU. On valid 65540 / 545 accesses it will generate LDEV# which is monitored by the system logic controller. This interface is essentially the same as the VL-Bus interface with the exception that both 1x and 2x CPU clocks are acceptable. When using a 2x clock the CPU Reset must be connected to the 65540 / 545 CRESET input for phase coherency. The 65540 / 545 does not support pipelined mode in its 386 processor interface.

PCI Interface

The 65545 also supports a full 32-bit PCI bus interface as defined by PCI Interface Specification Revision 2.0. All features required of a non-bus-master 'target' device are implemented on-chip with no external glue logic required. Read/Write cycles are supported for Memory, I/O, and Configuration address spaces. Burst accesses are not supported. Interrupt capability is provided for vertical interrupts.

Refer to the PCI Pin Descriptions and Configuration Registers sections for further information.

Display Memory Interface

Memory Architecture

The 65540 / 545 supports both 512K and 1MB configurations for display memory plus an additional 512K for an optional external frame buffer. Frame buffering is required for support of simultaneous display on CRTs and DD panels, however, the 65540 / 545 has the ability to embed frame buffer data in display memory. Since this uses some of the available memory bandwidth, the 65540 / 545 also supports an additional DRAM for use as an external frame buffer for improved performance.

The 65540 / 545 implements a 32-bit wide data bus for display memory and 16-bit for the optional external frame buffer. The memory data buses are named 'A', 'B', and 'C' in groups of 16 bits. 'A' holds the lower 512K of display memory, 'B' normally holds the upper 512K of display memory in 1MB configurations and 'C' is normally used for the external frame buffer (if used). The chip may, however, be optionally programmed to put the upper half of display memory in DRAM 'C' instead (i.e., 'C' may be programmed to hold either display memory or external frame buffer data). When an external frame buffer is not required, 'C' may also be used as an input port for external video data (to implement overlay of live video over VGA output for example) and to provide additional panel interface data bits beyond the basic 16 (for TFT panels with 18-bit or 24-bit data interfaces since TFT panels are single panels and never require frame buffering).

There are separate groups of RAS, CAS, and WE pins for each of the three DRAMs (A, B, and C). There are only two OE pins and two address buses however, one for A and B and another for C. Configuration initialization data is latched from memory address pins AA0-8 (the address bus for DRAMs A and B) at the end of reset. These bits are readable in XR01[0-7] and XR6C[1] respectively.

The 65540 and 65545 support all VGA text and graphics modes (planar, packed pixel, odd/even chain modes, etc.) but the storage locations of the data (i.e., the locations and bit positions in the DRAMs) does not correspond to the original VGA which implemented 256KB of display memory as 4 physical 'planes' of 64KB (using two 64Kx4 DRAMs to implement each 'plane' with separate address buses for planes 0-1 and 2-3). In other words, no assumptions should be made regarding the correspondence of the data pins on the display memory data bus of the 65540 / 545 to traditional VGA 'plane' concepts. For example, text data is still stored in 'plane' 0, attribute data in 'plane' 1, and font data in 'plane' 2, but due to the extensive use of page-mode cycles and the use of a single address bus for display memory data, where those planes are physically located in the DRAMs is much different.

In addition, the 65540 / 545 make extensive use of internal FIFOs to improve performance. As a result the read / write activity on the DRAM interface pins at any point in time corresponds only approximately to system bus and CRT / panel output activity at that time.

Memory Chip Requirements

The 65540 / 545 is designed to use 256K x 4 or 256K x 16 DRAMs. Fast-page-mode capability is required. Either 'CAS-Before-RAS' or 'Self-Refresh' DRAMs may be used. Both dual-CAS# (default) and dual-WE# types of 256Kx16 DRAMs are supported. DRAMs with 'symmetrical' address inputs (A0-8) are supported by default, but the chip can be configured to support 'asymmetrical' address (A0-9) DRAMs. The BIOS can test the DRAMs to detect the type of DRAM used and program the chip accordingly.

The 65540 / 545 can generate Page Mode Read, Page Mode Write, and Page Mode Read-Modify-Write cycles. CAS-before-RAS Refresh and Self-Refresh cycles are also supported. The memory interface is optimized for 40ns page mode cycles but is flexible and can be tuned for any speed DRAM.

The 65540 / 545 supports various DRAM speeds. The maximum frequency of the 65540 / 545 is 75 MHz. The recommended maximum memory clock frequency for various DRAM based on commonly available DRAM specifications is as follows:

DRAM Speed	Memory Clock Frequency*
100 ns	50.000 MHz
80 ns	57.000 MHz
70 ns	65.000 MHz

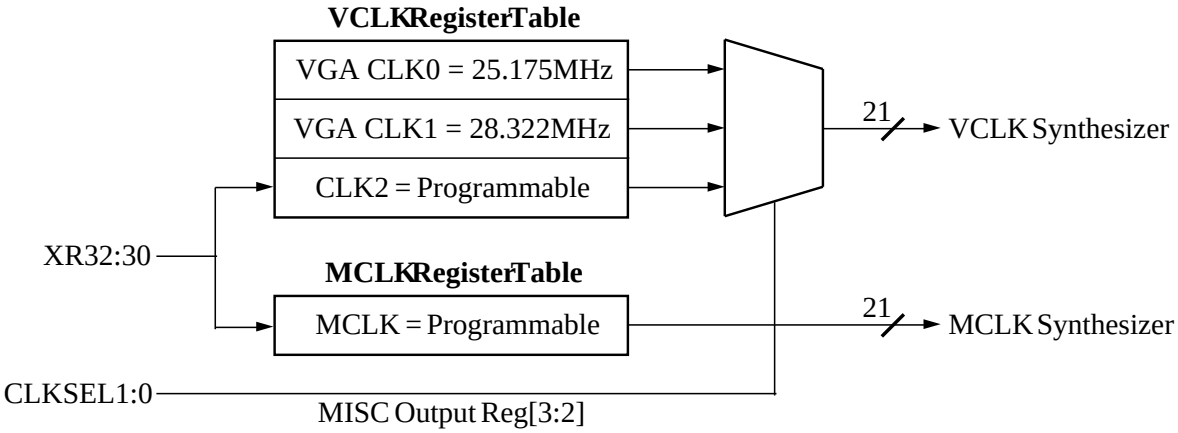
***** DRAM AC timing parameters varies among different DRAM manufacturers therefore please check with DRAM specifications and 65540 / 545 memory timing.

Clock Synthesizer

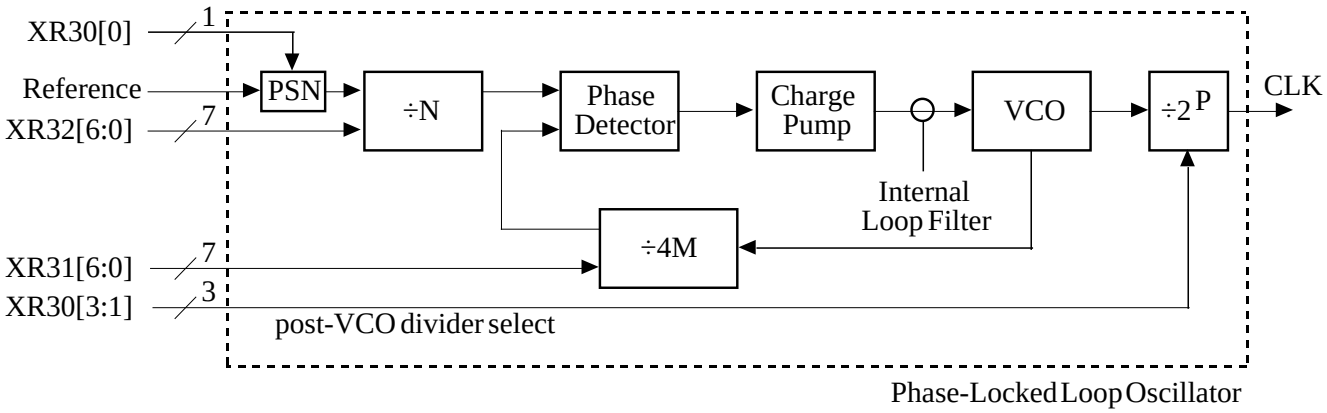
An integrated clock synthesizer supports all pixel clock (VCLK) and memory clock (MCLK) frequencies which may be required by the 65540 / 545. Each of the two clock synthesizer phase lock loops may be programmed to output frequencies ranging between 1MHz and the maximum specified operating frequency for that clock in increments not exceeding 0.5%. The frequencies are generated by an 18-bit divisor word. This value contains divisor fields for the Phase Lock Loop (PLL), Voltage Controlled Oscillator (VCO) and Pre/Post Divide Control blocks. The divisor word for both synthesizers is programmable via Clock Control Registers XR30-32.

MCLK Operation

Normal operational frequencies for MCLK are between 50MHz and 68MHz. Refer to the Electrical Specifications for maximum frequencies at 3.3V and 5V (the maximum frequency at 3.3V will be slightly lower). Normal MCLK operational frequencies are defined by the display memory sequencer parameters described in the Memory Timing section. The frequency selected is also dependent upon the AC characteristics of the display memories connected to the 65540 / 545. A typical match is between industry standard 70ns access memories and a 65MHz MCLK. The MCLK output defaults to 60MHz on reset and is fully programmable. This initial value is conservative enough not to violate slow DRAM parameters but not so slow as to cause a system timeout on CPU accesses. The MCLK frequency must always equal or exceed the host clock (CCLK) frequency.



Clock Synthesizer Register Structure



Clock Synthesizer PLL Block Diagram

VCLK Operation

The VCLK output typically ranges between 19MHz and 65MHz. VCLK has a table of three frequencies from which to select a frequency. This is required for VGA compatibility. CLK0 and CLK1 are fixed at the VGA compatible frequencies of 25.175MHz and 28.322MHz respectively. These values can not be changed unlike CLK2 which is fully programmable. The active frequency is chosen by clock select bits MSR[3:2].

Programming the Clock Synthesizer

The desired output frequency is defined by an 18-bit value programmed in XR30-32. The 65540 / 545 has two programmable clock synthesizers; one for memory (MCLK) and one for video (VCLK). They are both programmed by writing the divisor values to XR30-32. The clock to be programmed is selected by the Clock Register Program Pointer XR33[5]. The output frequency of each of the clock synthesizers is based on the reference frequency (F_{REF}) and the 4 programmed fields:

Field	# Bits	
Prescale N (PSN)	**XR30[0]**	**(÷1 or ÷4)**
Mcounter(M')	**XR31[6:0]**	**(M' = M - 2)**
N counter (N')	**XR32[6:0]**	**(N' = N - 2)**
Post Divisor (P)	**XR30[3:1]**	**($\div 2^P$; $0 \le P \le 5$)**

$$F_{OUT} = \frac{F_{REF} * 4 * M}{PSN * N * 2^P}$$

The frequency of the Voltage Controlled Oscillator (F_{VCO}) is determined by these fields as follows:

$$F_{VCO} = \frac{F_{REF} * 4 * M}{PSN * N}$$

where F_{REF} = Reference frequency (between 4 MHz - 20 MHz; typically 14.31818 MHz)

Note: If a reference frequency other than 14.31818 MHz is used, then the frequencies loaded on RESET will not be correct.

P	Post Divisor
000	1
001	2
010	4
011	8
100	16
101	32

Programming Constraints

There are five primary programming constraints the programmer must be aware of:

$$4 \text{ MHz} \le F_{REF} \le 20 \text{ MHz}$$

$$150 \text{ KHz} \le F_{REF}/(PSN * N) \le 2 \text{ MHz}$$

$$48 \text{ MHz} < F_{VCO} \le 220 \text{ MHz}$$

$$3 \le M \le 127$$

$$3 \le N \le 127$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation.

The value of F_{VCO} must remain between 48 MHz and 220 MHz inclusive. Therefore, for output frequencies below 48 MHz, F_{VCO} must be brought into range by using the post-VCO Divisor.

To avoid crosstalk between the VCO's, the VCO frequencies should not be within 0.5% of each other nor should their harmonics be within 0.5% of the other's fundamental frequency.

The 65540 / 545 clock synthesizers will seek the new frequency as soon as it is loaded following a write to XR32. Any change in the post-divisor will take affect immediately. There is a possibility that the output may glitch during this transition of post divide values. Because of this, the programmer may wish to hold the post-divisor value constant across a range of frequencies (eg. changing MCLK from the reset value of 50MHz to 72MHz). There is also the consideration of changing from a low frequency VCO value with a post-divide ÷1 (eg. 50MHz) to a high frequency ÷4 (eg. 220MHz). Although the beginning and ending frequencies are close together, the intermediate frequencies may cause the 65540 / 545 to fail in some environments. In this example there will be a short-lived time frame during which the output frequency will be in the neighborhood of 12.5MHz. The bus interface may not function correctly if the MCLK frequency falls below a certain value. Register and memory accesses which are synchronized to MCLK may be so slow as to violate bus timing and cause a watchdog timer error. Programmers should time-out the system (CPU) for approximately 10ms after writing XR32 before accessing the VGA again. This will ensure that accesses do not occur to the VGA while the clocks are in an indeterminate state.

Note: On reset the MCLK is initialized to a 60MHz output with a post divisor = 2 (F_{VCO} = 120MHz).

Programming Example

The following is an example of the calculations which are performed:

Derive the proper programming word for a 25.175 MHz output frequency using a 14.31818 MHz reference frequency:

Since 25.175 MHz < 48 MHz, double it to 50.350 MHz to get FVCO in its valid range. Set the post divide field (P) to 001.

Prescaling PSN = 4

The result:

FVCO = 50.350 = (14.31818 x 4 x M/4 x N)

M/N = 3.51655

Several choices for M and N are available:

M	N	Fvco	Error
109	31	50.344	-0.00300
102	29	50.360	+0.00500

Choose (M, N) = (109,31) for best accuracy.

Prescaling PSN = 1

The result:

FVCO = 50.350 = (14.31818 x 4 x M/1 x N)

M/N = 0.879127

M	N	Fvco	Error
80	91	50.349	-0.00050

FREF/(PSN x N) = 157.3KHz

Therefore M/N = 80/91 with PSN = 1 is even better than with PSN = 4.

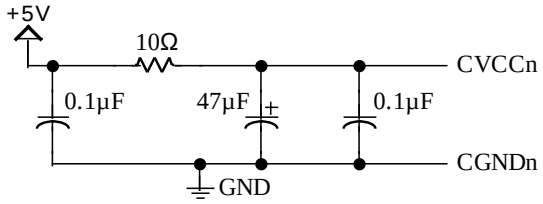
XR30 = 0000010b (02h)
XR31 = 80 - 2 = 78 (4Eh)
XR32 = 91 - 2 = 89 (59h)

Designator	Value
C1,C3,C4,C6,C7	0.1µF
C2,C5	47µF
R1,R2	10Ω

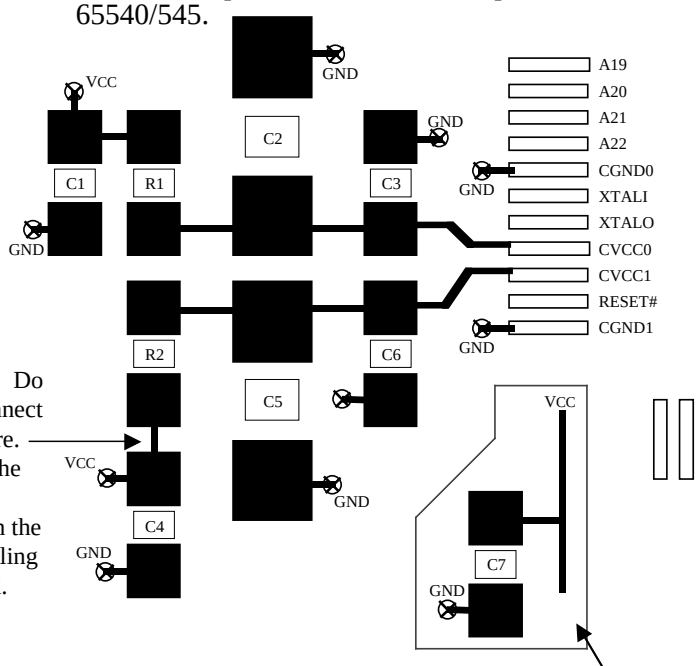
PCB Layout Considerations

Clock synthesizers, like most analog components, must be isolated from the digital noise which exists on a PCB power plane. Care must be taken not to route any high frequency digital signals in close proximity to the analog sections. Inside the 65540/545, the clocks are physically located in the lower left corner of the chip surrounded by low frequency input and output pins. This helps minimize both internally and externally coupled noise.

The memory clock and video clock power pins on the 65540/545 each require similar RC filtering to isolate the synthesizers from the VCC plane and from each other. The filter circuit for each CVCCn / CGNDn pair is shown below:



The suggested method for layout assumes a multi-layer board including VCC and GND planes. All ground connections should be made as close to the pin / component as possible. The CVCC trace should route from the 65540/545 **through the pads** of the filter components. The trace should NOT be connected to the filter components by a stub. All components (particularly the initial 0.1µF capacitor) should be placed as close as possible to the 65540/545.



NOTE: Do not connect Vcc here. Force the trace through the decoupling cap pad.

Always pass the Vcc trace through the decoupling cap pad. Do not leave a stub as shown here.

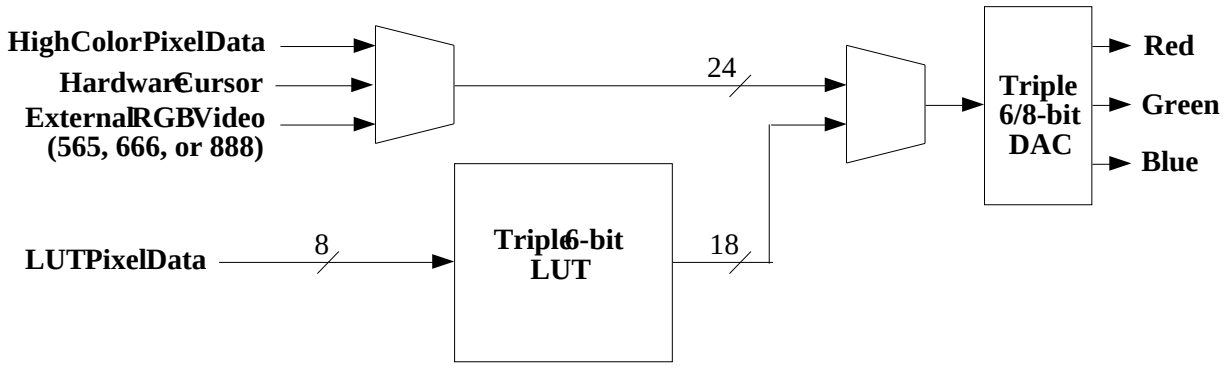
VGA Color Palette DAC

The 65540 / 545 integrates a VGA compatible triple 6-bit lookup table (LUT) and high speed 6/8-bit DACs. Additionally the internal color palette DAC supports true-color bypass modes displaying color depths up to 24bpp (8-8-8). The palette DAC can switch between true-color data and LUT data on a pixel by pixel basis. Thus, video overlays may be any arbitrary shape and can lie on any pixel boundary. The hardware cursor is also a true-color bitmap which may overlay both video and graphics on any pixel boundary.

The internal palette DAC register I/O addresses and functionality are 100% compatible with the VGA standard. In all bus interfaces the palette DAC automatically controls accesses to its registers to avoid data overrun. This is accomplished by holding RDY in the ISA configuration and by delaying LRDY# for VL-Bus and direct processor interfaces.

For compatibility with the VL-Bus Specification the 65540 / 545 may be disabled from responding to palette writes (although it will perform them) so that an adapter card on a slow (ISA) bus which is shadowing the palette LUT may see the access. The 65540 / 545 always responds to palette read accesses so it is still possible for the shadowing adapter to become out of phase with the internal modulo-3 RGB pointer. It is presumed that this will not be a problem with well-behaved software.

Extended display modes may be selected in the Palette Control Register (XR06). Two 16bpp formats are supported: 5-5-5 Targa format and 5-6-5 XGA format.



VGA Color Palette DAC Data Flow

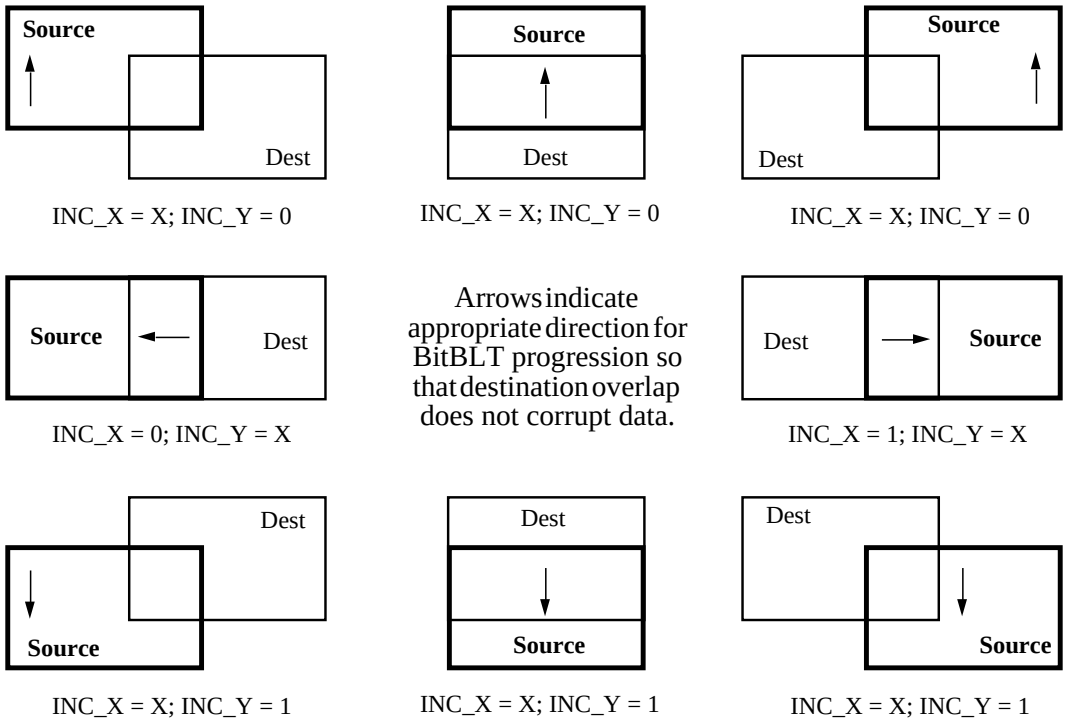
BitBLT Engine (65545 only)

Bit Block Transfer

The 65545 integrates a Bit Block Transfer (BitBLT) Engine which is optimized for operation in a Microsoft Windows environment. The BitBLT engine supports system-to-screen and screen-to-screen memory data transfers. It handles monochrome to color data expansion using either system or screen data sources. Color depths of 8 and 16bpp are supported in the expansion logic. Integrated with the screen and system BitBLT data streams is a 3-operand raster-op (ROP) block. This ROP block includes an independent 8x8 pixel (mono or color) pattern. Color depths of 8 and 16bpp are supported by the pattern array. All possible logical combinations of Source (system or screen data), Destination (screen data), and Pattern data are available.

The BitBLT and ROP subsystems have been architected for compatibility with the standard Microsoft Windows BitBLT parameter block. The source and destination screen widths are independently programmable. This permits expansion of a compressed off-screen bitmap transparent to the software driver. The BitBLT Control Register (DR04) uses the same raster-op format as the Microsoft Windows ROP so no translation is required. All 256 Windows defined ROPs are available.

All possible overlaps of source and destination data are handled by controlling the direction of the BitBLT in the x and y directions. As shown below there are eight possible directions for a screen-to-screen BitBLT (no change in position is a subset of all eight). Software must determine the overlap, if any, and set the INC_X and INC_Y bits accordingly. This is only critical if the source and destination actually overlap. For most BitBLTs this will not be the case. In BitBLTs where INC_X is a 'don't care' it should be set to 1 (proceed from left to right). This will increase the performance in some cases.



Possible BitBLT Orientations With Overlap

Sample Screen-to-Screen Transfer

Below is an example of how a screen-to-screen BitBLT operation is traditionally performed. The source and destination blocks both appear on the visible region of the screen and have the same dimensions. The BitBLT is to be a straight source copy with no raster operation. The memory address space is 2MBytes and display resolution is 1024 x 768. The size of the block to be transferred is 276 horizontal x 82 vertical pixels (114h x 52h). The coordinates of the upper left corner (ULC) of the source block is 25h,30h. The ULC coordinates of the destination block are 157h,153h. Because the source and destination blocks do not overlap, the INC_X and INC_Y BitBLT direction bits are not important. We will assume that INC_X = 1, INC_Y = 0, and the BitBLT will proceed one scan line at a time from the lower left corner of the source moving to the right and then from the bottom to the top.

The source and destination offsets are both the same as the screen width (400h):

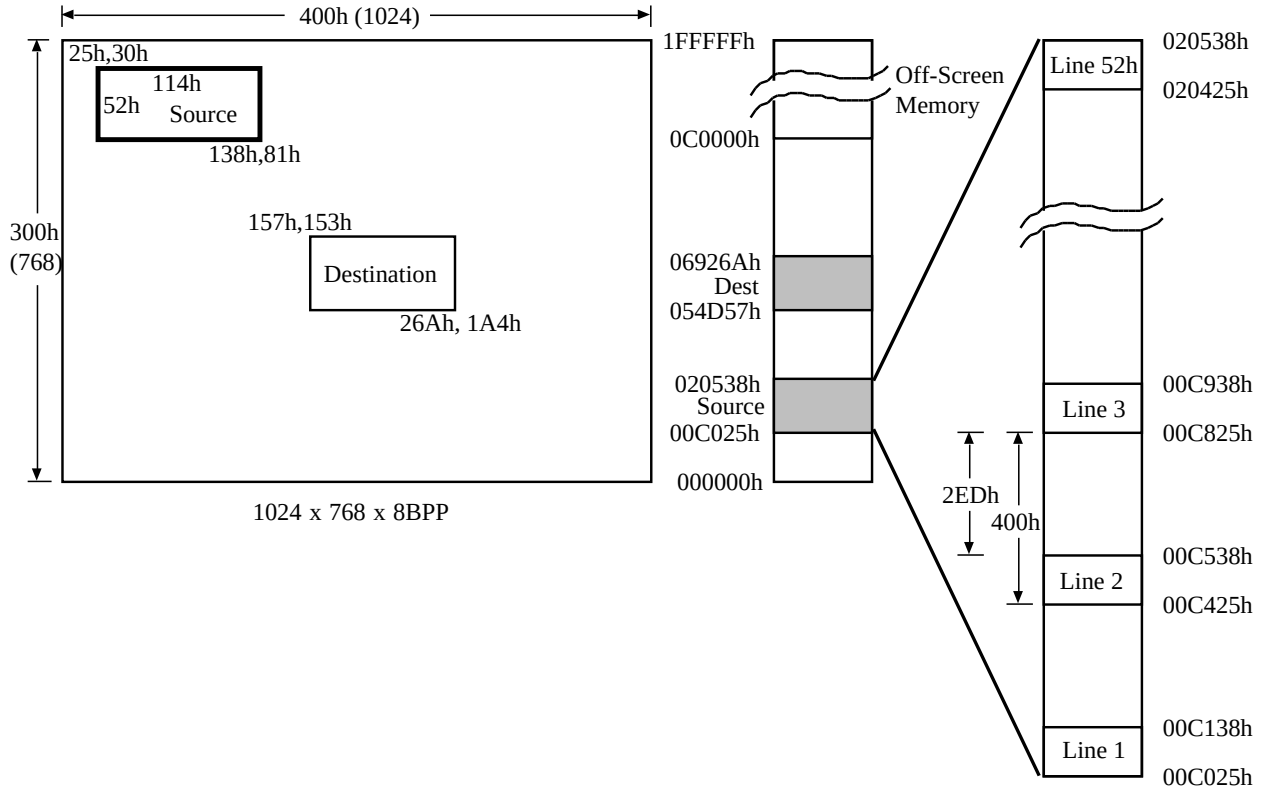
BitBLT Offset Register (DR00) = 04000400h

The Pattern ROP Register does not need to be programmed since there is no pattern involved. Neither the Foreground Color nor Background Color Register has to be programmed since this does not involve a color expansion or rectangle solid color paint. The BitBLT Control Register contains the most individual fields to be set:

ROP = Source Copy = 0CCh
INC_Y = 0 (Bottom to Top)
INC_X = 1 (Left to Right)
Source Data = Variable Data = 0
Source Depth = Source is Color = 0
Pattern Depth = Don't Care = 0
Background = Don't Care = 0
BitBLT = Screen-to-Screen = 00
Pattern Seed = Don't Care = 000

BitBLT Control Register (DR04) = 002CCh

Since the BitBLT will be starting in the lower left corner (LLC) of the source rectangle, the start address for the source data is calculated as:



Screen-to-Screen BitBLT

(81h * 400h) + 25h = 020425h
BitBLT Source Register (DR05) = 020425h

Similarly, the LLC of the destination register calculated as:

(1A4h * 400H) + 157h = 069157h

BitBLT Destination Register (DR06) = 069157h

To begin any BitBLT the Command Register must be written. This register contains key information about the size of the current BitBLT which must be written for all BitBLT operations:

Lines per Block = 52h
Bytes per line = 114h (Current example 8bpp)

Command Register (DR07) = 00520114h

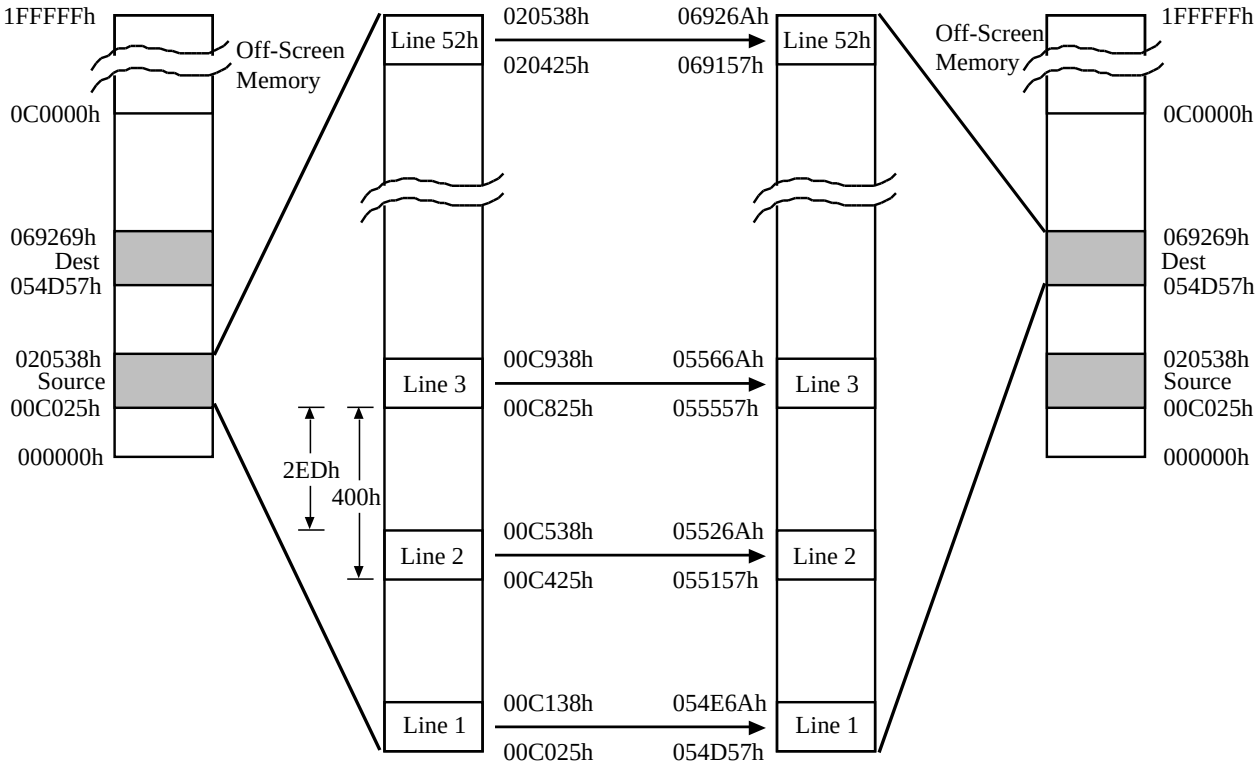
After the Command Register (XR07) is written the BitBLT engine performs the requested operation. The status of the BitBLT operation may be read in DR04[20] (read only bit). This is necessary to determine when the BitBLT is finished so that another BitBLT may be issued. No reads or writes of the display memory by the CPU are permitted while the BitBLT engine is active.

In the present example the BitBLT source and destination blocks have the same width as the display. As can be seen below each scan line is transferred from source to destination. Alignment is handled by the BitBLT engine without assistance from software.

Compressed Screen-to-Screen Transfer

Next we consider an example of how a screen-to-screen BitBLT operation is performed when the source and destination blocks have different widths (pitch). This type of BitBLT is commonly used to store bitmaps efficiently in offscreen memory or when recovering a saved bitmap from offscreen memory.

The 65545 display memory consists of a single linear frame buffer. The number of bytes per scan line and lines displayed changes with resolution and pixel depth. For simplification, the concepts of pixels,



BitBLT Data Transfer

lines, and columns are foreign to the BitBLT engine. Instead, the 65545 operates on groups of bytes (rows) which are separated by the width of the screen. The 65545 permits separation between the row lengths to be different for source and destination bitmaps. For efficient use of offscreen memory we may assume that the "width" of the screen is the same as the width of the data.

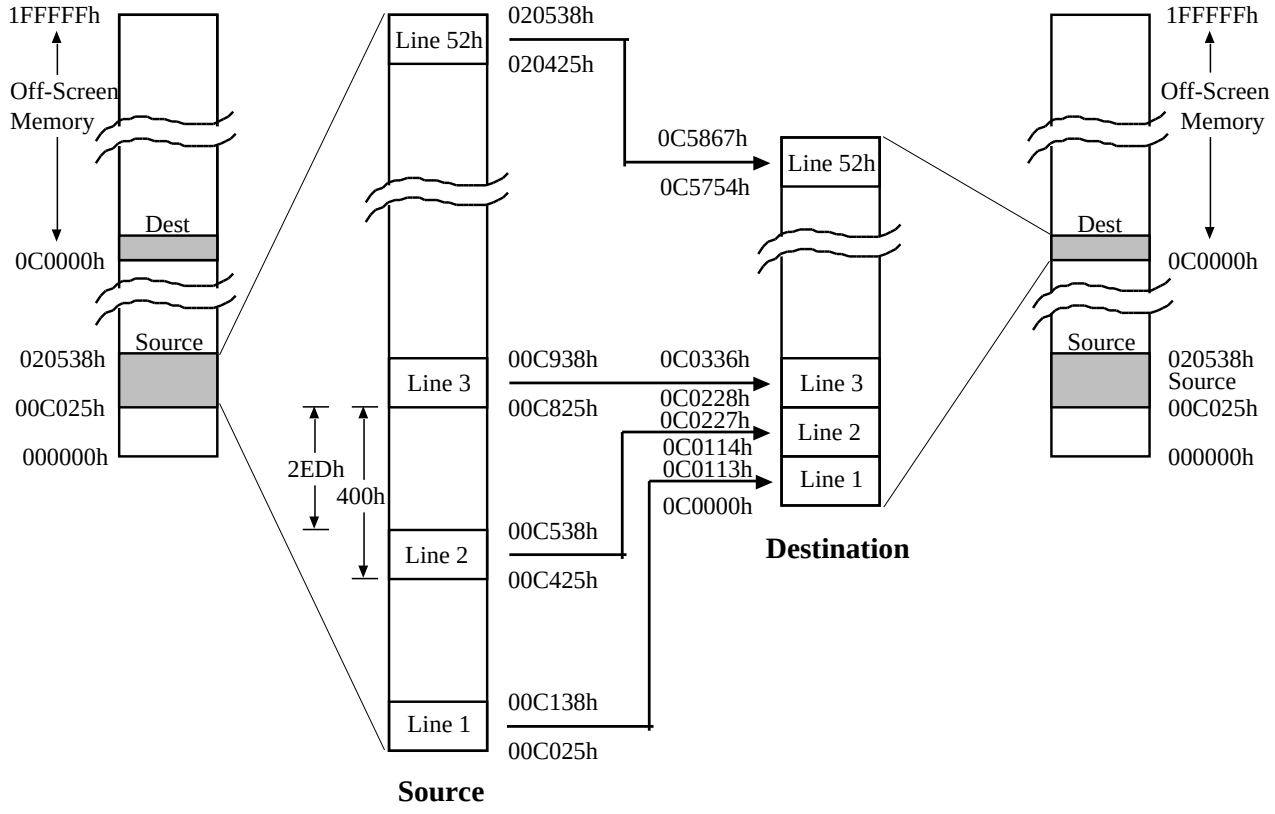
Below is an example of how a screen-to-screen BitBLT operation is performed with the destination data efficiently compressed into the offscreen area. The reverse operation is also valid to recreate the original block on the visible screen. Once again the BitBLT is to be a straight source copy with the source block in the same location as the previous example. The destination block is to be located beginning at the first byte of off-screen memory. Because the source and destination blocks do not overlap the INC_X and INC_Y BitBLT direction bits are not important. We will assume that INC_X = 1, INC_Y = 1 and the BitBLT will proceed one scan line at a time from the upper left corner of the source moving to the right and then from the top to the bottom.

The source offset is the same as the screen width (400h) and the destination offset is the same as the source block width (114h):

BitBLT Offset Register (DR00) = 01140400h

The Pattern ROP Register does not need to be programmed since there is no pattern involved. Neither the Foreground Color nor Background Color Register has to be programmed since there is no color expansion. The BitBLT Control Register contains the following bit fields:

ROP = Source Copy = 0CCh
INC_Y = 1 (Top to Bottom)
INC_X = 1 (Left to Right)
Source Data = Variable Data = 0
Source Depth = Source is Color = 0
Pattern Depth = Don't Care = 0
Background = Don't Care = 0
BitBLT = Screen --> Screen = 00



Differential Pitch BitBLT Data Transfer

Pattern Seed = Don't Care = 000

BitBLT Control Register (DR04) = 003CCh

Since the BitBLT will be beginning in the ULC of the source rectangle, the start address for the source data is calculated as:

(30h * 400h) + 25h = 0C025h
BitBLT Source Register (DR05) = 0C025h

Similarly, the ULC of the destination register calculated as (Number of scan lines * Bytes per scan line):

300h * 400h = 0C0000h

BitBLT Destination Register (DR06) = 0C0000h

As in the previous example the Command Register must be written to begin the BitBLT. This register contains the size of the current BitBLT which must be written for all BitBLT operations:

Lines per Block = 52h
Bytes per line = 114h (Current example 8bpp)

Command Register (DR07) = 00520114h

System-to-Screen BitBLTs

When performing a system-to-screen BitBLT the source rotation information is passed in the BitBLT Source Address and Source Offset registers. The 2 LSbits of the Source Address register indicate the alignment. For example if the system data resides at system address 0413456h then the processor pointer should be set to 0413454h (doubleword aligned) and the Source address register is written with xxxxx2h. When the end of the scan line is reached (the number of bytes programmed in the Command Register have been written) any remaining bytes in the last doubleword written to the 65545 are discarded. The 2 LSbits of the Source Offset Register are then added to the 2 LSbits of the Source Address Register to determine the starting byte alignment for the first doubleword of the next scanline. This process is continued until all scanlines are completed. The most common case will be a doubleword aligned bitmap in system memory in which case the 2 Lbits of the Source Address Register are zero. It is also common for bitmaps to be stored with each scanline doubleword aligned (Source Offset Register = xxxxx0h). Once the Command Register is written and the BitBLT operation has begun the 65545 will wait for data to be sent to its memory address space. Any write to a valid 65545 memory address, either in the VGA space or linear address space if enabled, will be recognized as BitBLT source data and will be routed to the correct address by the BitBLT engine. This enables the programmer to set up a destination pointer into the video address window (doubleword aligned) and simply perform a REP MOVSD. Any unused data in the last word/doubleword write will be discarded by the BitBLT Engine.

For system-to-screen monochrome (font) expansions the data is handled on a scanline by scanline basis. As with the system-to-screen BitBLT with ROP, this type of transfer uses the 2 LSbits of the source address register to determine the beginning byte index into the first doubleword. On subsequent scanlines the source offset register is added to the current scanline byte index to determine the indexing for the start of the next scan line. Monochrome data is taken from bit 7 through bit 0, byte 0 through 3 and expanded left to right in video memory (NOTE: monochrome source only supports left to right operation). At the end of the first scanline any remaining data in the active doubleword is flushed and the byte pointer for the starting byte in the next doubleword (for the next scanline) is calculated by adding 2 LSbits of the source offset to the starting byte position in the previous scanline. Monochrome expansion then continues bit 7 through 0 incrementing byte (after byte 3 bit 0 a new doubleword begins at byte 0: bit 7) until the scanline is complete. Note that the number of bytes programmed into the Command register references the number of expanded bytes written; not the number of bytes to be expanded.

Hardware Cursor (65545 only)

The 65545 supports four types of cursors:

32 x 32	x 2bpp	(and/xor)
64 x 64	x 2bpp	(and/xor)
64 x 64	x 2bpp	(4-color)
128 x 128	x 1bpp	(2-color)

The first two hardware cursor types indicated as 'and/xor' above follow the MS Windows™ AND/XOR cursor data plane structure which provides for two colors plus 'transparent' (background color) and 'inverted' (background color inverted). The last two types in the list above are also referred to as 'Pop-Ups' because they are typically used to implement pop-up menu capabilities. Hardware cursor / pop-up data is stored in display memory, allowing multiple cursor values to be stored and selected rapidly. The two or four colors specified by the values in the hardware cursor data arrays are stored in on-chip registers as high-color (5-6-5) values independent of the on-chip color lookup tables (i.e., Attribute Controller and VGA Color Palette).

The hardware cursor can overlay either graphics or video data on a pixel by pixel basis. It may be positioned anywhere within screen resolutions up to 2048x2048 pixels. 64x64 'and/xor' cursors may also be optionally doubled in size to 128 pixels either horizontally and/or vertically by pixel replication.

Hardware cursor screen position, type, color, and base address of the cursor data array in display memory may be controlled via the 32-bit 'DR' extension registers.

Hardware Cursor Programming

Once the 32-bit extension registers are enabled (XR03[1]=1), the cursor registers (DR08-DR0C) may be accessed. DR08 controls the cursor type and X/Y zoom (H/V pixel replication). It also enables the hardware cursor to appear on the screen. DR09 and DR0A specify up to four 16-bit RGB (5-6-5) cursor color values. DR0B specifies the cursor position on screen in X-Y coordinates (number of pixels from the left and top edges of the addressable portion of the display). DR0C specifies the address in display memory where the cursor data array is stored. A 10-bit base address may be specified allowing cursor data patterns to be stored in any of 1024 different locations in the maximum 1MB of display memory. Each cursor storage area takes up 1024 bytes of display memory which is exactly large enough to hold a 64x64x2 cursor pattern.

Cursor Data Array Format and Layout

Cursor data is stored in display memory as shown:

32x32 2bpp Cursor

Offset	Line	Plane 0	Plane 1	Plane 2	Plane 3
000h	0	A7-0	X7-0	A15-8	X15-8
004h	0	A23-16	X23-16	A31-24	X31-24
008h	1	A7-0	X7-0	A15-8	X15-8
00Ch	1	A23-16	X23-16	A31-24	X31-24
...	...	...	...	...	...
0FCh	31	A23-16	X23-16	A31-24	X31-24

64x64 2bpp Cursor / Pop-Up

Offset	Line	Plane 0	Plane 1	Plane 2	Plane 3
000h	0	A7-0	X7-0	A15-8	X15-8
004h	0	A23-16	X23-16	A31-24	X31-24
008h	0	A39-32	X39-32	A47-40	X47-40
00Ch	0	A55-48	X55-48	A63-56	X63-56
010h	1	A7-0	X7-0	A15-8	X15-8
014h	1	A23-16	X23-16	A31-24	X31-24
...	...	...	...	...	...
3FCh	63	A55-48	X55-48	A63-56	X63-56

128x128 1bpp Pop-Up

Offset	Line	Plane 0	Plane 1	Plane 2	Plane 3
000h	0	P7-0	P15-8	P23-16	P31-24
004h	0	P39-32	P47-40	P55-48	P63-56
008h	0	P71-64	P79-72	P87-80	P95-88
00Ch	0	P103-96	P111-104	P119-112	P127-120
010h	1	P7-0	P15-8	P23-16	P31-24
014h	1	P39-32	P47-40	P55-48	P63-56
...	...	...	...	...	...
7FCh	127	P103-96	P111-104	P119-112	P127-120

A7/X7 is the left-most pixel of the cursor pattern displayed on the screen for all cursor types. Note that 32x32 cursors take up 256 bytes each (the upper 3/4 of the 1KB space allocated for each cursor storage location in display memory is unused). 128x128 cursors (pop-ups) take up 2KB each, so require A10 of the base address to be set to 0.

Cursor data array elements map as follows:

Ann	Xnn	And/Xor Type	4-Color Type
0	0	Color 0	Color 0
0	1	Color 1	Color 1
1	0	Transparent	Color 2
1	1	Inverted	Color 3

where colors 0 and 1 are defined by DR09 and colors 2 and 3 are defined by DR0A. Each pixel in 2-color (1bpp) cursors (pop-ups) may be either color 0 or color 1.

Display Memory Base Address Formation

The address bits in the cursor base address register DR0C are aligned so they are in the proper position corresponding to the CPU address required to write to display memory. However, there are two methods of addressing display memory, VGA-style and 'Linear Frame Buffer' style, so the actual CPU address for loading a cursor data array must be constructed differently depending on the addressing method used. If VGA addressing is used, the lower 16-bits of DR0C may be used as an offset into the 64KB VGA address space (starting at either 0A0000h or 0B0000h depending on whether the VGA is set for text mode or graphics mode). DR0C bits 16-19 would then be used to control the VGA's paging mechanism to set the 64KB CPU aperture into display memory to the correct location for storing the cursor pattern (see XR0B, XR10, and XR11). If 'linear frame buffer' addressing is used, the entire 1MB of display memory can be accessed directly and the base value in DR0C may be used directly as a 24-bit offset into a programmable 1MB space in system memory (specified in the Linear Addressing Base register XR08).

VGA Controller Programming

In order to copy the cursor data pattern to the controller, the VGA controller must be properly programmed for 32-bit direct access to all 4 planes. Proper programming for the controller consists of putting the controller in either 'text' or 'graphics' mode and then setting the following registers as indicated:

SR04	=0Eh	Sequencer Memory Mode
SR02	=0Fh	Sequencer Plane Mask
GR05	=00h	Graphics Controller Mode
GR06	=04h (text mode)	Graphics Controller Misc
	=05h (gr mode)	Graphics Controller Misc
XR0B	=x5h	Paging Control

This sets up the VGA controller to allow 32-bit direct access to all 4 planes of all 1MB of display memory in a linear fashion. It also sets the VGA memory aperture to a 64KB space at 0A0000h independent of initial graphics or text mode settings.

Copying Cursor Data to Display Memory

Once the base address for the cursor data pattern in display memory has been determined and the VGA has been properly programmed, the cursor data pattern may be copied from system memory to display memory. The following program sequence shows an example of one method which may be used:

es:edi = display memory base address for cursor
ds:si = address of AND array in system memory
ds:bx = address of XOR array in system memory

```
MOV     AL, [SI+1]
MOV     AH, [BX+1]
SHL     EAX,16
MOV     AL, [SI]
MOV     AH, [BX]
STOSD
```

Setting the Cursor Position, Type, and Base Address

Following storage of the cursor data array in display memory, the location of the cursor in display memory is set via the Cursor Base Address register (DR0C) and the X-Y coordinates for positioning the cursor are written to the Cursor Position Register (DR0B). The cursor type and X/Y zoom (H/V pixel replication) factors are then set and the cursor enabled via the Cursor Control Register (DR08).

To update the cursor position, a 32-bit write (or two 16-bit writes) are performed to the Cursor Position Register (DR0B). This new position will take effect on the next frame (synchronized to VSync).

When the cursor changes shape, it should normally be disabled, reprogrammed as described above, and then re-enabled. Alternately, a new shape may be stored in a different location in display memory, the cursor screen XY location updated (via DR0B), then the new cursor selected as the active cursor (by reprogramming the base register DR0C). Cursor base register changes are also synchronized to VSync to avoid glitching of the cursor on the display.

Flat Panel Timing

Overview

A number of extension registers in the 65540 / 545 control the panel interface, including the functions of the interface pins and the timing sequences produced for compatibility with various types of panels. Some key registers of interest for panel interfacing are:

XR1C H Panel Size (# of characters – 1)
XR68 V Panel Size (# of scan lines – 1) bits 0-7 (XR65[1]=Vsize bit-8, XR65[6]=bit-9)

XR4F Panel Format 2 (Bits/pixel,M/LP function)
XR50 Panel Format 1 (FRC,dither,clkdiv,VAM)
XR51 Display Type (Panel type,clk/LP control)
XR53 Panel Format 3 (FRC opt,pixel packing)
XR54 Panel Interface (FLM/LP Control)
XR5E M (ACDCLK) Control
XR6F Frame Buffer Control

This section summarizes the function of the various fields of the above registers as they pertain to panel interfacing. Detailed timing diagrams are shown for output of data and control sequences to a variety of panel types. The 65540 / 545 highly configurable controllers can interface to virtually all existing monochrome LCD, EL, and Plasma panels and all color LCD STN and TFT panels. The panel types supported are:

Single panel-Single drive (SS) Monochrome
1 pixel/clock, 8 bits/pixel
2 pixels/clock, 8 bits/pixel
4 pixels/clock, 4 bits/pixel
8 pixels/clock, 2 bit/pixel
16 pixels/clock, 1 bit/pixel

Dual panel-Double drive (DD) Monochrome
8 pixels/clock, 1 bit/pixel
16 pixels/clock, 1 bit/pixel

Single panel-Single drive (SS) Color TFT
1 pixel/clock, 16 bit/pixel 5-6-5 RGB
1 pixel/clock, 24 bit/pixel 8-8-8 RGB
2 pixels/clock, 12 bit/pixel 4-4-4 RGB

Single panel-Single drive (SS) Color STN
2 2/3 pixels/clock, 3 bit/pixel 1-1-1 RGB
5 1/3 pixels/clock, 3 bit/pixel 1-1-1 RGB

Dual panel-Double drive (DD) Color STN
2 2/3 pixels/clock, 3 bit/pixel 1-1-1 RGB
5 1/3 pixels/clock, 3 bit/pixel 1-1-1 RGB

Panel Size

The horizontal panel size register (XR1C) is an 8-bit register programmed with panel width (minus one) in units of 8-pixel characters (e.g., a 640x480 panel is 80 'characters' wide so XR1C would be programmed with 79 decimal). The vertical panel size register is programmed with the panel height (minus one) in scan lines (independent of single or dual panel type). The programmed value is 10 bits in size with the 8 lsbs in XR68 and the overflow in XR65 bits 1 and 6. The maximum panel resolution supported is 2048 x 1024.

Panel Type

The panel type (PT) is determined by XR51 bits 1-0:

00 Single panel-Single drive (SS)
11 Dual panel-Double drive (DD)

For DD panels, XR6F bit-0 (Frame Buffer Enable) and/or bit-1 (Frame Accelerator Enable) must also be set (either external or embedded may be used).

TFT Panel Data Width

XR50 bit-7 controls output width for TFT panels:

0 16-bit color TFT panel interface (565 RGB)
1 24-bit color TFT panel interface (888 RGB)

Display Quality Settings

Frame Rate Control (FRC)

The 65540 / 545 provides 2 and 16 level FRC to generate multiple gray / color levels. FRC selection is determined by XR50 bits 1-0:

00 No FRC
01 16-frame FRC (color or mono STN panels)
10 2-frame FRC (color TFT or mono panels)

Three options are provided for FRC control:

FRC option 1 (XR53[2]) (always set to 1)
FRC option 2 (XR53[3]) (always set to 1)
FRC option 3 (XR53[6]) (for 2-frame FRC only):

0 FRC data changes every frame
1 FRC data changes every other frame

A setting of 0 typically results in better display quality, but panels with an internal 'M' signal typically recommend this bit be set to 1 for longer panel life.

XR6E is also provided for FRC polynomial control. The values of the 'm' and 'n' parameters are typically set by trial and error (recommended settings are given elsewhere in this manuals for selected panels as derived by Chips and Technologies).

Dither

The 65540 / 545 also provides Dither capability to generate multiple gray / color levels. Ditherselection is determined by XR50 bits 3-2:

00 No Dither
01 Enable Dither for 256-color modes only
10 Enable Dither for all modes

M Signal Timing

Register XR5E (M/ACDCLK Control) is provided to control the timing of the M (sometimes called ACDCLK) signal. XR5E bit-7 selects between two types of timing control:

0 Use XR5E bits 0-6 to determine M signal timing (bits 0-6 are programmed with the number of HSYNCs between phase changes minus 2)
1 M phase changes every frame if the frame buffer is used, otherwise the phase changes every other frame

XR4F bit-6 controls the M pin output. If set, the M pin will output flat panel BLANK# / Display Enable (DE) instead of the normal M signal (and XR5E will be ignored).

Gray / Color Levels

Gray / color levels are selected via XR4F bits 2-0 (somewhat misleading called 'Bits Per Pixel'):

No FRC

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61
101	5	32	125
110	6	64	253
111	8	256	n/a

2-Frame FRC
(Color TFT or Monochrome Panels)

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
010	1	3	9
011	2	5	25
100	3	15	57
101	4	31	121

16-Frame FRC
(Color or Monochrome STN Panels)

	# of msbs Used to Generate Gray/Color Levels	Gray / Color Levels	Gray / Color Levels with Dithering
001	1	2	5
010	2	4	13
011	3	8	29
100	4	16	61

The setting programmed into XR4F bits 0-2 above determines how many most-significant color-bits / pixel are used to generate flat panel video data. In general, 8 bits of monochrome data or 8 bits/color of RGB color data enter the flat panel logic for every dot clock. Not all of these bits, however, are used to generate output colors / gray scales, depending on the type of panel used, graphics / text mode, and the gray-scaling algorithm chosen (the actual number of bits used is indicated in the table above). Also note that settings which achieve higher gray / color levels may not necessarily produce acceptable display quality on some (or any) currently available panels. This document contains recommended settings for various popular panels that Chips & Technologies has found to produce acceptable results with those panels. Customers may modify these settings to achieve a better match with their requirements.

Pixels Per Shift Clock

The 65540 / 545 can be programmed to output 1, 2, 4, 8, or 16 pixels per shift clock. This is achieved by programming the frequency ratio between the dot clock and the shift clock. The shift clock divide (CD) is set by XR50 bits 6-4. For monochrome panels, the valid settings are:

	Shift Clock	Pixels Per Shift Clock without Frm Acc	Pixels Per Shift Clock with Frm Acc
000	Dot clk	1	2
001	Dclk / 2	2	4
010	Dclk / 4	4	8
011	Dclk / 8	8	16
100	Dclk / 16	16	n/a

Pixels Per Shift Clock	8-Bit Panel Interface	Valid Outputs (8-bit)	16-Bit Panel Interface	Valid Outputs (16-bit)
1	8bpp	P8-15	8bpp	P8-15
2	4bpp	P8-15 (8-11 1st)	8bpp	P0-15
4	2bpp	P8-15 (8-9 1st)	4bpp	P0-15
8	1bpp	P1,3,5,... (1 1st)	2bpp	P0-15
16	n/a	n/a	1bpp	P0-15

The pixel on the lowest numbered output pin is always the first pixel output (the pixel shown first on the left side of the screen). For example, for 8 pixels per clock, 1bpp on an 8-bit interface, P1 is the first pixel, P3 is the second, etc. For 16 pixels per clock, 1bpp on a 16-bit interface, P0 is the first pixel, P1 is the second, etc. For 4 pixels per clock, 2bpp on an 8-bit interface, P8-9 is the first pixel, P10-11 is the second, etc.

	24bit Color	24bit Color	16bit Color	8bit Mono	16bit Mono	16bit Mono	16bit Mono
Pix/clk:	1	2	1	1	2	4	8
CD:	000	001	000	000	001	010	011
P0	B0n	B4n	B3n	–	G0n	G4n	G6n
P1	B1n	B5n	B4n	–	G1n	G5n	G7n
P2	B2n	B6n	B5n	–	G2n	G4n+1	G6n+1
P3	B3n	B7n	B6n	–	G3n	G5n+1	G7n+1
P4	B4n	B4n+1	B7n	G0n†	G0n+1	G4n+2	G6n+2
P5	B5n	B5n+1	G2n	G1n†	G1n+1	G5n+2	G7n+2
P6	B6n	B6n+1	G3n	G2n†	G2n+1	G4n+3	G6n+3
P7	B7n	B7n+1	G4n	G3n†	G3n+1	G5n+3	G7n+3
P8	G0n	G4n	G5n	G0n	G4n	G6n	G6n+4
P9	G1n	G5n	G6n	G1n	G5n	G7n	G7n+4
P10	G2n	G6n	G7n	G2n	G6n	G6n+1	G6n+5
P11	G3n	G7n	R3n	G3n	G7n	G7n+1	G7n+5
P12	G4n	G4n+1	R4n	G4n	G4n+1	G6n+2	G6n+6
P13	G5n	G5n+1	R5n	G5n	G5n+1	G7n+2	G7n+6
P14	G6n	G6n+1	R6n	G6n	G6n+1	G6n+3	G6n+7
P15	G7n	G7n+1	R7n	G7n	G7n+1	G7n+3	G7n+7
P16	R0n	R4n	–	–	–	–	–
P17	R1n	R5n	–	–	–	–	–
P18	R2n	R6n	–	–	–	–	–
P19	R3n	R7n	–	–	–	–	–
P20	R4n	R4n+1	–	–	–	–	–
P21	R5n	R5n+1	–	–	–	–	–
P22	R6n	R6n+1	–	–	–	–	–
P23	R7n	R7n+1	–	–	–	–	–

† For information only, not recommended for panel connections

The number of bits per pixel is determined as follows:

1bpp: Bits/Pixel=000 or 001 or
16-Frame FRC or
2-Frame FRC with Bits/Pixel=010

2bpp: Not 1bpp and CD=011 (8 Pixels/Clock)

4bpp: Not 1bpp and CD=010 (4 Pixels/Clock)

8bpp: Not 1bpp and CD=001 (2 Pixels/Clock) or
Not 1bpp and CD=000 (1 Pixels/Clock)

Valid Color TFT panel shift clock divide settings are:

	Pixels per Shift Clock	TFT Output Width	TFT Output Format	"B0-n" Panel Outputs	"G0-n" Panel Outputs	"R0-n" Panel Outputs
000	1	16	5-6-5	P0-4	P5-10	P11-15
		24	8-8-8	P0-7	P8-15	P16-23
001	2	24	4-4-4	P0-3	P8-11	P16-19
				P4-7	P12-15	P20-23

For 2 pixels/shift clock, the first pixel output is on P0-3, 8-11, and 16-19.

For Color STN, valid shift clock divide settings are:

	Pixels Per Clock without FrameAcceleration SS or DD Panels	Pixels Per Clock with FrameAcceleration DD Panels Only
000	1	2
001	2	4
010	4	n/a

For Color STN data, pixel output sequences are controlled by the 'Color STN Pixel Packing' bits (XR53[5-4]) described on the following page (packing may be selected as '3-Bit Pack', '4-Bit Pack', or 'Extended 4-Bit Pack' sometimes referred to in this document as 3bP, 4bP, and X4bP). All cases in the above table can use 3-Bit Pack or 4-Bit Pack. Extended 4-Bit Pack is only used for the single case of 2 pixels per shift clock without frame acceleration. Pixel Packing is not used for EL/Plasma, Monochrome DD, or Color TFT panels so the pixel packing bits should be set to 00 for all panels except color STN.

Shift Clock Divide

The above clock divide ('CD') bits (XR50 bits 6-4) affect both shift clock and data out. XR51[3] (Shift Clock Divide or SD) may be set so that only the shift clock (and not the video data) is further divided by two beyond the setting of XR50 bits 6-4. This has the effect of causing a new pixel to be output on every clock edge (i.e., both rising and falling) instead of just every falling clock edge (the first pixel output on every scan line will be on the rising edge).

Extended 4-Bit Pack for Color STN panels requires that the SD bit (XR51[3]) be set to 1. In all other cases in the Color STN table above, either setting may be used.

Color STN Pixel Packing (Pixel Output Order)

For color STN panels, pixel packing must be selected via XR53 bits 5-4:

	Packing	CD Settings Allowable
00	3-Bit Pack	SS: 000, 001, or 010 DD: 000, 001 (010 w/o FA)
01	4-Bit Pack	SS: 000, 001, or 010 DD: 000, 001 (010 w/o FA)
11	Ext'd 4-Bit Pack	SS: 001 (8bit panels only)

These settings are valid for color STN panels only (these bits must be set to 00 for monochrome and color TFT panels).

Pixel output order for 3-Bit Pack STN-SS panels without frame acceleration:

	CD=000 (1p/clk) ShfClk Edge				CD=001 (2p/clk) Shift Clock Edge				CD=010 (4p/clk) Shift Clock Edge			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
P0	–	–	–					...				...
P1	R1	R2	R3	...	R1	R3	R5	...	R1	R5	R9	...
P2	G1	G2	G3	...	G1	G3	G5	...	G1	G5	G9	...
P3	B1	B2	B3	...	B1	B3	B5	...	B1	B5	B9	...
P4	–	–	–		–	–	–		–	–	–	
P5	–	–	–		R2	R4	R6	...	R2	R6	R10	...
P6	–	–	–		G2	G4	G6	...	G2	G6	G10	...
P7	–	–	–		B2	B4	B6	...	B2	B6	B10	...
P8	–	–	–		–	–	–					...
P9	–	–	–		–	–	–		R3	R7	R11	...
P10	–	–	–		–	–	–		G3	G7	G11	...
P11	–	–	–		–	–	–		B3	B7	B11	...
P12	–	–	–		–	–	–		–	–	–	
P13	–	–	–		–	–	–		R4	R8	R12	...
P14	–	–	–		–	–	–		G4	G8	G12	...
P15	–	–	–		–	–	–		B4	B8	B12	...

	4b Pack, CD=001 Shift Clock Edge				Ext'd 4b Pack, CD=001 Shift Clock Edge						
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	5th	6th	7th
P0	R1	B3	G6	...	R1	G1	G6	B6	B11	R12	...
P1	G1	R4	B6	...	B1	R2	R7	G7	G12	B12	...
P2	B1	G4	R7	...	G2	B2	B7	R8	R13	G13	...
P3	R2	B4	G7	...	R3	G3	G8	B8	B13	R14	...
P4	G2	R5	B7	...	B3	R4	R9	G9	G14	B14	...
P5	B2	G5	R8	...	G4	B4	B9	R10	R15	G15	...
P6	R3	B5	G8	...	R5	G5	G10	B10	B15	R16	...
P7	G3	R6	B8	...	B5	R6	R11	G11	G16	B16	...

The pixel sequence for 3-bit Pack repeats with either 1, 2, or 4 pixels every shift clock edge depending on the setting of the clock divide (CD) field. The pixel sequence for 4-bit Pack repeats with 8 pixels every 3 shift clock edges. The sequence for Extended 4-Bit Pack repeats with 16 pixels every 6 shift clock edges. Extended 4-bit Pack is used only for 8-bit color STN-SS panels. It is not used for color STN DD panels or for 16-bit color STN interfaces.

Pixel output order for 4-Bit Pack 8-bit STN DD panels:

	Shift Clock Edge 1st	2nd	3rd	4th
Upper:				
P0	R1	G2	B3	...
P1	G1	B2	R4	...
P2	B1	R3	G4	...
P3	R2	G3	B4	...
Lower:				
P4	R1	G2	B3	...
P5	G1	B2	R4	...
P6	B1	R3	G4	...
P7	R2	G3	B4	...

The pixel sequence repeats with 8 pixels (4 for each of the upper and lower panels) every 3 shift clock edges. Clock divide must be set to 000 with Frame Acceleration and 001 without Frame Acceleration.

Pixel output order for 16-bit STN panels (4bit Pack):

	STN-SS Panels Shift Clock Edge				STN-DD Panels Shift Clock Edge				
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	
P0	R1	G6	B11	...	Upper:				
P1	G1	B6	R12	...	P0	R1	B3	G6	...
P2	B1	R7	G12	...	P1	G1	R4	B6	...
P3	R2	G7	B12	...	P2	B1	G4	R7	...
P4	G2	B7	R13	...	P3	R2	B4	G7	...
P5	B2	R8	G13	...					
P6	R3	G8	B13	...	P8	G2	R5	B7	...
P7	G3	B8	R14	...	P9	B2	G5	R8	...
P8	B3	R9	G14	...	P10	R3	B5	G8	...
P9	R4	G9	B14	...	P11	G3	R6	B8	...
P10	G4	B9	R15	...	Lower:				
P11	B4	R10	G15	...	P4	R1	B3	G6	...
P12	R5	G10	B15	...	P5	G1	R4	B6	...
P13	G5	B10	R16	...	P6	B1	G4	R7	...
P14	B5	R11	G16	...	P7	R2	B4	G7	...
P15	R6	G11	B16	...					
					P12	G2	R5	B7	...
					P13	B2	G5	R8	...
					P14	R3	B5	G8	...
					P15	G3	R6	B8	...

For STN-SS panels the pixel sequence repeats with 16 pixels every 3 shift clock edges (5-1/3 pixels per shift clock edge). Clock divide must be set to 010.

For STN-DD panels the pixel sequence repeats with 16 pixels (8 for each of the upper and lower panels) every 3 shift clock edges (2-2/3 pixels per shift clock edge per panel). Clock divide must be set to 001 with Frame Acceleration and 010 without Frame Acceleration.

Output Signal Timing

LP Signal Timing

LP output polarity is controlled by XR54[6] (0=positive, 1=negative). Setting XR4F bit-7, however, causes the LP pin to output flat panel BLANK# / DE instead of the normal LP signal (and all other LP timing control parameters will be ignored). Some panels (e.g., Plasma and EL) require LP to be active during vertical blank time. XR51[7] may be set to enable this. Otherwise LP pulses are not generated during vertical blank.

FLM Output Signal Timing

FLM signal output polarity is controlled by XR54[7] (0=positive, 1=negative).

BLANK# / DE Output Signal Timing

The polarity of the BLANK# / DE output (if selected for output on M, LP, or FLM as indicated above) may be controlled by XR54[0] (0=positive, 1=negative). XR54[1] selects whether BLANK# / DE outputs both H and V (0) or just H (1). XR51[2] selects whether BLANK# / DE is generated from CRT Blank or Flat Panel Blank.

SHFCLK Output Signal Timing

XR51[5] (Shift Clock Mask or SM) may be set to force the shift clock output low outside the display enable interval.

Pixel Timing Diagrams

Pixel output timing sequences are shown for the following panel configurations:

1) **SS Monochrome Plasma / EL**

Single Panel-Single Drive (Panel Type = 00)
Plasma/EL Panel
2 pixels/shift clock, 4 bits/pixel (CD = 001)

2) **DD Monochrome LCD**

Dual Panel-Double Drive (Panel Type = 11)
Monochrome LCD Panel
8 pixels/shiftclk, 1bit/pixel, CD = 011
(010 with FB)
16 pixels/shiftclk, 1bit/pixel, CD = 100
(011 with FB)

3) **SS Color TFT LCD**

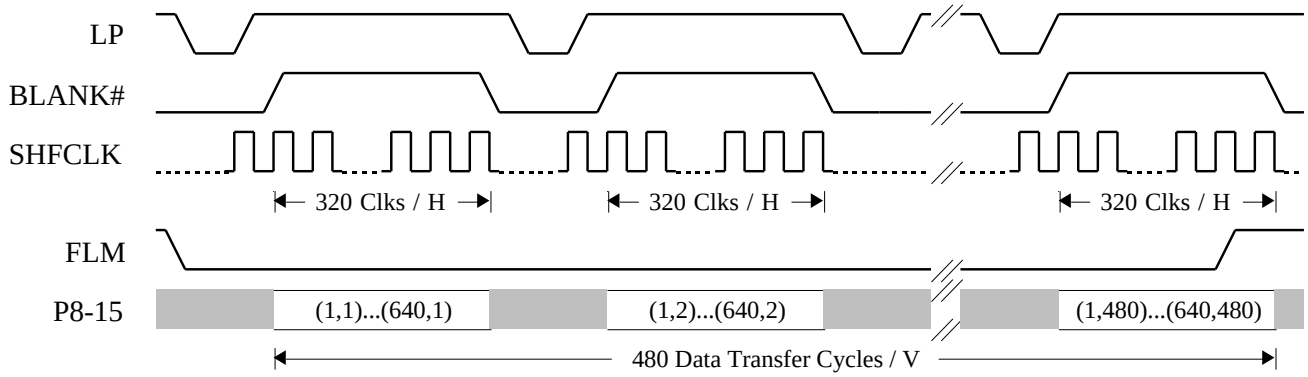
Single Panel-Single Drive (Panel Type = 00)
Color TFT LCD Panel
4/5/6/8 bits/color/pixel (12/16/18/24 bits total)
1 pixel/shift clock, 16-bit 5-6-5 RGB, CD=000
1 pixel/shift clock, 24-bit 8-8-8 RGB, CD=000
2 pixels/shift clock, 24-bit 4-4-4 RGB, CD=001

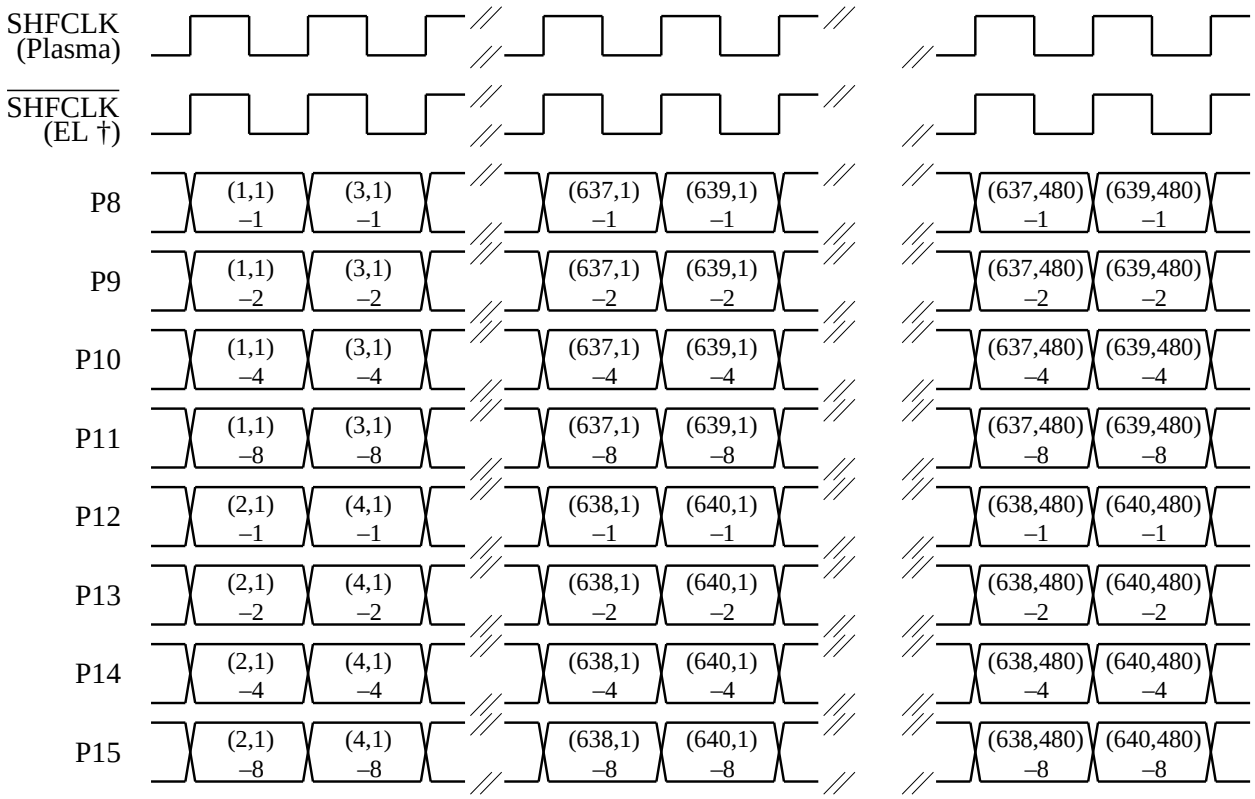
4) **SS Color STN LCD**

Single Panel-Single Drive (Panel Type = 00)
Color STN LCD Panel
1 bit/color/pixel (3 bits total) 1-1-1 RGB
1 pixel/shiftclk (3bit), CD=000
2 pixels/shiftclk (6bit), CD=001
2-2/3 pixels/shift clock (8bit), CD=010
5-1/3 pixels/shift clock (8bit), CD=010, SD=1
5-1/3 pixels/shift clock (16bit), CD=010

5) **DD Color STN LCD**

Dual Panel-Dual Drive (Panel Type = 11)
Color STN LCD Panel
All timings = 1 bit/color/pixel (3 bits total) RGB
2-2/3 pixels/shift clock (8-bit), CD=001
5-1/3 pixels/shift clock (16-bit), CD=010

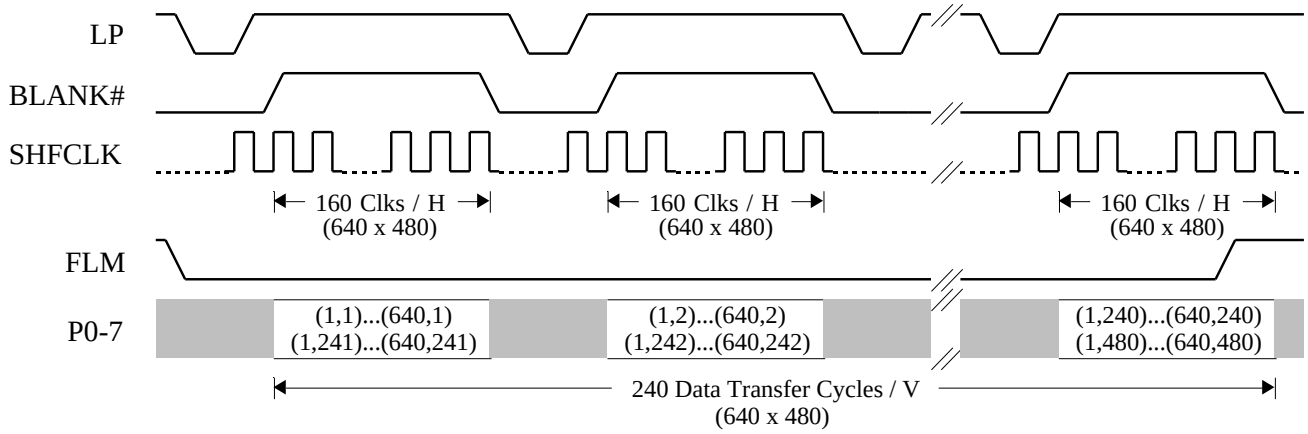




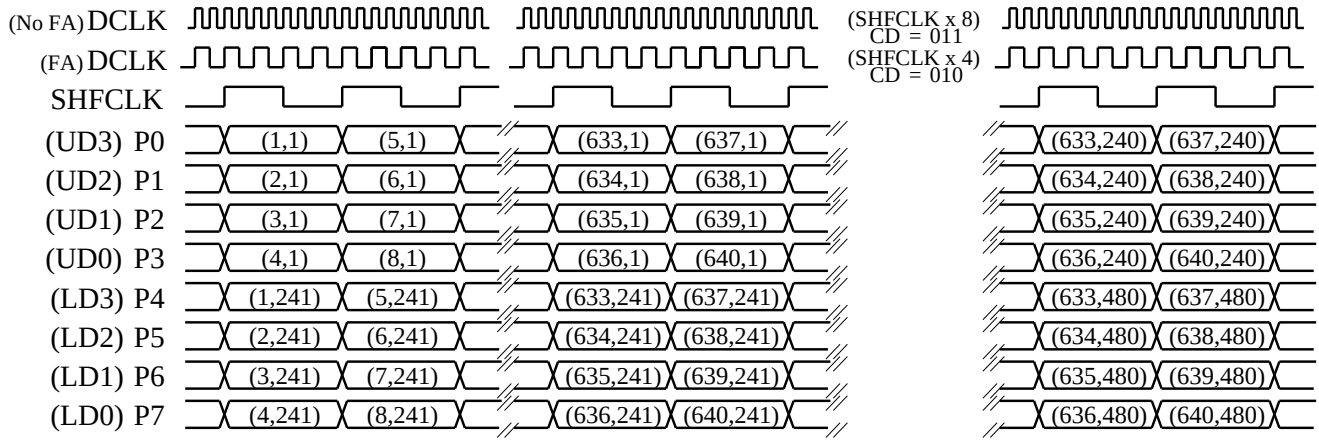
† EL panels use the rising edge of SHFCLK to clock in panel data, so the SHFCLK output from the 65540 / 545 must be inverted prior to driving the panel

Panel Timing - Monochrome 16-Gray-Level EL / Plasma 8-Bit Interface

Panel Output Timing - 640 x 480 Monochrome DD 8-Bit (1 Bit / Pixel, 8 Pixels / Shift Clock)



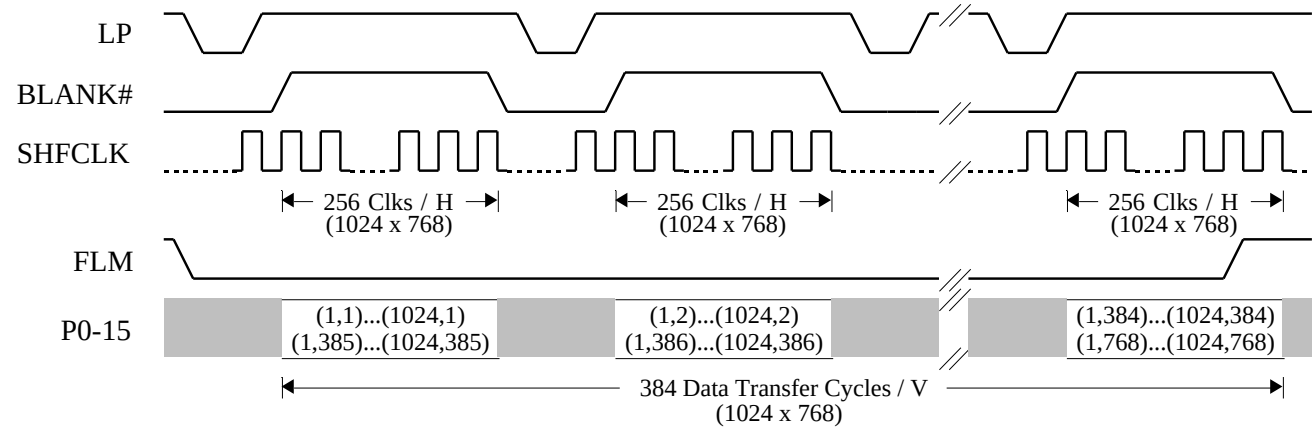
Panel Output Pixel Order - 640 x 480



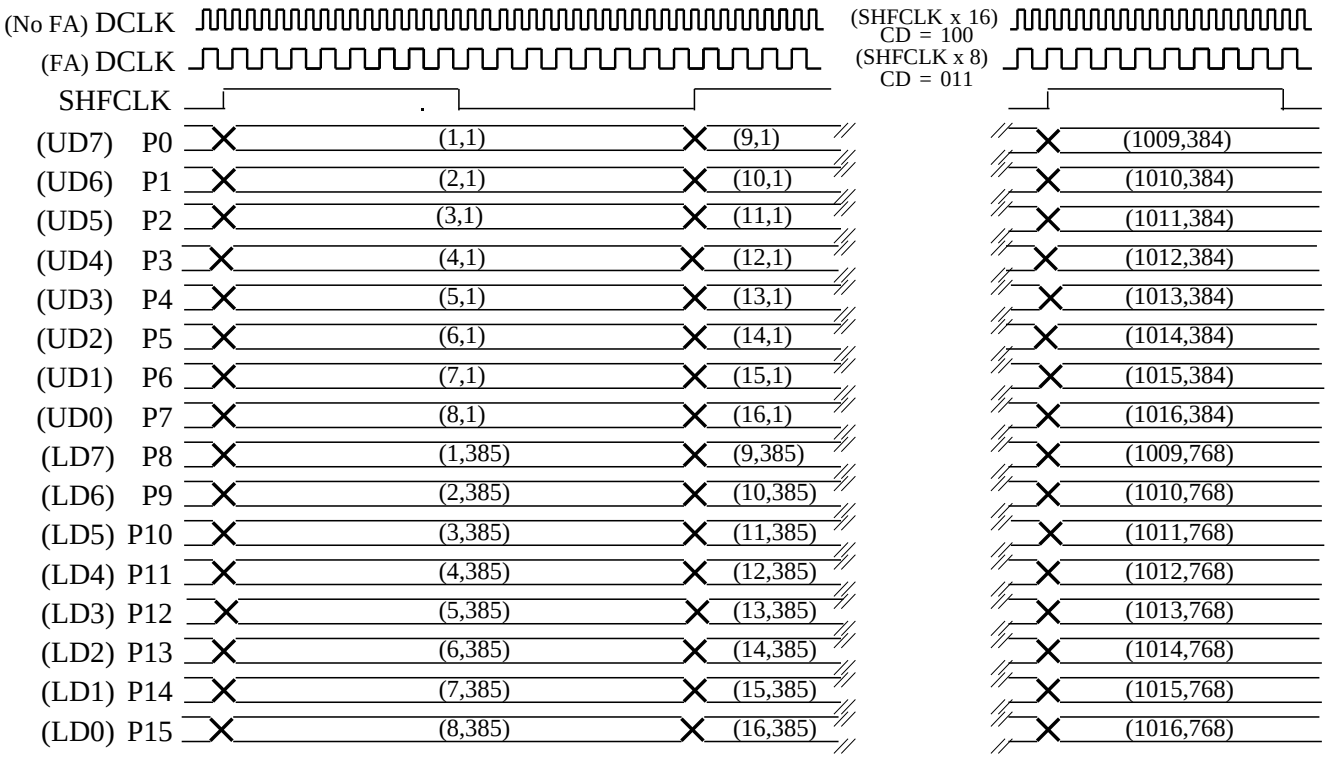
FA = Frame Accelerator (Imbedded or External)

Panel Timing - Monochrome LCD DD 8-Bit Interface

Panel Output Timing - 1024 x 768 Monochrome DD 16-Bit (1 Bit / Pixel, 16 Pixels / Shift Clock)

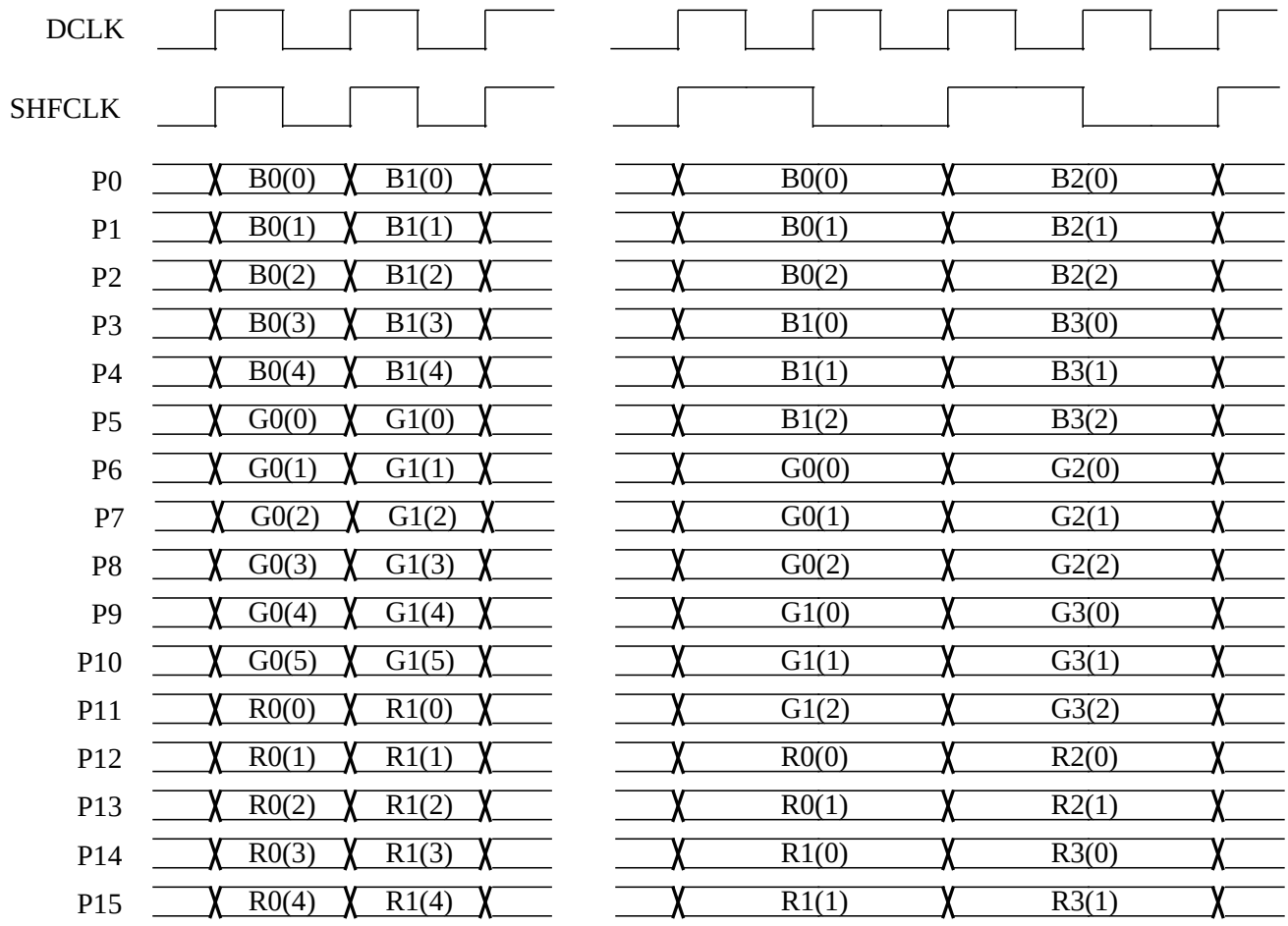


Pixel Output Pixel Order - 1024 x 768



FA = Frame Accelerator (Embedded or External)

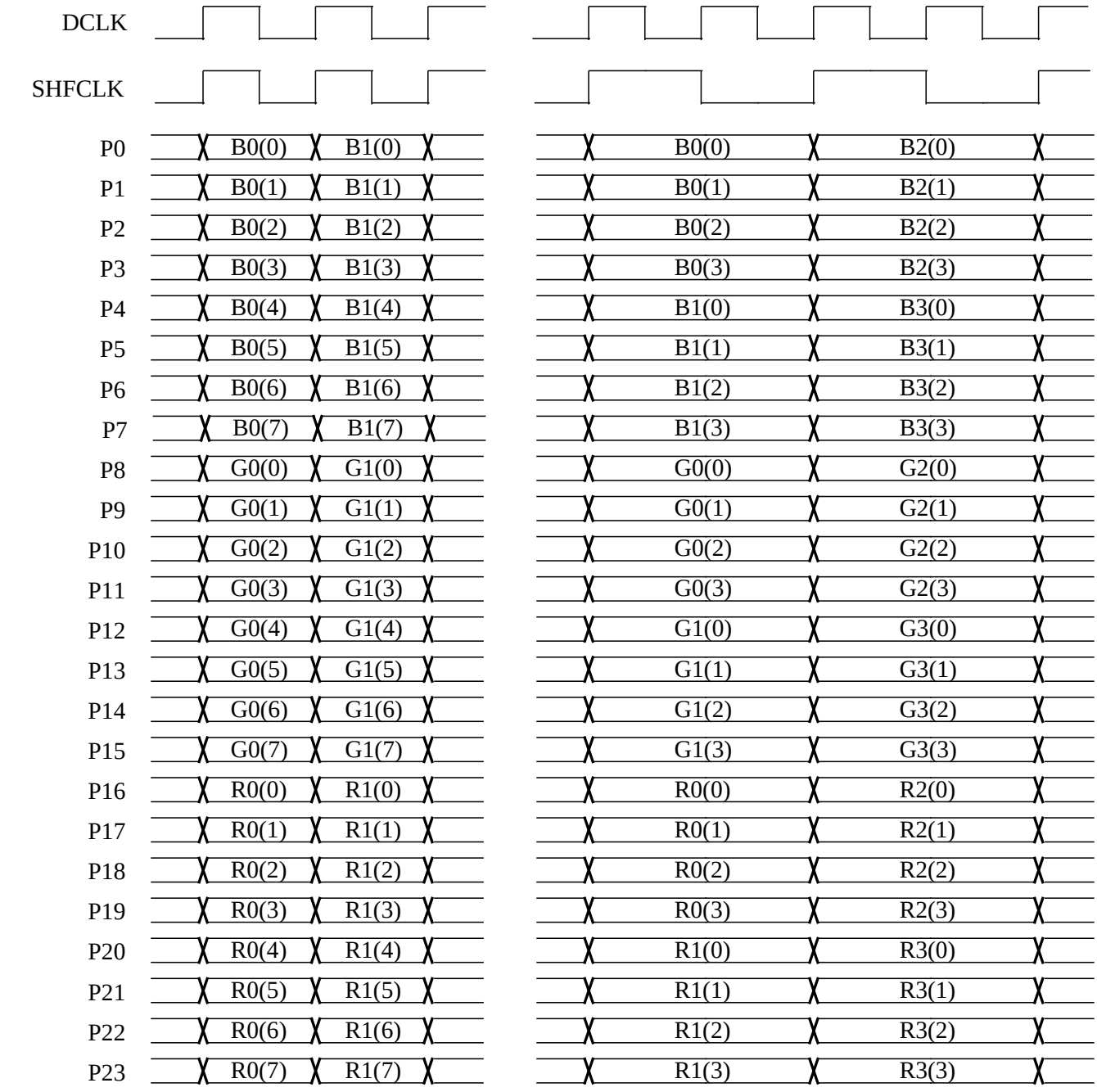
Panel Timing - Monochrome LCD DD 16-Bit Interface



CD:	000 (1 Pixel / Clock)	001 (2 Pixels / Clock)
FRC:	10 (2 Frame)	10 (2-Frame)
Bits / Pixel:	110 (6 bits/pixel)	011 (3 bits/pixel)
Pixel Format:	5-6-5 RGB	2-3-3 RGB
Data Width:	16-Bit †	16-Bit †

† Panels with 9 or 12-bit data interfaces would use this setting and only connect to the msbs of each color

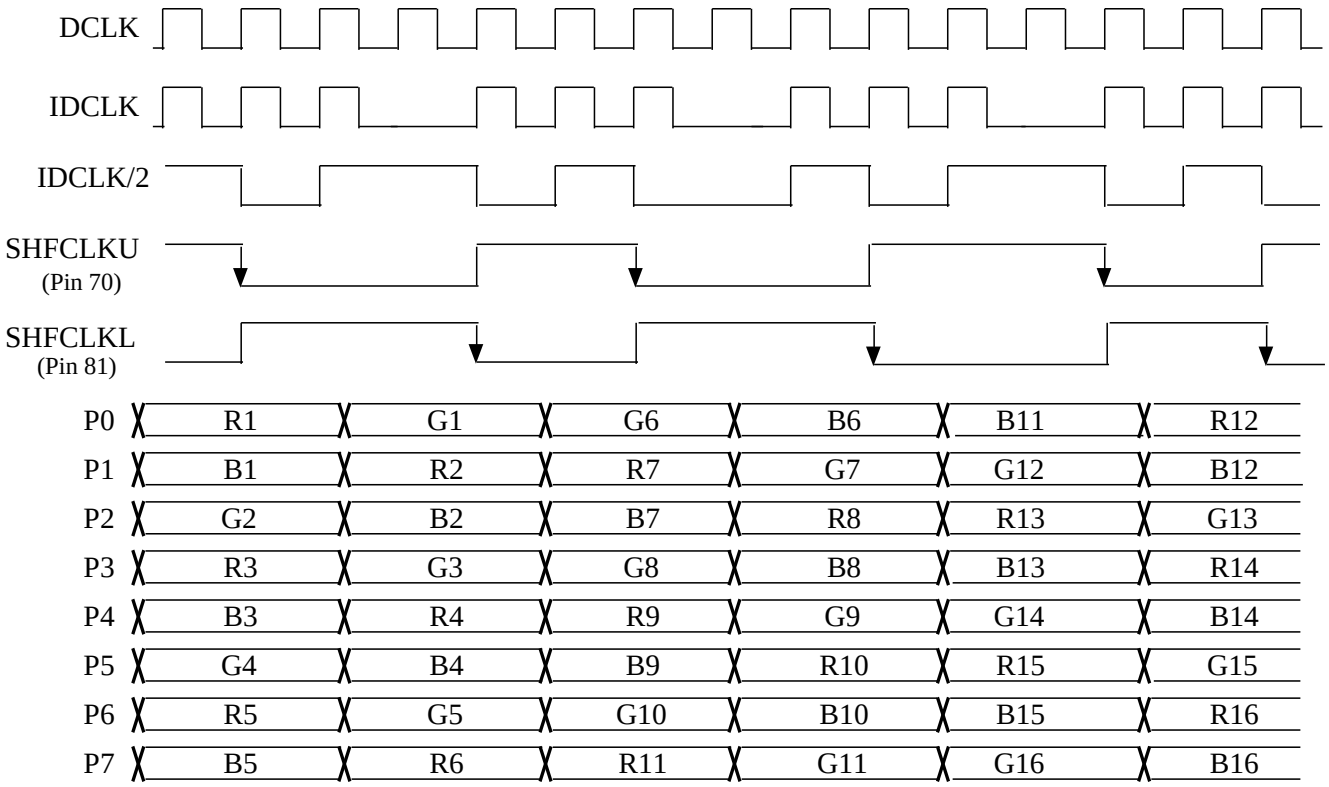
Panel Timing - Color LCD TFT 9 / 12 / 16-Bit Interface



CD:	000 (1 Pixel / Clock)	001 (2 Pixels / Clock)
FRC:	00 (no FRC)	10 (2-Frame)
Bits / Pixel:	111(8 bits/pixel)	100/101 (4 or 5 bits/pixel)
Pixel Format:	8-8-8 RGB	4-4-4 RGB
Data Width:	24-Bit †	24-Bit †

† Panels with 18-bit data interfaces would use this setting and only connect to the msbs of each color

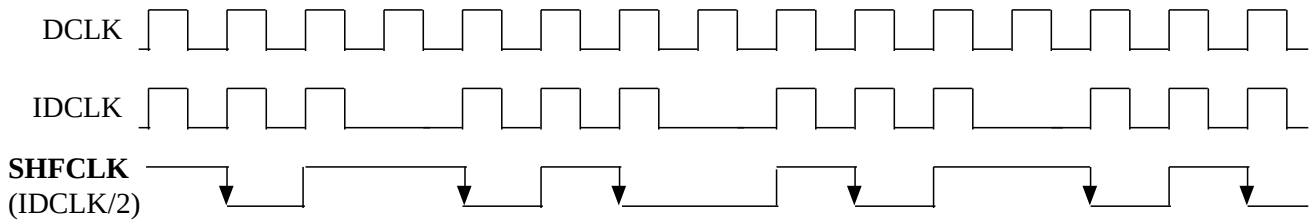
Panel Timing - Color LCD TFT 18 / 24-Bit Interface



PT:	00 (SS Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	11 (Extended 4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Disabled / Disabled

16 Pixels are transferred every 16 dot clocks (6 shift clock edges)

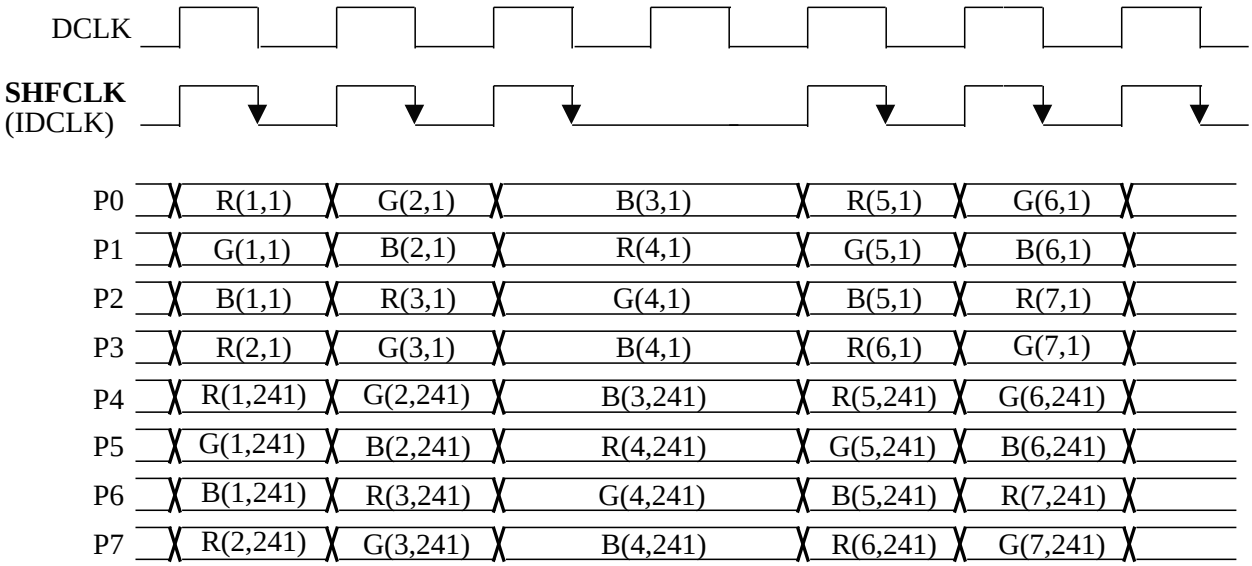
Panel Timing - Color LCD STN 8-Bit (Extended 4-Bit Pack) Interface



P0	R1	G6	B11	R17	G22	B27
P1	G1	B6	R12	G17	B22	R28
P2	B1	R7	G12	B17	R23	G28
P3	R2	G7	B12	R18	G23	B28
P4	G2	B7	R13	G18	B23	R29
P5	B2	R8	G13	B18	R24	G29
P6	R3	G8	B13	R19	G24	B29
P7	G3	B8	R14	G19	B24	R30
P8	B3	R9	G14	B19	R25	G30
P9	R4	G9	B14	R20	G25	B30
P10	G4	B9	R15	G20	B25	R31
P11	B4	R10	G15	B20	R26	G31
P12	R5	G10	B15	R21	G26	B31
P13	G5	B10	R16	G21	B26	R32
P14	B5	R11	G16	B21	R27	G32
P15	R6	G11	B16	R22	G27	B32

PT:	00 (SS Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Disabled / Disabled

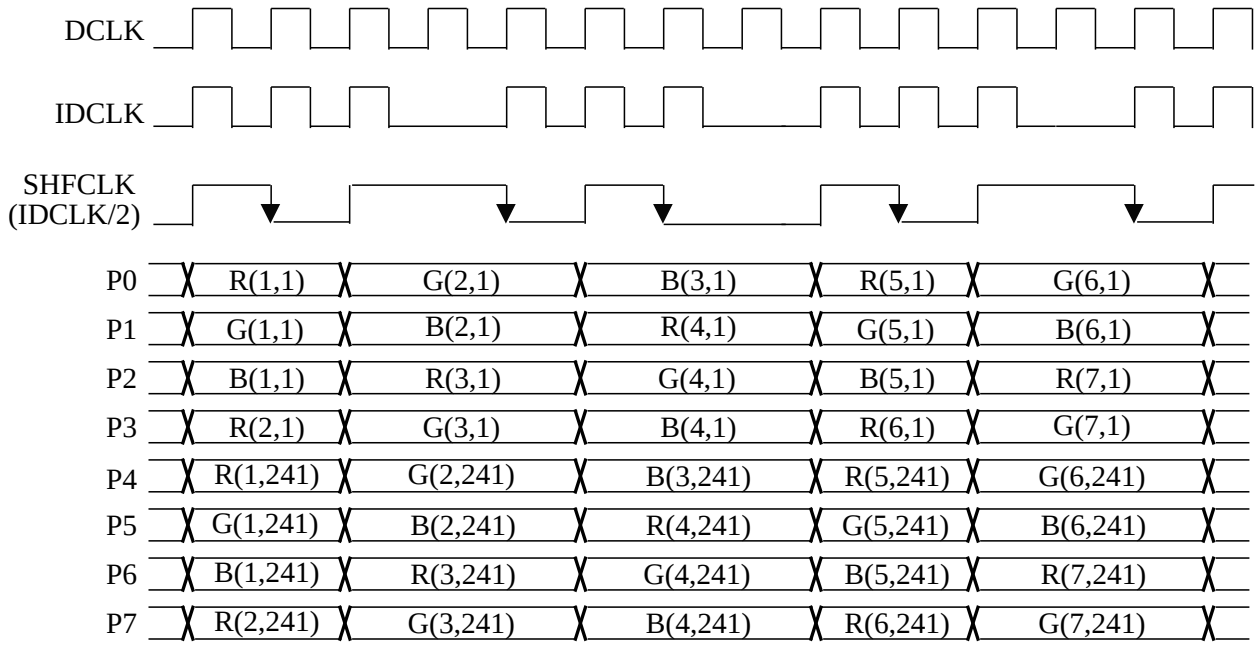
Panel Pixel Timing - Color LCD STN 16-Bit (4-Bit Pack) Interface



PT:	11 (DD Panel)
CD:	000 (2-2/3 Pixels / Clock)
FRC:	01 (16-Frame)
Bits / Pixel:	100 (4 bits/pixel)
Pixel Packing:	01 (4-Bit Pack)
Frame Buffer/Acceleration:	Enabled/Enabled

8 Pixels (4 each for the upper and lower panels) are transferred every 4 Dot Clocks (3 Shift Clock Edges)

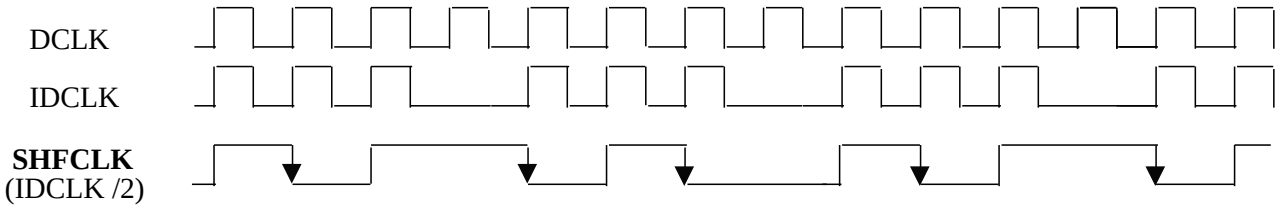
Panel Pixel Timing - Color LCD STN-DD 8-Bit (4-Bit Pack) Interface - With Frame Acceleration



PT:	11 (DD Panel)
CD:	001 (2-2/3 Pixels / Clock)
FRC:	01 (16-Frame)
Bits / Pixel:	100 (4 bits/pixel)
Pixel Packing:	01 (4-Bit Pack)
Frame Buffer/Acceleration:	Enabled/Disabled

8 Pixels (4 each for the upper and lower panels) are transferred every 8 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 8-Bit (4-Bit Pack) Interface - Without Frame Acceleration

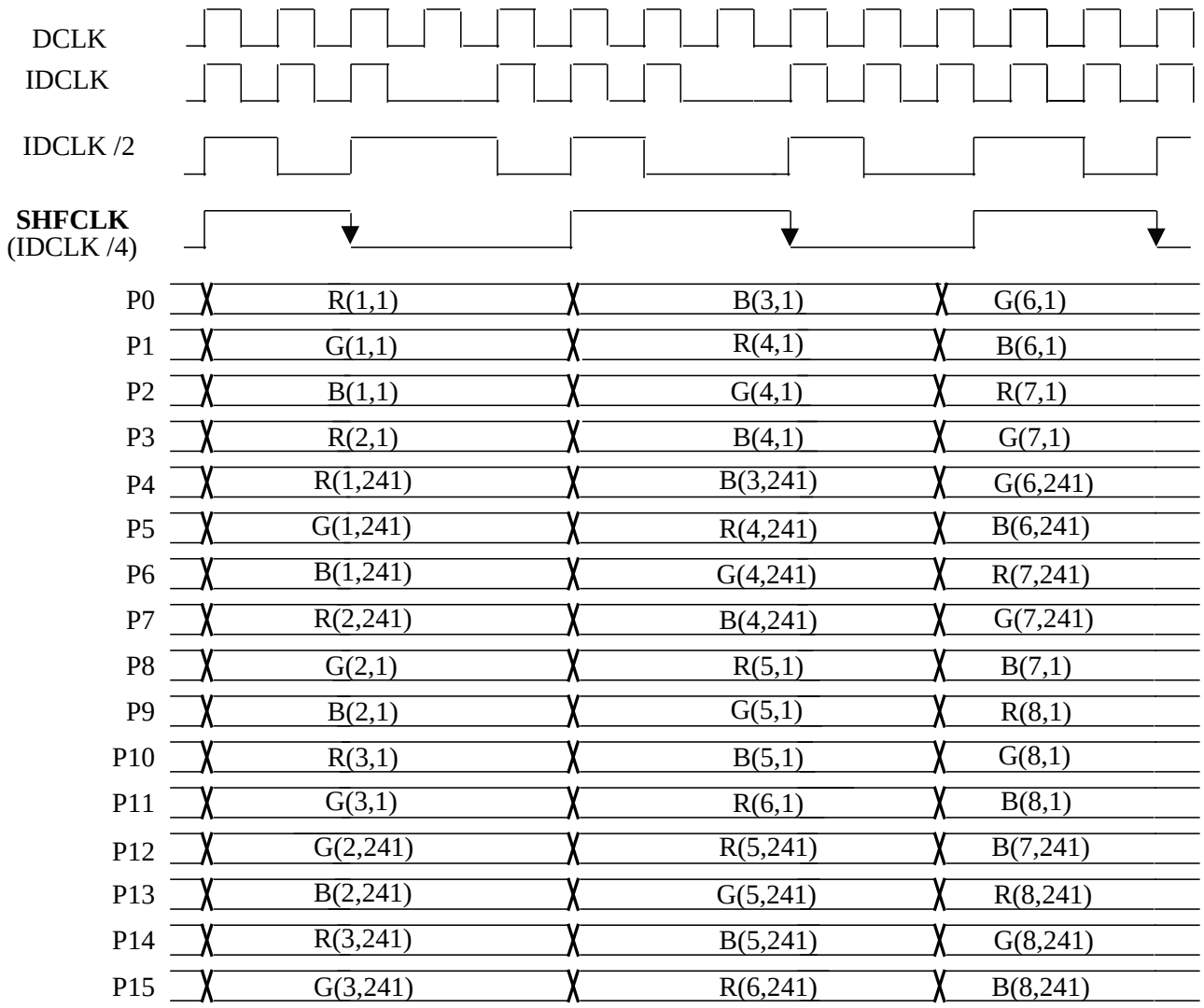


P0	R(1,1)	B(3,1)	G(6,1)	R(9,1)	B(11,1)
P1	G(1,1)	R(4,1)	B(6,1)	G(9,1)	R(12,1)
P2	B(1,1)	G(4,1)	R(7,1)	B(9,1)	G(12,1)
P3	R(2,1)	B(4,1)	G(7,1)	R(10,1)	B(12,1)
P4	R(1,241)	B(3,241)	G(6,241)	R(9,241)	B(11,241)
P5	G(1,241)	R(4,241)	B(6,241)	G(9,241)	R(12,241)
P6	B(1,241)	G(4,241)	R(7,241)	B(9,241)	G(12,241)
P7	R(2,241)	B(4,241)	G(7,241)	R(10,241)	B(12,241)
P8	G(2,1)	R(5,1)	B(7,1)	G(10,1)	R(13,1)
P9	B(2,1)	G(5,1)	R(8,1)	B(10,1)	G(13,1)
P10	R(3,1)	B(5,1)	G(8,1)	R(11,1)	B(13,1)
P11	G(3,1)	R(6,1)	B(8,1)	G(11,1)	R(14,1)
P12	G(2,241)	R(5,241)	B(7,241)	G(10,241)	R(13,241)
P13	B(2,241)	G(5,241)	R(8,241)	B(10,241)	G(13,241)
P14	R(3,241)	B(5,241)	G(8,241)	R(11,241)	B(13,241)
P15	G(3,241)	R(6,241)	B(8,241)	G(11,241)	R(14,241)

PT:	11 (DD Panel)
CD:	001 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer / Acceleration:	Enabled / Enabled

16 Pixels (8 each for the upper and lower panels) are transferred every 8 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 16-Bit (4-Bit Pack) Interface - With Frame Acceleration



PT:	11 (DD Panel)
CD:	010 (5-1/3 Pixels / Clock)
FRC:	01 (16-Frame)
Pixel Packing:	01 (4-Bit Pack)
Bits / Pixel:	100 (4 bits / pixel)
Frame Buffer/Acceleration:	Enabled/Disabled

16 Pixels (8 each for the upper and lower panels) are transferred every 16 Dot Clocks (3 Shift Clock Edges)

Panel Pixel Timing - Color LCD STN-DD 16-Bit (4-Bit Pack) Interface - Without Frame Acceleration

Programming and Parameters

GENERAL PROGRAMMING HINTS

The values presented in this section make certain assumptions about the operating environment. The flat panel clock ('dot clock') is assumed to be generated by the internal clock synthesizer. The values programmed into the SmartMap™ control registers (XR61 and XR62) give a threshold of 3 with foreground and background shift of 3 but SmartMap™ is turned off. To enable it, set XR61 bit-0 = 1. The 65540 and 65545 provide programmability of the gray scaling algorithm by adjusting 'm' and 'n' polynomial values in extended register 6E.

The horizontal parameter values presented here are the minimum required for each panel type. For high resolution panels, these parameters may be changed to suit the panel size. The horizontal values equal the number of characters clocks output per line. In dual drive panels this value includes both panels. Therefore, the horizontal values are double those expected.

Due to pipelining of the horizontal counters, certain sync or blank values may result in no display. Generally, the horizontal blank start must equal the display end and the blank end must equal the horizontal total. The horizontal sync start and end values have a wide range of acceptable values. The 65540 / 545 also has the versatility to program an LP delay to aid in interfacing to panels with a wide variety of timing requirements.

In order to program the 65540 / 545 for simultaneous display, two FLM signals are required. The first shorter FLM will match the normal FLM frequency as the data is displayed on the first half of the CRT display data. The second FLM will be longer to allow for the CRT blank time. The FLM delay is programmed in XR2C and should be equal to the CRT blank time — FLM front porch — FLM width.

For flat panel types and sizes not presented here, start with the parameters for a panel that most closely resembles the target panel. Adjust the flat panel configuration registers as needed and adjust the horizontal and vertical parameters as needed. Adaption to a non-standard panel is usually a trial and error process.

These parameters are recommended by Chips and Technologies, Inc. for the 65540 / 545. They have been tested on several different flat panel displays. Customers should feel free to test other register values to improve the screen appearance or to customize the 65540 / 545 for other flat panel displays.

EXTENSION REGISTER VALUES

The 65540 / 545 controller can be programmed for a wide variety of flat panels, compensation techniques and backwards compatibility. The following pages provide the following 65540 / 545 Extension Register Value tables:

Table	Extension Registers	Display Type Description	Panels
#1	Minimum	Parameters for Initial Boot (Analog CRT VGA Mode)	
#2	Additional	Parameters for Emulation Modes	
#3	Additional	640x480 Monochrome LCD-DD (Panel Mode Only)	Epson EG-9005F-LS Citizen G6481L-FF Sharp LM64P80 Sanyo LCM-6494-24NTK Hitachi LMG5364XUFC
#4	Additional	640x480 Monochrome LCD-DD (Simultaneous Mode Display)	
#5	Additional	640x480 Color TFT LCD (Panel Mode Only)	Hitachi TX26D02VC2AA Sharp LQ9D011 Toshiba LTM-09C015-1
#6	Additional	640x480 Color TFT LCD (Simultaneous Mode Display)	
#7	Additional	640x480 Color STN-SS LCD - 4-Bit Pack (Panel Mode & Simultaneous Mode Display)	Sanyo LM-CK53-22NEZ Sanyo LCM5327-24NAK Sanyo LCM5330
#8	Additional	640x480 Color STN-SS LCD - Extended 4-Bit Pack	Sharp LM64C031
#9	Additional	640x480 Color STN-DD LCD - 16-Bit Interface (Panel & Simultaneous Mode Display)	Sharp LM64C08P Sanyo LCM5331-22NTK Hitachi LMG9721XUFC Toshiba TLX-8062S-C3X Optrex DMF-50351NC-FW
#10	Additional	640x480 16 Internal Gray Scale Plasma	Matsushita S804
#11	Additional	640x480 16 Internal Gray Scale EL	Sharp LJ64ZU50

Table #1 specifies the minimum Extension Register values required for the 65540 / 545 to boot to VGA mode on an analog CRT monitor.

Table #2 specifies the additional Extension Register values required for emulation of EGA, CGA, MDA and Hercules backwards compatibility modes. The registers in Table #2 should be used in conjunction with the registers specified in Table #1. For registers listed in both tables, use the values in Table #2 (shown in bold text).

Tables #3-11 specify the additional Extension Register values required to support various panels. The registers in Tables #3-11 should be used in conjunction with the registers specified in Table #1 (and optionally Table #2). For registers listed in more than one table, use the values in Tables #3-11 (shown in bold text).

Table #1 - Parameters for Initial Boot

Initial Boot-Up Extension Register Values for VGA Display on an Analog CRT Monitor

Register	Value (in Hex)	Register	Comments
XR02	01	CPU Interface Control 1	
XR04	A1	Memory Control 1	Note 1
XR05	00	Memory Control 2	
XR06	00	Palette Control	
XR08	00	Linear Addressing Base	
XR0B	00	CPU Paging	
XR0C	00	Start Address Top	
XR0D	00	Auxiliary Offset	
XR0E	80	Text Mode Control	
XR0F	10	Software Flags 0	Note 2
XR10	00	Single/Low Map	
XR11	00	High Map	
XR14	00	Emulation Mode	
XR15	00	Write Protect	
XR16	00	Vertical Overflow	
XR17	00	Horizontal Overflow	
XR1E	00	Alternate Offset	
XR1F	00	Virtual EGA Switch	
XR24	12	Alternate Max Scanline	
XR25	59	Horizontal Virtual Panel Size	
XR28	80	Video Interface	
XR29	4C	Half Line Compare	
XR2B	00	Software Flags 1	Note 2
XR30	03	Clock Divide Control	(Initialize Memory Clock)
XR31	6B	Clock M-Divisor	(Initialize Memory Clock)
XR32	3C	Clock N-Divisor	(Initialize Memory Clock)
XR33	20	Clock Control	(Initialize Memory Clock)
XR30	03	Clock Divide Control	(Initialize Clock 2)
XR31	4E	Clock M-Divisor	(Initialize Clock 2)
XR32	59	Clock N-Divisor	(Initialize Clock 2)
XR33	00	Clock Control	(Initialize Clock 2)
XR44	10	Software Flags 2	Note 2
XR45	00	Software Flags 3	Note 2
XR51	63	Display Type	
XR52	40	Power Down Control	
XR53	00	Panel Format 3	
XR54	32	Panel Interface	
XR5F	06	Power Down Mode Refresh	
XR60	88	Blink Rate Control	
XR61	2E	SmartMap™ Control	
XR62	07	SmartMap™ Shift Parameter	
XR63	41	SmartMap™ Color Mapping Control	
XR70	80	Setup / Disable Control	
XR72	24	External Device I/O	

Note: 1) Memory Control Register 1 is automatically re-programmed with the proper display memory configuration by the BIOS
2) The Software Flag Registers are used by the BIOS and should not be re-programmed

Table #2 - Parameters for Emulation Modes

Extension Register Values for CRT-Only, Panel-Only, & Simultaneous CRT / Panel Display

Register	Value (in Hex)	Register	Comments
XR14	**00**	**Emulation Mode**	**EGA Emulation**
XR15	**18**	**Write Protect**	**EGA Emulation**

Register	Value (in Hex)	Register	Comments
XR14	**01**	**Emulation Mode**	**CGA Emulation**
XR15	**0D**	**Write Protect**	**CGA Emulation**
XR18	27	Alternate Horizontal Display Enable End	CGA Emulation
XR19	2B	Alternate Horizontal Retrace Start	CGA Emulation
XR1A	A0	Alternate Horizontal Retrace End	CGA Emulation
XR1B	2D	Alternate Horizontal Total	CGA Emulation
XR1C	28	Alternate Horizontal Blanking Start	CGA Emulation
XR1D	10	Alternate Horizontal Blanking End	CGA Emulation
XR1E	**14**	**Alternate Offset**	**CGA Emulation**
XR7E	**30**	**CGA / Hercules Color Select**	**CGA Emulation**

Register	Value (in Hex)	Register	Comments
XR14	**52**	**Emulation Mode**	**MDA Emulation**
XR15	**0D**	**Write Protect**	**MDA Emulation**
XR7E	**0F**	**CGA / Hercules Color Select**	**MDA Emulation**

Register	Value (in Hex)	Register	Comments
XR0D	**02**	**Auxiliary Offset**	**Hercules Emulation**
XR14	**52**	**Emulation Mode**	**Hercules Emulation**
XR15	**0D**	**Write Protect**	**Hercules Emulation**
XR18	59	Alternate Horizontal Display Enable End	Hercules Emulation
XR19	60	Alternate Horizontal Retrace Start	Hercules Emulation
XR1A	8F	Alternate Horizontal Retrace End	Hercules Emulation
XR1B	6E	Alternate Horizontal Total	Hercules Emulation
XR1C	5C	Alternate Horizontal Blanking Start	Hercules Emulation
XR1D	31	Alternate Horizontal Blanking End	Hercules Emulation
XR1E	**16**	**Alternate Offset**	**Hercules Emulation**
XR7E	**0F**	**CGA / Hercules Color Select**	**Hercules Emulation**

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #3 - Parameters for 640x480 Monochrome LCD-DD Panels (Panel Mode Only)

Extension Register Values for Epson EG9005F-LS
Citizen G6481L-FF
Sharp LM64P80
Sanyo LCM-6494-24NTK
Hitachi LMG5364XUFC

Register	Value (in Hex)	Register	Comments
XR06	**02**	**Palette Control**	**Disable Internal DAC**
XR19	57	Alternate Horizontal Sync Start	
XR1A	19	Alternate Horizontal Sync End	
XR1B	59	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	
XR2D	50	LP Delay (CMPR enabled)	
XR2E	50	LP Delay (CMPR disabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	25	Panel Format 1	
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	3A	Panel Interface	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	E4	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	E0	Alternate Vertical Sync Start	
XR67	01	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	00	Programmable Output Drive	
XR6E	26	Polynomial FRC Control Register	Optimize for best display quality
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #4 - Parameters for 640x480 Monochrome LCD-DD Panels (Simultaneous Mode Display)

Extension Register Values for Epson EG9005F-LS
Citizen G6481L-FF
Sharp LM64P80
Sanyo LCM-6494-24NTK
Hitachi LMG5364XUFC

Register	Value (in Hex)	Register	Comments
XR19	55	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	21	FLM Delay	
XR2D	50	LP Delay (CMPR enabled)	
XR2E	50	LP Delay (CMPR disabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	25	Panel Format 1	
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	3A	Panel Interface	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0B	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	26	Polynomial FRC Control Register	Optimize For LCD
XR6F	1B	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #5 - Parameters for 640x480 Color TFT Panels (Panel Mode Only)

Extension Register Values for Hitachi TX26D02VC2AA
Sharp LQ9D011 (set to accommodate the DE signal)
Toshiba LTM-09C015-1

Register	Value (in Hex)	Register	Comments
XR06	**C2**	**Palette Control**	**Color Reduction**
XR19	56	Alternate Horizontal Sync Start	
XR1A	13	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	
XR2D	4F	LP Delay (CMPR enabled)	
XR2E	4F	LP Delay (CMPR disabled)	
XR2F	0F	LP Width	
XR4F	44	Panel Format 1	
XR50	02	Panel Format 2	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**FA**	**Panel Interface**	**Set to F9 for Toshiba color panels**
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M(ACDCLK) Control	
XR64	01	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	DF	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	BD	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #6 - Parameters for 640x480 Color TFT Panels (Simultaneous Mode Display)

Extension Register Values for Hitachi TX26D02VC2AA
Sharp LQ9D011 (set to accommodate the DE signal)
Toshiba LTM-09C015-1

Register	Value (in Hex)	Register	Comments
XR06	**C0**	**Palette Control**	**Color Reduction**
XR19	55	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	5F	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	00	FLM Delay	
XR2D	4F	LP Delay (CMPR enabled)	
XR2E	4F	LP Delay (CMPR disabled)	
XR2F	0F	LP Width	
XR4F	44	Panel Format 2	
XR50	02	Panel Format 1	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**FA**	**Panel Interface**	**Set to F9 for Toshiba color panels**
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0C	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	BD	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #7 - Parameters for 640x480 Color STN-SS Panels with 16-Bit Interface 4-Bit Pack (Panel & Simultaneous Mode Display)

Extension Register Values for Sanyo LM-CK53-22NEZ
Sanyo LCM5327-24NAK
Sanyo LCM5330

Register	Value (in Hex)	Register	Comments
XR06	**C2**	**Palette Control**	**C0 for Simultaneous Display**
XR19	56	Alternate Horizontal Sync Start	55 for Simultaneous Display
XR1A	19	Alternate Horizontal Sync End	00 for Simultaneous Display
XR1B	59	Alternate Horizontal Total	5F for Simultaneous Display
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	22 for Simultaneous Display
XR2D	5C	LP Delay (CMPR enabled)	62 for Simultaneous Display
XR2E	5C	LP Delay (CMPR disabled)	62 for Simultaneous Display
XR2F	5C	LP Width	60 for Simultaneous Display
XR4F	44	Panel Format 1	
XR50	25	Panel Format 2	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**1C**	**Panel Format 3**	
XR54	**3A**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR50	10	Panel Format 1	
XR5E	80	M (ACDCLK) Control	
XR64	E4	Alternate Vertical Total	0B for Simultaneous Display
XR65	07	Alternate Overflow	26 for Simultaneous Display
XR66	E1	Alternate Vertical Sync Start	EA for Simultaneous Display
XR67	02	Alternate Vertical Sync End	0C for Simultaneous Display
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	61	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #8 - Parameters for 640x480 Color STN-SS Panels with 8-Bit Interface (Extended 4-Bit Pack)

Extension Register Values for Sharp LM64C031

Register	Value (in Hex)	Register	Comments
XR06	**C2**	**Palette Control**	**C0 simultaneous mode**
XR19	56	Alternate Horizontal Sync Start	55 simultaneous mode
XR1A	00	Alternate Horizontal Sync End	
XR1B	59	Alternate Horizontal Total	5F simultaneous mode
XR1C	4F	Horizontal Panel Size	
XR2C	02	FLM Delay	2B simultaneous mode
XR2D	50	LP Delay (CMPR enabled)	
XR2E	50	LP Delay (CMPR disabled)	
XR2F	00	LP Width	
XR4F	44	Panel Format 2	
XR50	15	Panel Format 1	
XR51	**6C**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**3C**	**Panel Format 3**	
XR54	**3A**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	E8	Alternate Vertical Total	15 simultaneous mode
XR65	07	Alternate Overflow	26 simultaneous mode
XR66	E1	Alternate Vertical Sync Start	EA simultaneous mode
XR67	02	Alternate Vertical Sync End	0C simultaneous mode
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	36	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #9 - Parameters for 640x480 Color STN-DD Panels with 16-Bit Interface with Frame Acceleration (Panel & Simultaneous Mode Display)

Extension Register Values for Sharp LM64C08P
Sanyo LCM5331-22NTK
Hitachi LMG9721XUFC
Toshiba TLX-8062S-C3X
Optrex DMF-50351NC-FW

Register	Value (in Hex)	Register	Comments
XR06	**C2**	**Palette Control**	
XR19	57	Alternate Horizontal Sync Start	
XR1A	19	Alternate Horizontal Sync End	
XR1B	59	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	15	FLM Delay	22 for no frame acceleration
XR2D	50	LP Delay (CMPR enabled)	9E for no frame acceleration
XR2E	50	LP Delay (CMPR disabled)	
XR2F	00	LP Width	
XR4F	04	Panel Format 1	
XR50	25	Panel Format 2	35 for no frame acceleration
XR51	**67**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**1C**	**Panel Format 3**	
XR54	**3A**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	1F	Vertical Line Replication	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0B	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	EA	Alternate Vertical Sync Start	
XR67	0C	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	33	Polynomial FRC Control	Optimize for best display quality.
XR6F	1B	Frame Buffer Control	9F for external frame buffer with frame acceleration. 99 for external frame buffer without frame acceleration.

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table #10 - Parameters for 640x480 Plasma Panels with 16 Internal Gray Levels

Extension Register Values for Matsushita S804

Register	Value (in Hex)	Register	Comments
XR19	60	Alternate Horizontal Sync Start	
XR1A	00	Alternate Horizontal Sync End	
XR1B	60	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	04	FLM Delay	
XR2D	62	LP Delay (CMPR enabled)	
XR2E	6D	LP Delay (CMPR disabled)	
XR2F	08	LP Width	
XR4F	04	Panel Format 1	
XR50	17	Panel Format 2	
XR51	**C4**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**39**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	0D	Alternate Vertical Total	
XR65	26	Alternate Overflow	
XR66	E8	Alternate Vertical Sync Start	
XR67	0A	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	0D	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Table # 11 - Parameters for 640x480 EL Panels with 16 Internal Gray Levels

Extension Register Values for Sharp LJ64ZU50

Register	Value (in Hex)	Register	Comments
XR19	52	Alternate Horizontal Sync Start	
XR1A	15	Alternate Horizontal Sync End	
XR1B	54	Alternate Horizontal Total	
XR1C	4F	Horizontal Panel Size	
XR2C	0C	FLM Delay	
XR2D	4F	LP Delay (CMPR enabled)	
XR2E	4E	LP Delay (CMPR disabled)	
XR2F	81	LP Width	
XR4F	04	Panel Format 1	
XR50	17	Panel Format 2	
XR51	**44**	**Display Type**	
XR52	**41**	**Power Down Control**	
XR53	**0C**	**Panel Format 3**	
XR54	**F9**	**Panel Interface**	
XR55	E5	Horizontal Compensation	
XR56	00	Horizontal Centering	
XR57	1B	Vertical Compensation	
XR58	00	Vertical Centering	
XR59	84	Vertical Line Insertion	
XR5A	00	Vertical Line Replication	
XR5B	8F	Power Sequencing Delay	
XR5D	10	FP Diagnostic	
XR5E	80	M (ACDCLK) Control	
XR64	F0	Alternate Vertical Total	
XR65	07	Alternate Overflow	
XR66	E5	Alternate Vertical Sync Start	
XR67	05	Alternate Vertical Sync End	
XR68	DF	Vertical Panel Size	
XR6C	02	Programmable Output Drive	
XR6E	9D	Polynomial FRC Control	Optimize for best display quality
XR6F	00	Frame Buffer Control	

Note: 1) **Bold** text indicates registers with values different from those shown in Table #1
2) Non-bold text indicates additional registers (not included in Table #1)

Application Schematic Examples

This section includes schematic examples showing various 65540 / 65545 interfaces. The schematics are divided into into three main groups:

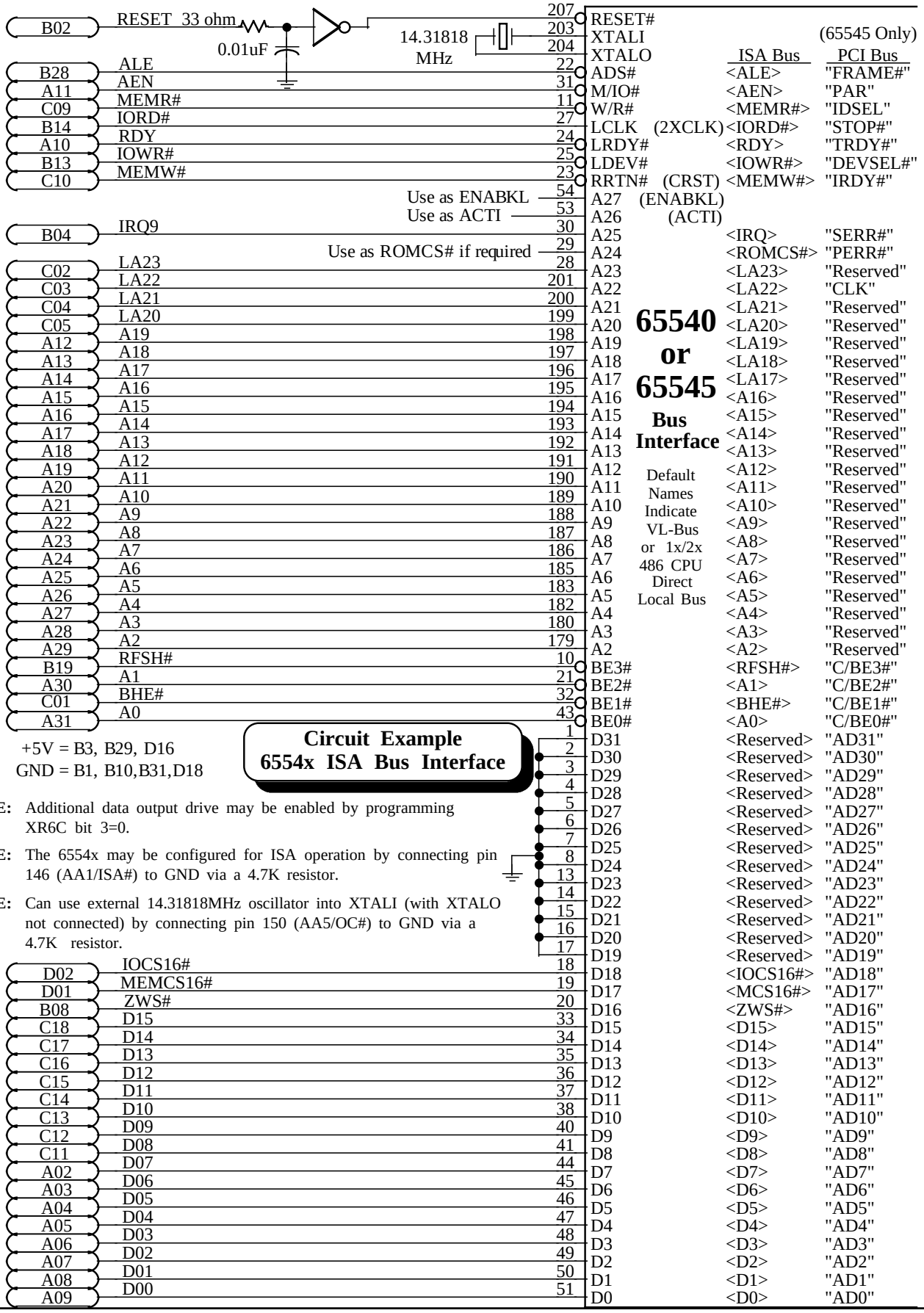
1) **System Bus Interface**
   - ISA (PC/AT) Bus (16-bit)
   - VL-Bus / 486 CPU-Direct Local Bus (1x Clock) (32-bit)
   - PCI Local Bus (32-bit)
2) **Display Memory Interface**
3) **CRT/Panel/Video Interface**

To design a system around the 65540 or 65545, one schematic page would be selected from each of the groups above.

Selection of a bus interface for the VGA controller is generally dictated by the type of bus and CPU available in the system. If performance is a concern, however, and a 386 or 486 CPU is being used, a local bus interface should be considered and linear addressing support should be implemented. Linear addressing improves performance in GUI environments such as Windows™ by allowing the software used to access display memory (typically the Windows Driver) to be more efficient. Clock connections are shown as part of the bus interface diagrams. A 14.31818 MHz reference crystal is shown, although if a clean source of 14.31818 MHz is available in the system, it may be input on XTALI and the crystal would then not be required.

Generally, 256Kx16 DRAMs would be used for display memory, although, if desired, the memory interface may be designed to use 256Kx4's instead. 256Kx16 DRAMs come in two types: one write enable (WE#) with two CAS# inputs (one for the high byte and one for the low byte) or one CAS# input with two write enables (one for the high byte and one for the low byte). Either variety of DRAM may be used (default is to the 2-CAS variety with a programming option in the 65540 / 545 to change the memory control outputs for compatibility with either type). CHIPS' BIOS is able to detect which type is connected and program the controller accordingly. It is also possible to lay out a PCB to allow either type to be used. The memory interface diagram also shows how to interface the 6554x to CHIPS' PC-Video products to provide live video overlay capability.

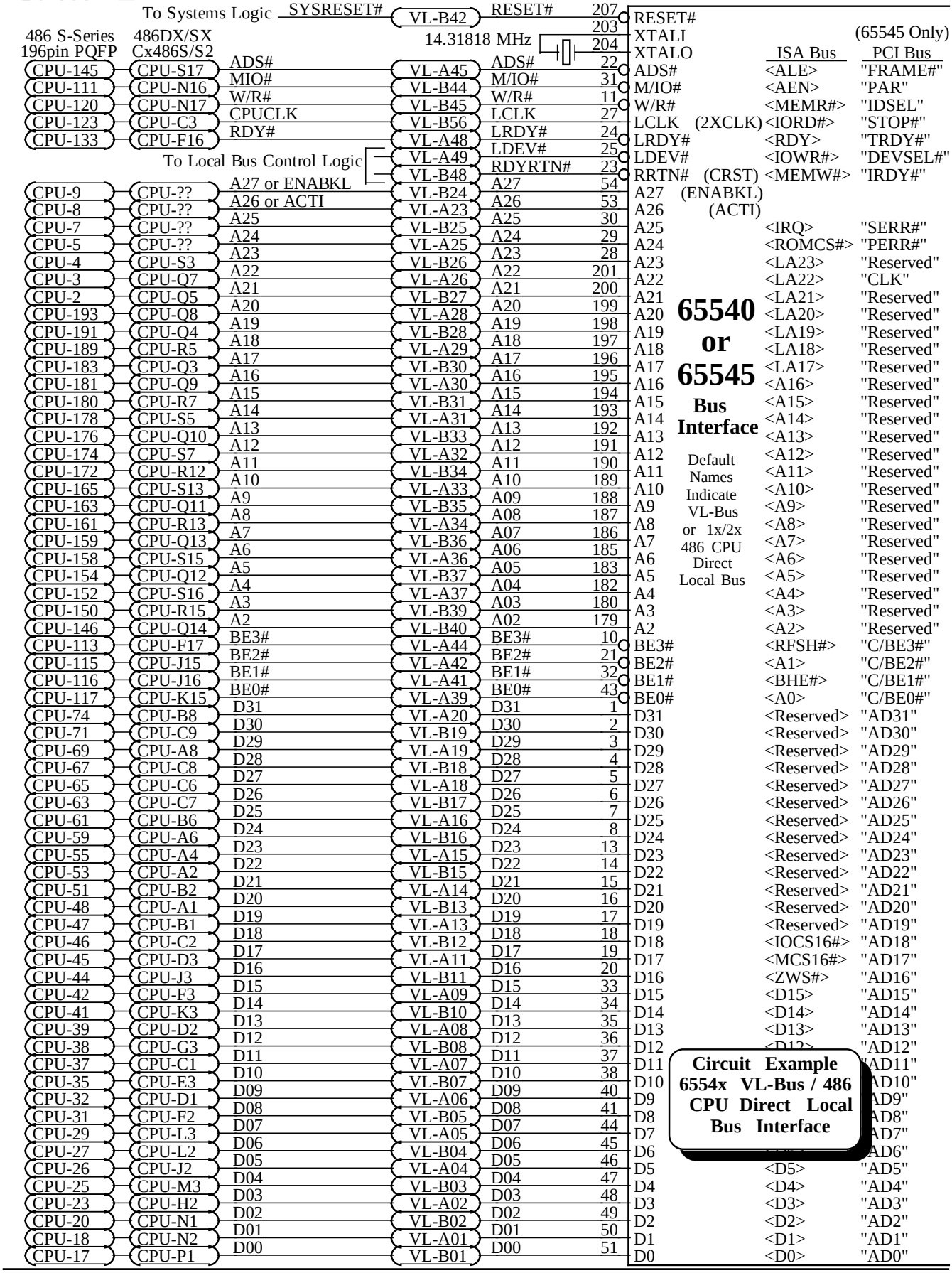
An interface diagram is included showing connections to a standard CRT display. Panel interfaces, however, are not as standardized (generally every panel interface is different). To show how to interface to a wide variety of commonly available panels, the interface diagram in this section shows the connections used on CHIPS' DK (Development Kit) Printed Circuit Board from the 6554x chip to connectors defined by CHIPS on that board. In the following section of this document, examples are included showing connections from those DK board connectors to a number of typical panels. The DK board connectors are used to simplify evaluation of the 6554x with various panels; a real system would not typically use the connectors shown, but would instead interface directly to the connector(s) used by the panel manufacturer.

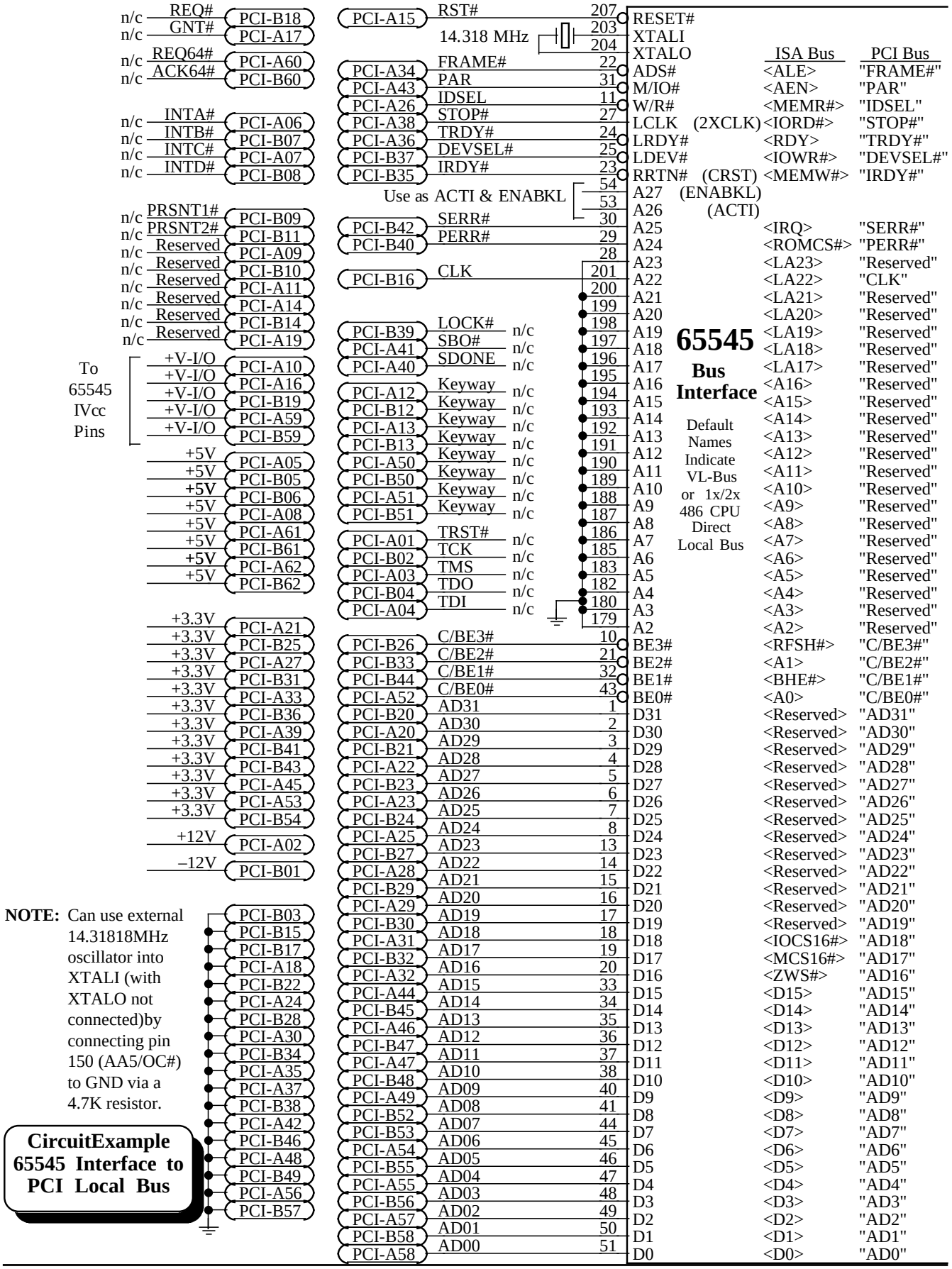


NOTE: Additional data output drive may be enabled by programming XR6C bit 3=0.

NOTE: The 6554x may be configured for ISA operation by connecting pin 146 (AA1/ISA#) to GND via a 4.7K resistor.

NOTE: Can use external 14.31818MHz oscillator into XTALI (with XTALO not connected) by connecting pin 150 (AA5/OC#) to GND via a 4.7K resistor.


To Systems Logic
SYSRESET#
VL-B42
RESET#
207
203
14.31818 MHz
204
486 S-Series 196pin PQFP
486DX/SX Cx486S/S2
CPU-145 CPU-S17 ADS#
CPU-111 CPU-N16 MIO#
CPU-120 CPU-N17 W/R#
CPU-123 CPU-C3 CPUCLK
CPU-133 CPU-F16 RDY#
VL-A45 ADS# 22
VL-B44 M/IO# 31
VL-B45 W/R# 11
VL-B56 LCLK 27
VL-A48 LRDY# 24
VL-A49 LDEV# 25
VL-B48 RDYRTN# 23
To Local Bus Control Logic
A27 or ENABKL
A26 or ACTI
CPU-9 CPU-?? A27 VL-B24 A26 54
CPU-8 CPU-?? A26 VL-A23 A25 53
CPU-7 CPU-?? A25 VL-B25 A24 30
CPU-5 CPU-?? A24 VL-A25 A23 29
CPU-4 CPU-S3 A23 VL-B26 A22 28
CPU-3 CPU-Q7 A22 VL-A26 A21 201
CPU-2 CPU-Q5 A21 VL-B27 A20 200
CPU-193 CPU-Q8 A20 VL-A28 A19 199
CPU-191 CPU-Q4 A19 VL-B28 A18 198
CPU-189 CPU-R5 A18 VL-A29 A17 197
CPU-183 CPU-Q3 A17 VL-B30 A16 196
CPU-181 CPU-Q9 A16 VL-A30 A15 195
CPU-180 CPU-R7 A15 VL-B31 A14 194
CPU-178 CPU-S5 A14 VL-A31 A13 193
CPU-176 CPU-Q10 A13 VL-B33 A12 192
CPU-174 CPU-S7 A12 VL-A32 A11 191
CPU-172 CPU-R12 A11 VL-B34 A10 190
CPU-165 CPU-S13 A10 VL-A33 A09 189
CPU-163 CPU-Q11 A9 VL-B35 A08 188
CPU-161 CPU-R13 A8 VL-A34 A07 187
CPU-159 CPU-Q13 A7 VL-B36 A06 186
CPU-158 CPU-S15 A6 VL-A36 A05 185
CPU-154 CPU-Q12 A5 VL-B37 A04 183
CPU-152 CPU-S16 A4 VL-A37 A03 182
CPU-150 CPU-R15 A3 VL-B39 A02 180
CPU-146 CPU-Q14 A2 VL-B40 BE3# 179
CPU-113 CPU-F17 BE3# VL-A44 BE2# 10
CPU-115 CPU-J15 BE2# VL-A42 BE1# 21
CPU-116 CPU-J16 BE1# VL-A41 BE0# 32
CPU-117 CPU-K15 BE0# VL-A39 D31 43
CPU-74 CPU-B8 D31 VL-A20 D30 1
CPU-71 CPU-C9 D30 VL-B19 D29 2
CPU-69 CPU-A8 D29 VL-A19 D28 3
CPU-67 CPU-C8 D28 VL-B18 D27 4
CPU-65 CPU-C6 D27 VL-A18 D26 5
CPU-63 CPU-C7 D26 VL-B17 D25 6
CPU-61 CPU-B6 D25 VL-A16 D24 7
CPU-59 CPU-A6 D24 VL-B16 D23 8
CPU-55 CPU-A4 D23 VL-A15 D22 13
CPU-53 CPU-A2 D22 VL-B15 D21 14
CPU-51 CPU-B2 D21 VL-A14 D20 15
CPU-48 CPU-A1 D20 VL-B13 D19 16
CPU-47 CPU-B1 D19 VL-A13 D18 17
CPU-46 CPU-C2 D18 VL-B12 D17 18
CPU-45 CPU-D3 D17 VL-A11 D16 19
CPU-44 CPU-J3 D16 VL-B11 D15 20
CPU-42 CPU-F3 D15 VL-A09 D14 33
CPU-41 CPU-K3 D14 VL-B10 D13 34
CPU-39 CPU-D2 D13 VL-A08 D12 35
CPU-38 CPU-G3 D12 VL-B08 D11 36
CPU-37 CPU-C1 D11 VL-A07 D10 37
CPU-35 CPU-E3 D10 VL-B07 D09 38
CPU-32 CPU-D1 D09 VL-A06 D08 40
CPU-31 CPU-F2 D08 VL-B05 D07 41
CPU-29 CPU-L3 D07 VL-A05 D06 44
CPU-27 CPU-L2 D06 VL-B04 D05 45
CPU-26 CPU-J2 D05 VL-A04 D04 46
CPU-25 CPU-M3 D04 VL-B03 D03 47
CPU-23 CPU-H2 D03 VL-A02 D02 48
CPU-20 CPU-N1 D02 VL-B02 D01 49
CPU-18 CPU-N2 D01 VL-A01 D00 50
CPU-17 CPU-P1 D00 VL-B01 51
RESET#
XTALI
XTALO
ADS#
M/IO#
W/R#
LCLK (2XCLK)
LRDY#
LDEV#
RRTN# (CRST)
A27 (ENABKL)
A26 (ACTI)
65540 or 65545 Bus Interface
Default Names Indicate VL-Bus or 1x/2x 486 CPU Direct Local Bus
ISA Bus
(65545 Only)
PCI Bus
<ALE> "FRAME#"
<AEN> "PAR"
<MEMR#> "IDSEL"
<IORD#> "STOP#"
<RDY> "TRDY#"
<IOWR#> "DEVSEL#"
<MEMW#> "IRDY#"
A25 <IRQ> "SERR#"
A24 <ROMCS#> "PERR#"
A23 <LA23> "Reserved"
A22 <LA22> "CLK"
A21 <LA21> "Reserved"
A20 <LA20> "Reserved"
A19 <LA19> "Reserved"
A18 <LA18> "Reserved"
A17 <LA17> "Reserved"
A16 <A16> "Reserved"
A15 <A15> "Reserved"
A14 <A14> "Reserved"
A13 <A13> "Reserved"
A12 <A12> "Reserved"
A11 <A11> "Reserved"
A10 <A10> "Reserved"
A9 <A9> "Reserved"
A8 <A8> "Reserved"
A7 <A7> "Reserved"
A6 <A6> "Reserved"
A5 <A5> "Reserved"
A4 <A4> "Reserved"
A3 <A3> "Reserved"
A2 <A2> "Reserved"
BE3# <RFSH#> "C/BE3#"
BE2# <A1> "C/BE2#"
BE1# <BHE#> "C/BE1#"
BE0# <A0> "C/BE0#"
D31 <Reserved> "AD31"
D30 <Reserved> "AD30"
D29 <Reserved> "AD29"
D28 <Reserved> "AD28"
D27 <Reserved> "AD27"
D26 <Reserved> "AD26"
D25 <Reserved> "AD25"
D24 <Reserved> "AD24"
D23 <Reserved> "AD23"
D22 <Reserved> "AD22"
D21 <Reserved> "AD21"
D20 <Reserved> "AD20"
D19 <Reserved> "AD19"
D18 <IOCS16#> "AD18"
D17 <MCS16#> "AD17"
D16 <ZWS#> "AD16"
D15 <D15> "AD15"
D14 <D14> "AD14"
D13 <D13> "AD13"
D12 <D12> "AD12"
D11 "AD11"
D10 "AD10"
D9 "AD9"
D8 "AD8"
D7 "AD7"
D6 "AD6"
D5 <D5> "AD5"
D4 <D4> "AD4"
D3 <D3> "AD3"
D2 <D2> "AD2"
D1 <D1> "AD1"
D0 <D0> "AD0"
Circuit Example
6554x VL-Bus / 486 CPU Direct Local Bus Interface


n/c REQ# PCI-B18
n/c GNT# PCI-A17
n/c REQ64# PCI-A60
n/c ACK64# PCI-B60
n/c INTA# PCI-A06
n/c INTB# PCI-B07
n/c INTC# PCI-A07
n/c INTD# PCI-B08
n/c PRSNT1# PCI-B09
n/c PRSNT2# PCI-B11
n/c Reserved PCI-A09
n/c Reserved PCI-B10
n/c Reserved PCI-A11
n/c Reserved PCI-A14
n/c Reserved PCI-B14
n/c Reserved PCI-A19
To 65545 IVcc Pins
+V-I/O PCI-A10
+V-I/O PCI-A16
+V-I/O PCI-B19
+V-I/O PCI-A59
+V-I/O PCI-B59
+5V PCI-A05
+5V PCI-B05
+5V PCI-B06
+5V PCI-A08
+5V PCI-A61
+5V PCI-B61
+5V PCI-A62
+5V PCI-B62
+3.3V PCI-A21
+3.3V PCI-B25
+3.3V PCI-A27
+3.3V PCI-B31
+3.3V PCI-A33
+3.3V PCI-B36
+3.3V PCI-A39
+3.3V PCI-B41
+3.3V PCI-B43
+3.3V PCI-A45
+3.3V PCI-A53
+3.3V PCI-B54
+12V PCI-A02
–12V PCI-B01
NOTE: Can use external 14.31818MHz oscillator into XTALI (with XTALO not connected)by connecting pin 150 (AA5/OC#) to GND via a 4.7K resistor.
CircuitExample 65545 Interface to PCI Local Bus
PCI-B03
PCI-B15
PCI-B17
PCI-A18
PCI-B22
PCI-A24
PCI-B28
PCI-A30
PCI-B34
PCI-A35
PCI-A37
PCI-B38
PCI-A42
PCI-B46
PCI-A48
PCI-B49
PCI-A56
PCI-B57
PCI-A15 RST# 207
14.318 MHz 203 204
PCI-A34 FRAME# 22
PCI-A43 PAR 31
PCI-A26 IDSEL 11
PCI-A38 STOP# 27
PCI-A36 TRDY# 24
PCI-B37 DEVSEL# 25
PCI-B35 IRDY# 23
Use as ACTI & ENABKL 54 53
PCI-B42 SERR# 30
PCI-B40 PERR# 29
28
PCI-B16 CLK 201
200
199
198
PCI-B39 LOCK# n/c
PCI-A41 SBO# n/c
PCI-A40 SDONE n/c
197
196
195
PCI-A12 Keyway n/c
PCI-B12 Keyway n/c
PCI-A13 Keyway n/c
PCI-B13 Keyway n/c
PCI-A50 Keyway n/c
PCI-B50 Keyway n/c
PCI-A51 Keyway n/c
PCI-B51 Keyway n/c
194
193
192
191
190
189
188
187
PCI-A01 TRST# n/c
PCI-B02 TCK n/c
PCI-A03 TMS n/c
PCI-B04 TDO n/c
PCI-A04 TDI n/c
186
185
183
182
180
179
PCI-B26 C/BE3# 10
PCI-B33 C/BE2# 21
PCI-B44 C/BE1# 32
PCI-A52 C/BE0# 43
PCI-B20 AD31 1
PCI-A20 AD30 2
PCI-B21 AD29 3
PCI-A22 AD28 4
PCI-B23 AD27 5
PCI-A23 AD26 6
PCI-B24 AD25 7
PCI-A25 AD24 8
PCI-B27 AD23 13
PCI-A28 AD22 14
PCI-B29 AD21 15
PCI-A29 AD20 16
PCI-B30 AD19 17
PCI-A31 AD18 18
PCI-B32 AD17 19
PCI-A32 AD16 20
PCI-A44 AD15 33
PCI-B45 AD14 34
PCI-A46 AD13 35
PCI-B47 AD12 36
PCI-A47 AD11 37
PCI-B48 AD10 38
PCI-A49 AD09 40
PCI-B52 AD08 41
PCI-B53 AD07 44
PCI-A54 AD06 45
PCI-B55 AD05 46
PCI-A55 AD04 47
PCI-B56 AD03 48
PCI-A57 AD02 49
PCI-B58 AD01 50
PCI-A58 AD00 51
65545 Bus Interface
Default Names Indicate VL-Bus or 1x/2x 486 CPU Direct Local Bus
RESET#
XTALI
XTALO
ADS#
M/IO#
W/R#
LCLK (2XCLK)
LRDY#
LDEV#
RRTN# (CRST)
A27 (ENABKL)
A26 (ACTI)
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
BE3#
BE2#
BE1#
BE0#
D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
ISA Bus
<ALE>
<AEN>
<MEMR#>
<IORD#>
<RDY>
<IOWR#>
<MEMW#>
<IRQ>
<ROMCS#>
<LA23>
<LA22>
<LA21>
<LA20>
<LA19>
<LA18>
<LA17>
<A16>
<A15>
<A14>
<A13>
<A12>
<A11>
<A10>
<A9>
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<A7>
<A6>
<A5>
<A4>
<A3>
<A2>
<RFSH#>
<A1>
<BHE#>
<A0>
<Reserved>
<IOCS16#>
<MCS16#>
<ZWS#>
PCI Bus
"FRAME#"
"PAR"
"IDSEL"
"STOP#"
"TRDY#"
"DEVSEL#"
"IRDY#"
"SERR#"
"PERR#"
"Reserved"
"CLK"
"C/BE3#"
"C/BE2#"
"C/BE1#"
"C/BE0#"
"AD31"
"AD30"
"AD29"
"AD28"
"AD27"
"AD26"
"AD25"
"AD24"
"AD23"
"AD22"
"AD21"
"AD20"
"AD19"
"AD18"
"AD17"
"AD16"
"AD15"
"AD14"
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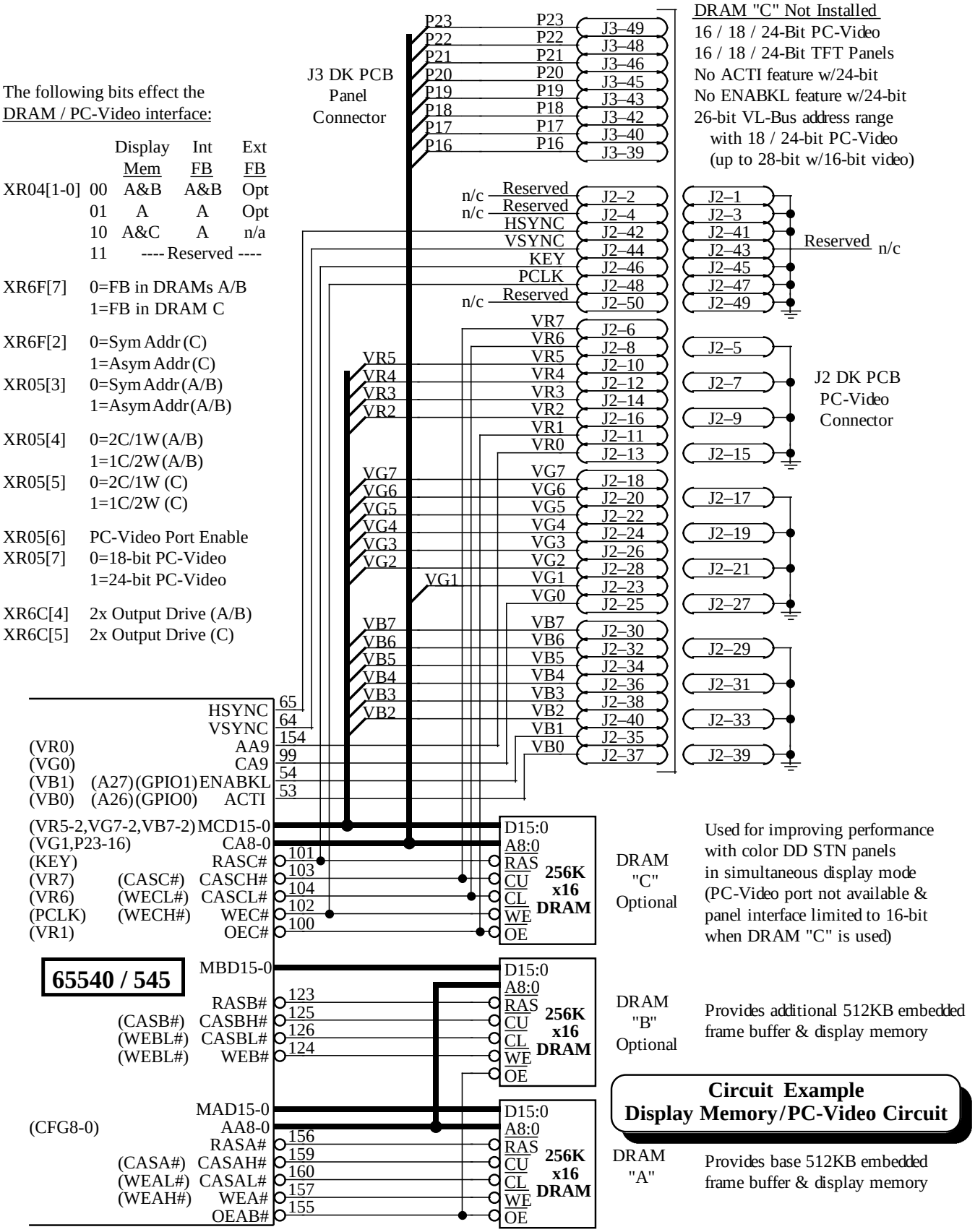
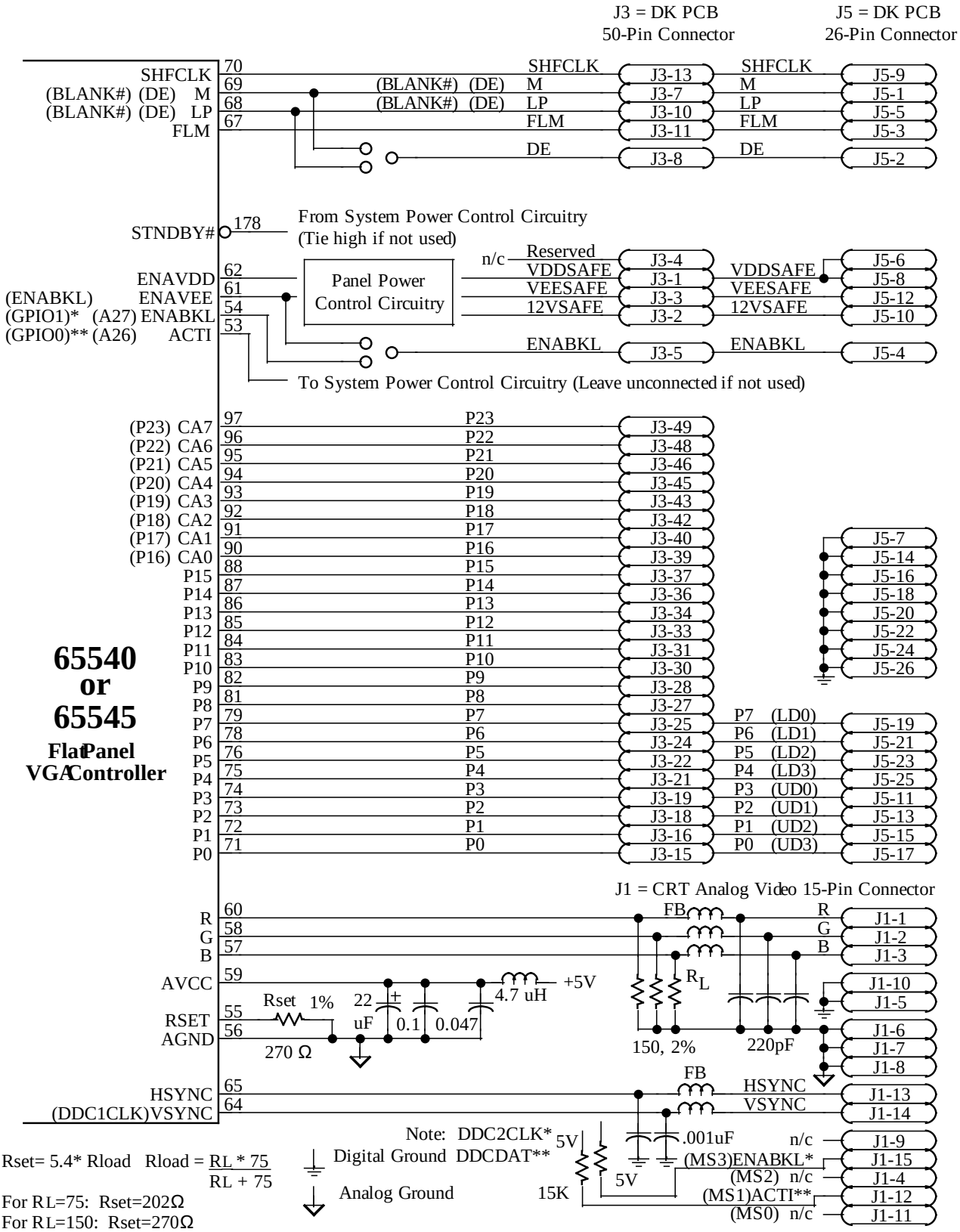
"AD12"
"AD11"
"AD10"
"AD9"
"AD8"
"AD7"
"AD6"
"AD5"
"AD4"
"AD3"
"AD2"
"AD1"
"AD0"


The following bits effect the DRAM / PC-Video interface:
Display Mem / Int FB / Ext FB
XR04[1-0] 00 A&B A&B Opt
01 A A Opt
10 A&C A n/a
11 ---- Reserved ----
XR6F[7] 0=FB in DRAMs A/B
1=FB in DRAM C
XR6F[2] 0=Sym Addr (C)
1=Asym Addr (C)
XR05[3] 0=Sym Addr (A/B)
1=Asym Addr (A/B)
XR05[4] 0=2C/1W (A/B)
1=1C/2W (A/B)
XR05[5] 0=2C/1W (C)
1=1C/2W (C)
XR05[6] PC-Video Port Enable
XR05[7] 0=18-bit PC-Video
1=24-bit PC-Video
XR6C[4] 2x Output Drive (A/B)
XR6C[5] 2x Output Drive (C)
J3 DK PCB Panel Connector
DRAM "C" Not Installed
16 / 18 / 24-Bit PC-Video
16 / 18 / 24-Bit TFT Panels
No ACTI feature w/24-bit
No ENABKL feature w/24-bit
26-bit VL-Bus address range with 18 / 24-bit PC-Video (up to 28-bit w/16-bit video)
J2 DK PCB PC-Video Connector
65540 / 545
Circuit Example
Display Memory/PC-Video Circuit
DRAM "C" Optional
DRAM "B" Optional
DRAM "A"
256K x16 DRAM
Used for improving performance with color DD STN panels in simultaneous display mode (PC-Video port not available & panel interface limited to 16-bit when DRAM "C" is used)
Provides additional 512KB embedded frame buffer & display memory
Provides base 512KB embedded frame buffer & display memory



65540/545 CRT/Panel Interface Circuit

Panel Interface Examples

This section includes schematic examples showing how to connect the 65540 / 545 to various flat panel displays.

Plasma/EL Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels	Page
1)	Matsushita	S804	640x480	Plasma	SS	8-bit	2 Pixels/Clk	16	217
2)	Sharp	LJ64ZU50	640x480	EL	SS	8-bit	2 Pixels/Clk	16	218

Monochrome LCD Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Gray Levels	Page
3)	Epson	EG-9005F-LS	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	219
4)	Citizen	G6481L-FF	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	220
5)	Sharp	LM64P80	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	221
6)	Sanyo	LCM-6494-24NTK	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	222
7)	Hitachi	LMG5364XUFC	640x480	LCD	DD	8-bit	8 Pixels/Clk	2	223
8)	Sanyo	LCM-5491-24NAK	1024x768	LCD	DD	16-bit	16 Pixels/Clk	2	224
9)	Epson	ECM-A9071	1024x768	LCD	DD	16-bit	16 Pixels/Clk	2	225

Active Color Panels

	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Colors	Page
10)	Hitachi	TM26D50VC2AA	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	226
11)	Sharp	LQ9D011	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	227
12)	Toshiba	LTM-09C015-1	640x480	TFT LCD	SS	9-bit	1 Pixel/Clk	512	228
13)	Sharp	LQ10D311	640x480	TFT LCD	SS	18-bit	1 Pixel/Clk	256K	229
14)	Sharp	LQ10DX01	1024x768	TFT LCD	SS	18-bit	2 Pixels/Clk	512	230

Passive Color Panels

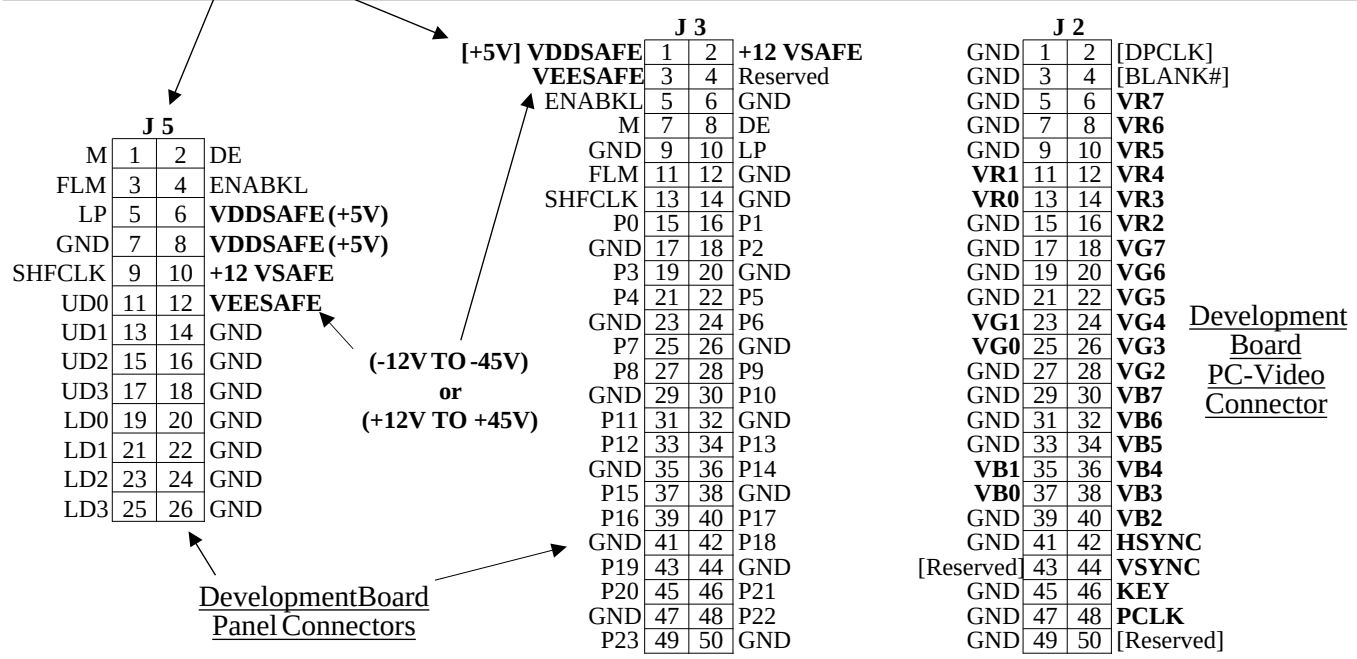
	Mfr	Part Number	Panel Resolution	Panel Technology	Panel Drive	Panel Interface	Panel Data Transfer	Panel Colors	Page
15)	Sanyo	LM-CK53-22NEZ	640x480	STN LCD	SS	16-bit	5-1/3 Pixels/Clk	8	231
16)	Sanyo	LCM5327-24NAK	640x480	STN LCD	SS	16-bit	5-1/3 Pixels/Clk	8	232
17)	Sharp	LM64C031	640x480	STN LCD	SS	8-bit	2-2/3 Pixels/Clk	8	233
18)	Kyocera	KCL6448	640x480	STN LCD	DD	8-bit	2-2/3 Pixels/Clk	8	234
19)	Hitachi	LMG9720XUFC	640x480	STN LCD	DD	8-bit	2-2/3 Pixels/Clk	8	235
20)	Sharp	LM64C08P	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	236
21)	Sanyo	LCM5331-22NTK	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	237
22)	Hitachi	LMG9721XUFC	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	238
23)	Toshiba	TLX-8062S-C3X	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	239
24)	Optrex	DMF-50351NC-FW	640x480	STN LCD	DD	16-bit	5-1/3 Pixels/Clk	8	240

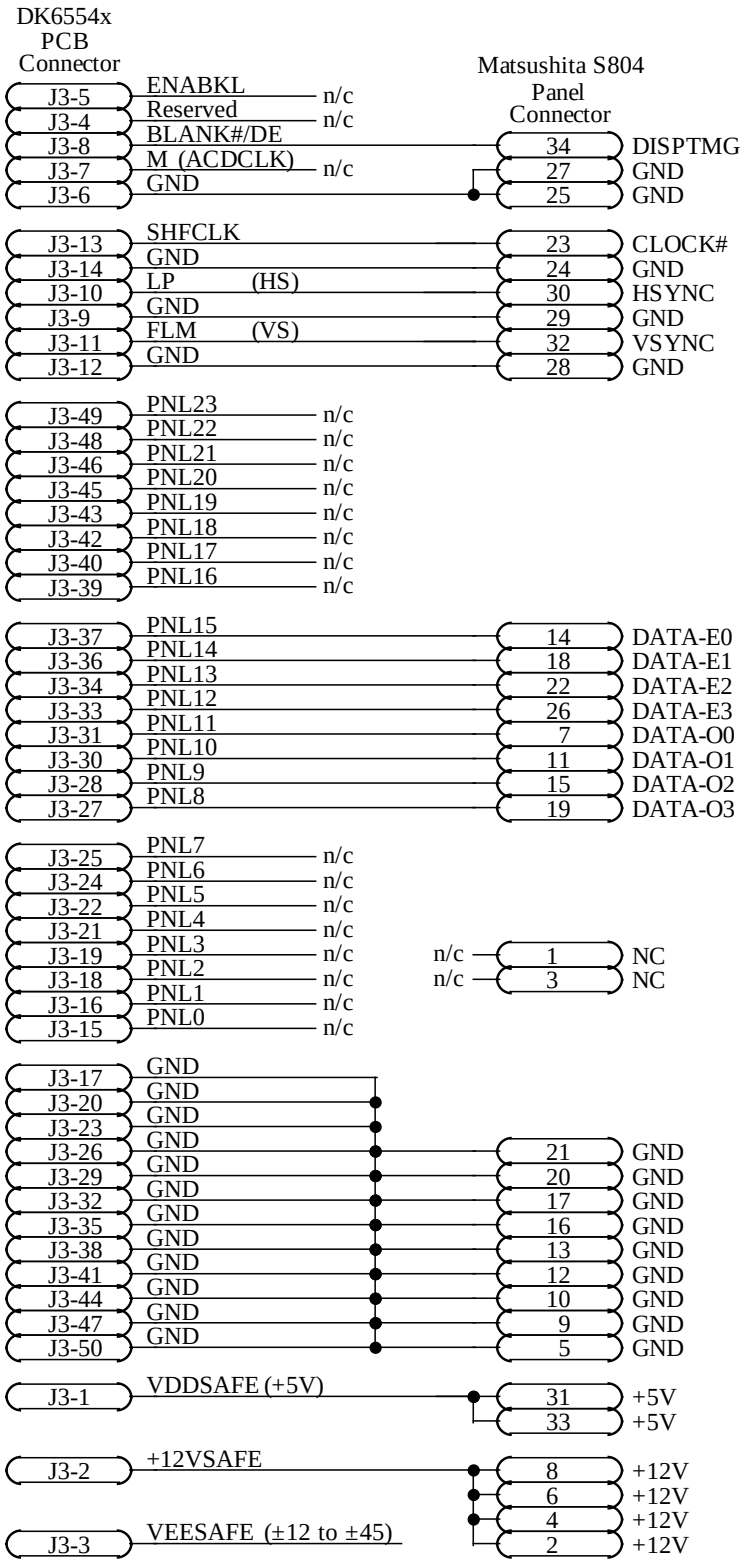
Glossary:

SS = Single Panel Single Scan
DD = Dual Panel Dual Scan
TFT = Thin Film Transistor ('Active Matrix')
STN = Super Twist Nematic ('Passive Matrix')

DEVELOPMENT KIT (DK) PRINTED CIRCUIT BOARD CONNECTOR SUMMARY

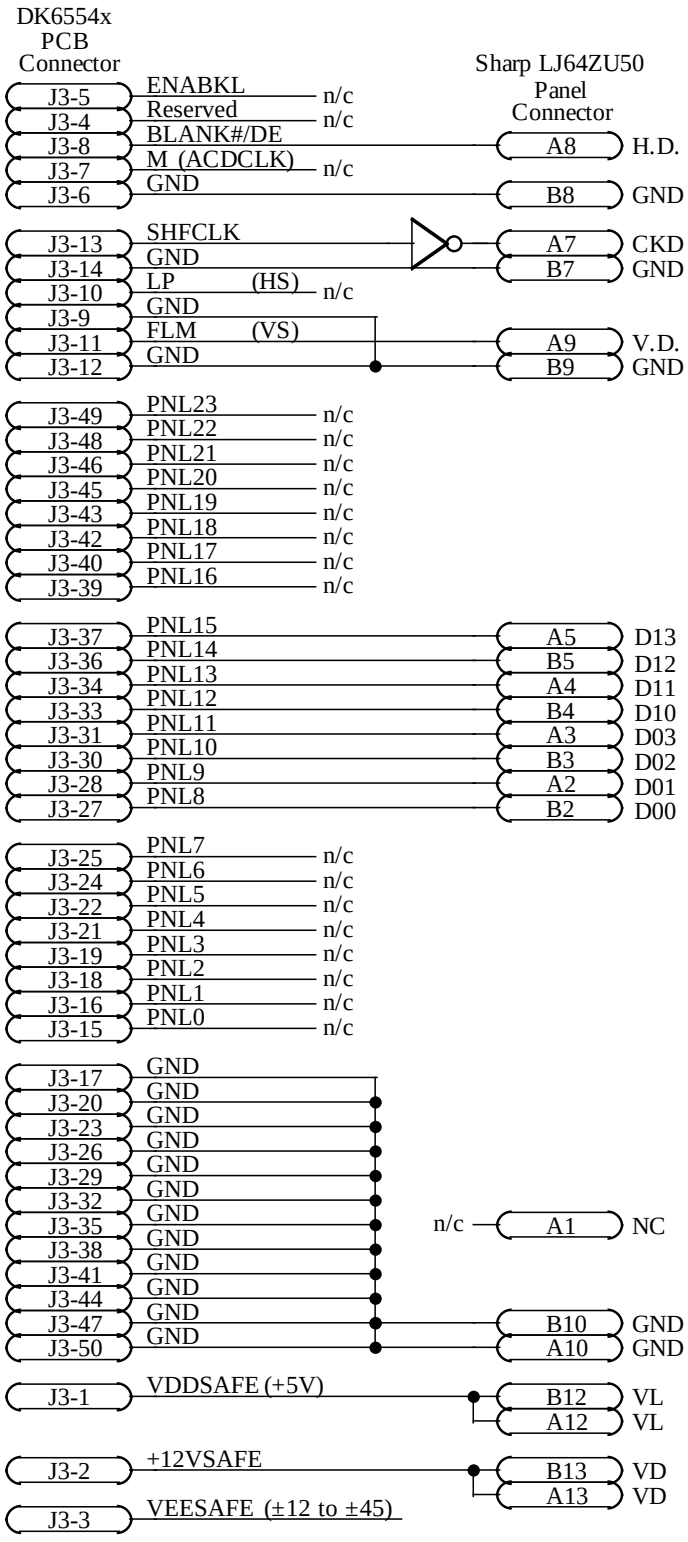
6554x Pin#	6554x Pin Name	DK6554x 26-Pin Connector	DK6554x 50-Pin Connector	Mono SS 8-bit	Mono DD 8-bit	Mono DD 16-bit	Color TFT 9/12/16-bit	Color TFT 18/24-bit	Color TFTHiRes 18/24-bit	Color STN 8-bit	Color STN 16-bit	Color STNDD 8-bit	Color STNDD 16-bit
	Pixels Transferred Per Shift Clock:	8	8	16	1	1	2	2-2/3	5-1/3	2-2/3	5-1/3		
71	P0	17	15	–	UD3	UD7	B0	B0	B00	R1...	R1...	UR1...	UR1...
72	P1	15	16	–	UD2	UD6	B1	B1	B01	B1...	G1...	UG1...	UG1...
73	P2	13	18	–	UD1	UD5	B2	B2	B02	G2...	B1...	UB1...	UB1...
74	P3	11	19	–	UD0	UD4	B3	B3	B03	R3...	R2...	UR2...	UR2...
75	P4	25	21	–	LD3	UD3	B4	B4	B10	B3...	G2...	LR1...	LR1...
76	P5	23	22	–	LD2	UD2	G0	B5	B11	G4...	B2...	LG1...	LG1...
78	P6	21	24	–	LD1	UD1	G1	B6	B12	R5...	R3...	LB1...	LB1...
79	P7	19	25	–	LD0	UD0	G2	B7	B13	B5...	G3...	LR2...	LR2...
81	P8	–	27	P0	–	LD7	G3	G0	G00	**SHFCLKU**	B3...	–	UG2...
82	P9	–	28	P1	–	LD6	G4	G1	G01	–	R4...	–	UB2...
83	P10	–	30	P2	–	LD5	G5	G2	G02	–	G4...	–	UR3...
84	P11	–	31	P3	–	LD4	R0	G3	G03	–	B4...	–	UG3...
85	P12	–	33	P4	–	LD3	R1	G4	G10	–	R5...	–	LG2...
86	P13	–	34	P5	–	LD2	R2	G5	G11	–	G5...	–	LB2...
87	P14	–	36	P6	–	LD1	R3	G6	G12	–	B5...	–	LR3...
88	P15	–	37	P7	–	LD0	R4	G7	G13	–	R6...	–	LG3...
90	P16	–	39	–	–	–	–	R0	R00	–	–	–	–
91	P17	–	40	–	–	–	–	R1	R01	–	–	–	–
92	P18	–	42	–	–	–	–	R2	R02	–	–	–	–
93	P19	–	43	–	–	–	–	R3	R03	–	–	–	–
94	P20	–	45	–	–	–	–	R4	R10	–	–	–	–
95	P21	–	46	–	–	–	–	R5	R11	–	–	–	–
96	P22	–	48	–	–	–	–	R6	R12	–	–	–	–
97	P23	–	49	–	–	–	–	R7	R13	–	–	–	–
54/61	ENABKL	4	5	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL	ENABKL
70	SHFCLK	9	13	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	SHFCLK	**SHFCLKI**	SHFCLK	SHFCLK	SHFCLK
69	M	1	7	M	M	M	M	M	M	M	M	M	M
68	LP	5	10	LP	LP	LP	LP	LP	LP	LP	LP	LP	LP
67	FLM	3	11	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM	FLM
68/69	DE	2	8	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE
–	VDDSAFE	6, 8	1	–	–	–	–	–	–	–	–	–	–
–	+12VSAFE	10	2	–	–	–	–	–	–	–	–	–	–
–	VEESAFE	12	3	–	–	–	–	–	–	–	–	–	–
–	GND	7,14,	6,9,12,14,	–	–	–	–	–	–	–	–	–	–
		16,18,	17,20,23,26,										
		20,22,	29,32,35,38,										
		24,26	41,44,47,50										





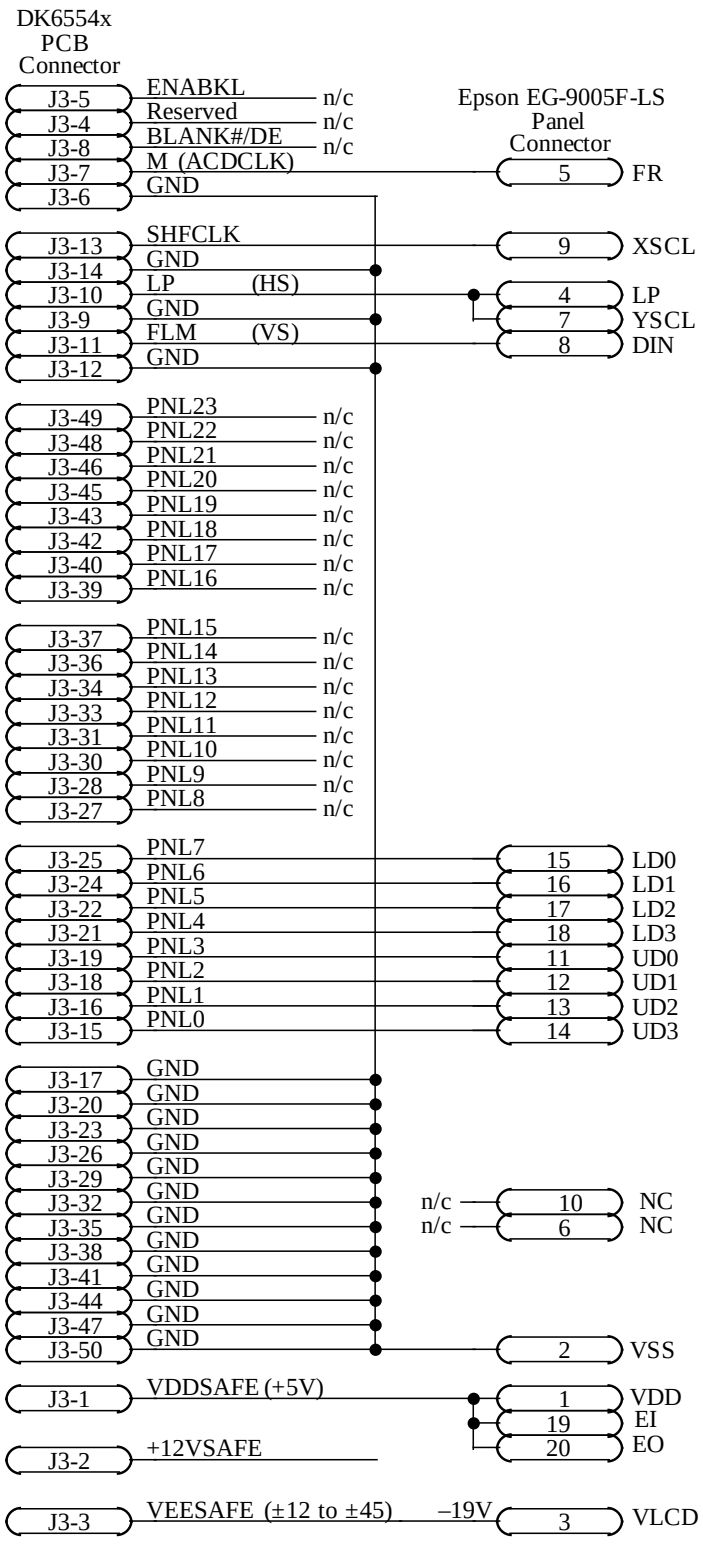
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	001	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (CMPR ena)	XR2F/2D	062h	
LP Delay (CMPR disa)	XR2F/2E	06Dh	
LP Pulse Width	XR2F[3-0]	8h	
LP Polarity	XR54[6]	0	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	0	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	60h	
Alt Hsync End (CR05)	XR1A	00h	
Alt H Total (CR00)	XR1B	60h	
Alt V Total (CR06)	XR65/64	20Dh	
Alt Vsync Start (CR10)	XR65/66	1E8h	
Alt Vsync End (CR11)	XR67[3-0]	0Ah	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	00	No FRC
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	1	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

6554x Interface - Matsushita S804 (640x480 16-Gray Level Plasma Panel)



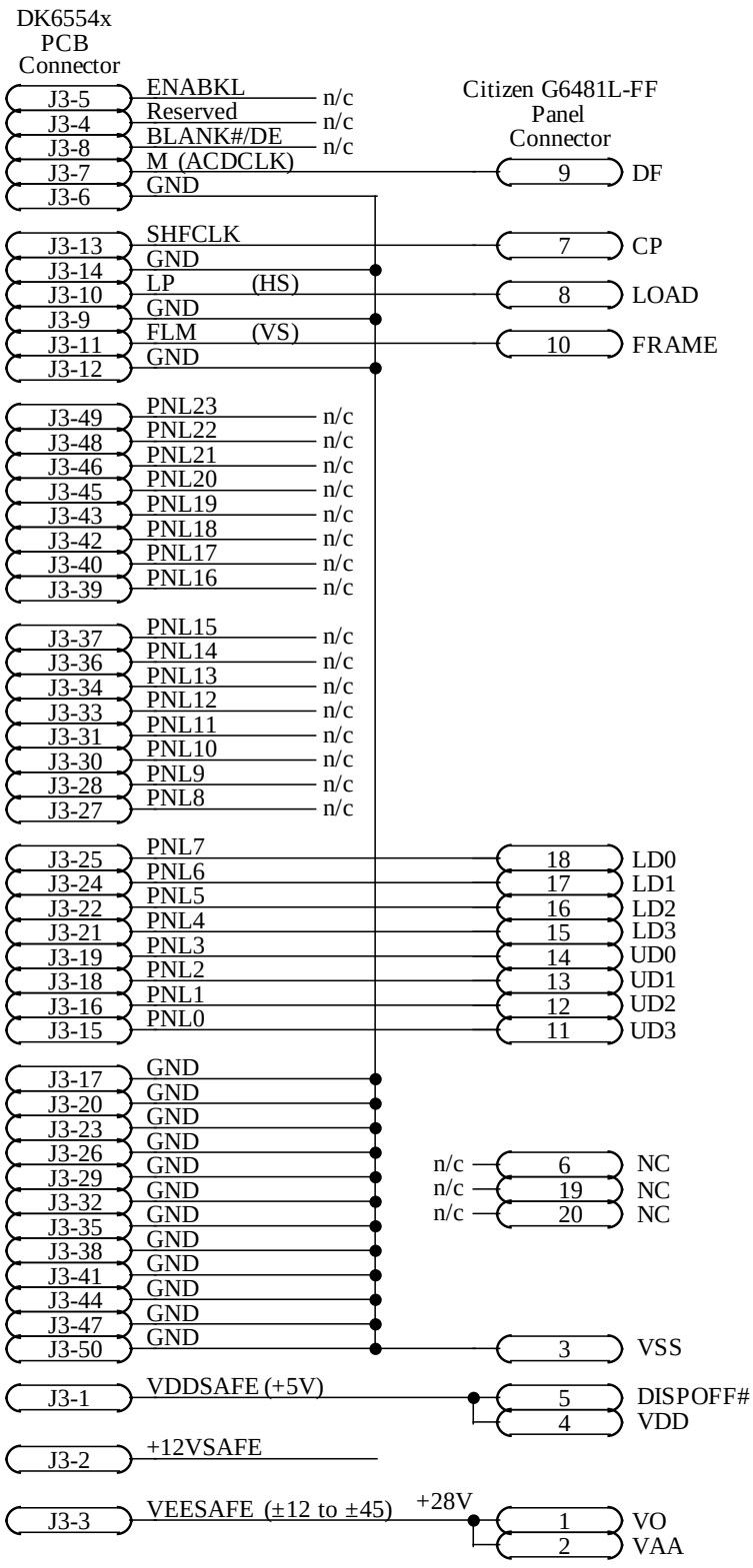
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	001	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (CMPR ena)	XR2F/2D	04Fh	
LP Delay (CMPR disa)	XR2F/2E	04Eh	
LP Pulse Width	XR2F[3-0]	01h	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	1	
FLM Delay	XR2C	0Ch	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	52h	
Alt Hsync End (CR05)	XR1A	15h	
Alt H Total (CR00)	XR1B	54h	
Alt V Total (CR06)	XR65/64	1F0h	
Alt Vsync Start (CR10)	XR65/66	1E5h	
Alt Vsync End (CR11)	XR67[3-0]	0Eh	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	00	No FRC
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	0	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

6554x Interface - Sharp LJ64ZU50 (640x480 16-Gray Level EL Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

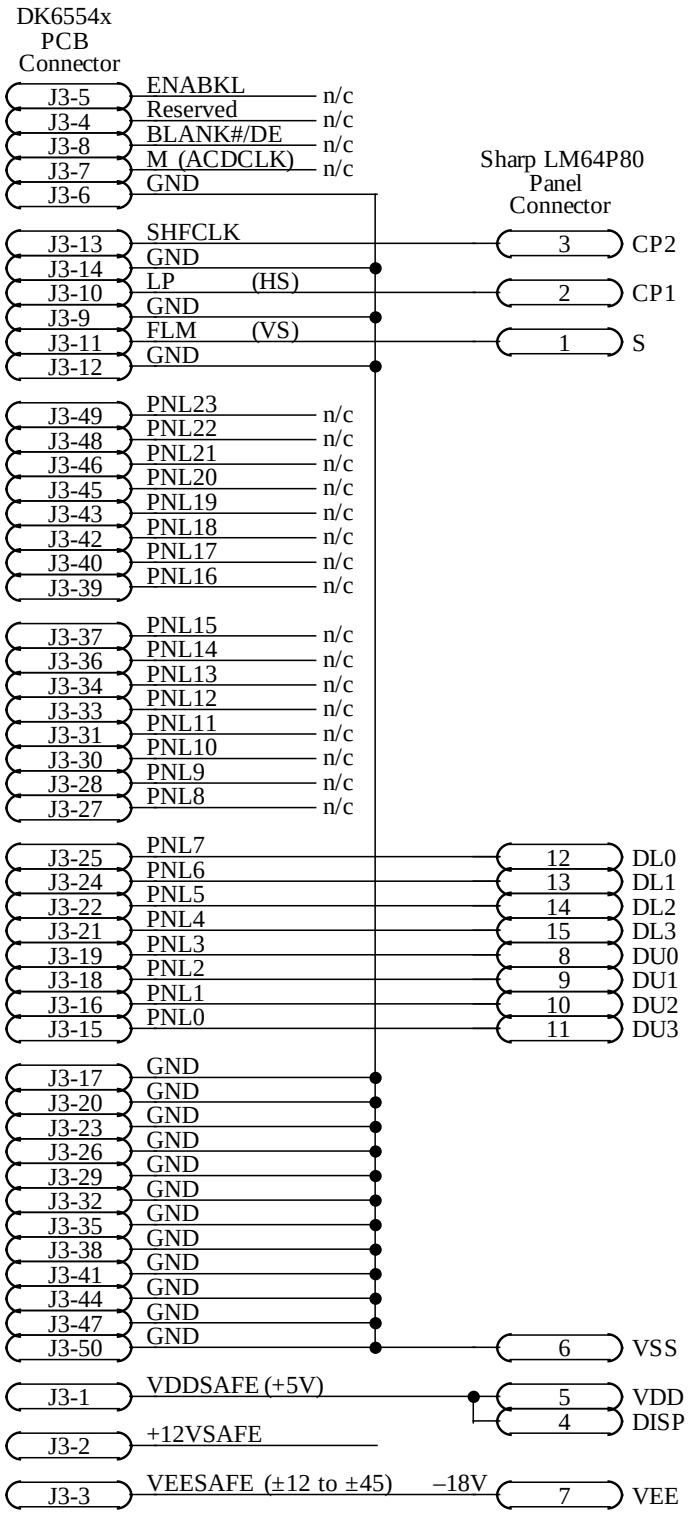
6554x Interface - Epson EG-9005F-LS (640x480 Monochrome LCD DD Panel)



Programming Recommendations/Requirements

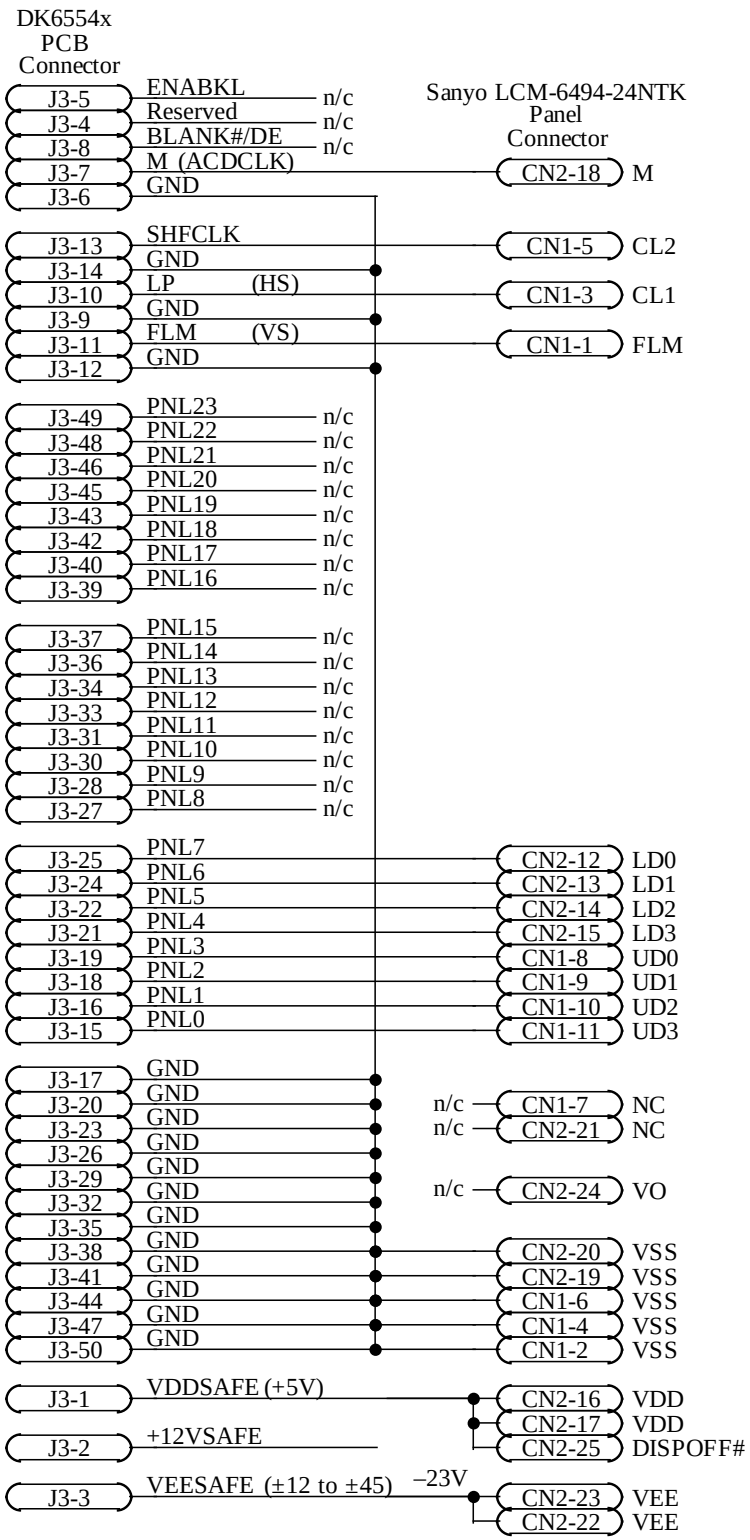
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Citizen G6481L-FF (640x480 Monochrome LCD DD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	11	DD
Clock Divide (CD)	XR50[6-4]	010	Dclk / 4
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]	100	16Level (61w/dith)
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	0	n/a
Frame Accel Ena	XR6F[1]	1	Enabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]	0	Enabled
LP Delay (CMPR ena)	XR2F/2D	050h	
LP Delay (CMPR disa)	XR2F/2E	050h	
LP Pulse Width	XR2F[3-0]	0h	
LP Polarity	XR54[6]		
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]	0	Enabled
FLM Delay	XR2C	04h	4 lines
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19	57h	
Alt Hsync End (CR05)	XR1A	19h	
Alt H Total (CR00)	XR1B	59h	
Alt V Total (CR06)	XR65/64	1E4h	
Alt Vsync Start (CR10)	XR65/66	1E0h	
Alt Vsync End (CR11)	XR67[3-0]	1	
Alt Hsync Polarity	XR55[6]	1	Negative
Alt Vsync Polarity	XR55[7]	1	Negative
Display Quality Recommendations			
FRC	XR50[1-0]	01	16-Frame FRC
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	n/a
FRC Polynomial	XR6E[7-0]	26h	
Dither	XR50[3-2]	01	256-color modes
M Phase Change	XR5E[7]	1	Every other frame
M Phase Change Count	XR5E[6-0]	00h	n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	Enabled
V Compensation	XR57[0]	1	Enabled
Fast Centering Disable	XR57[7]	0	Enabled
H AutoCentering	XR55[1]	0	Disabled
V AutoCentering	XR57[1]	1	Enabled
H Centering	XR56	00h	No left border
V Centering	XR59/58	000h	No top border
H Text Compression	XR55[2]	1	Enabled
H AutoDoubling	XR55[5]	1	Enabled
V Text Stretching	XR57[2]	0	Disabled
V Text Stretch Mode	XR57[4-3]	11	DS+TF,TF,DS
V Stretching	XR57[5]	0	Disabled
V Stretching Mode	XR57[6]	0	n/a
V Line Insertion Height	XR59[3-0]	0Fh	16 – 1
V H/W Line Replication	XR59[7]	0	Disabled
V Line Repl Height	XR5A[3-0]	0	n/a

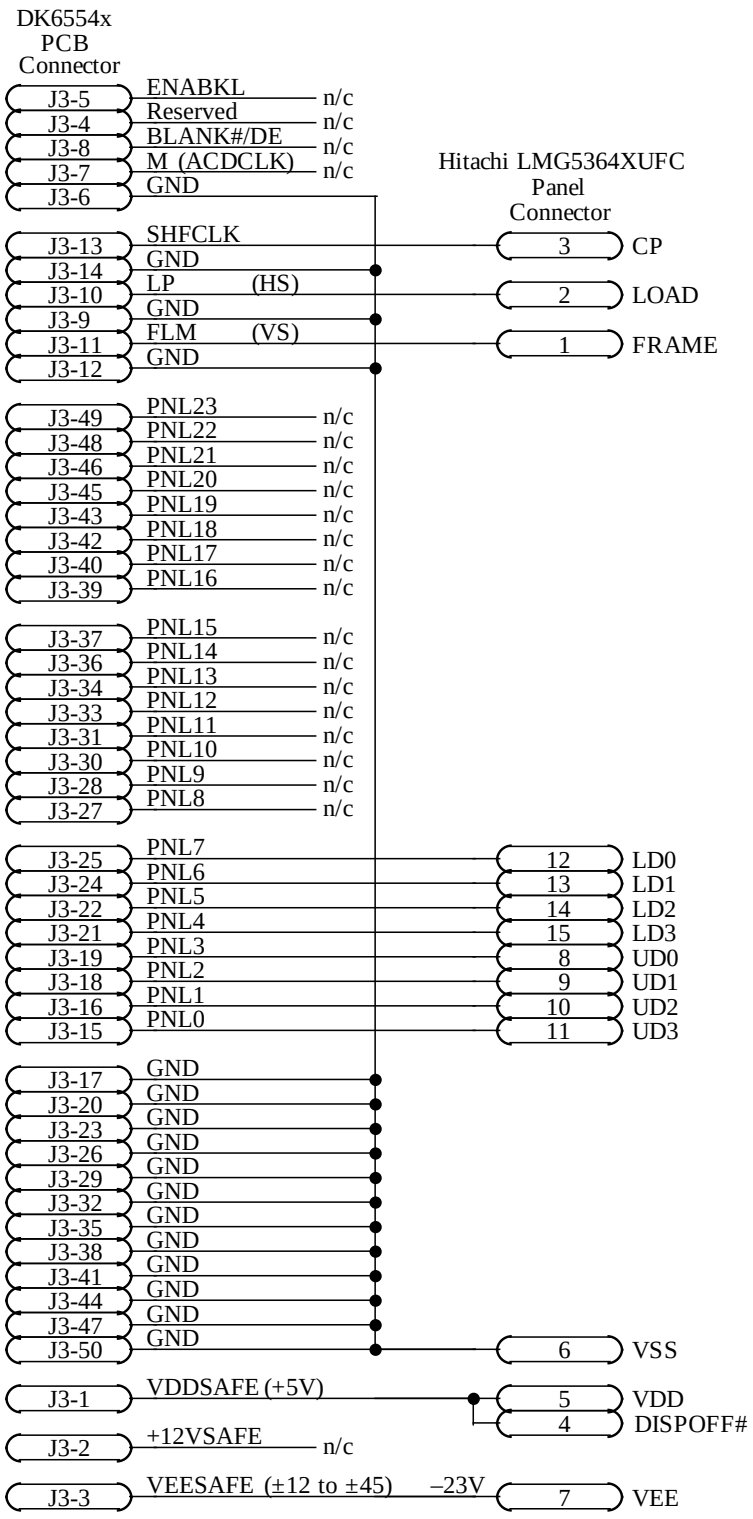
6554x Interface - Sharp LM64P80 (640x480 Monochrome LCD DD Panel)



Programming Recommendations/Requirements

Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

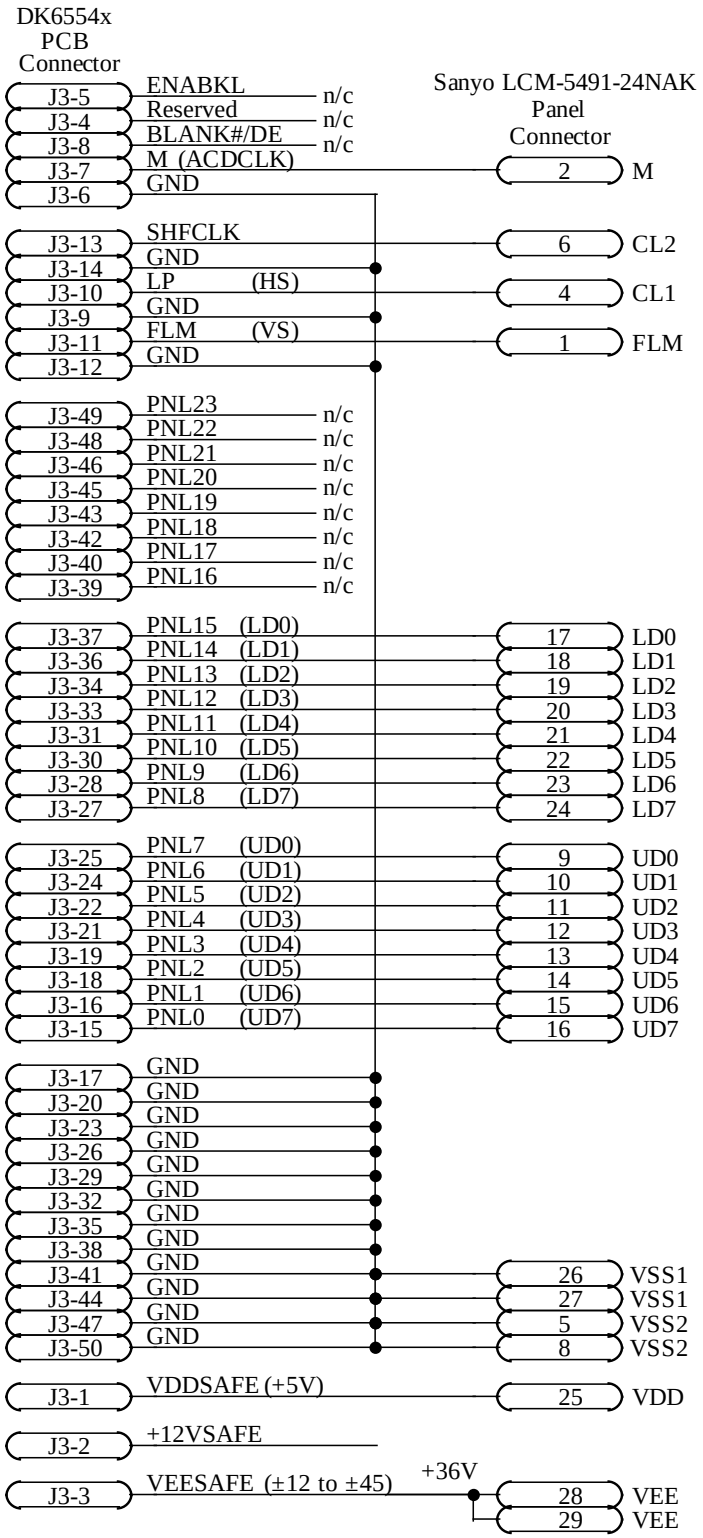
6554x Interface - Sanyo LCM-6494-24NTK (640x480 Monochrome LCD DD Panel)



Programming Recommendations/Requirements

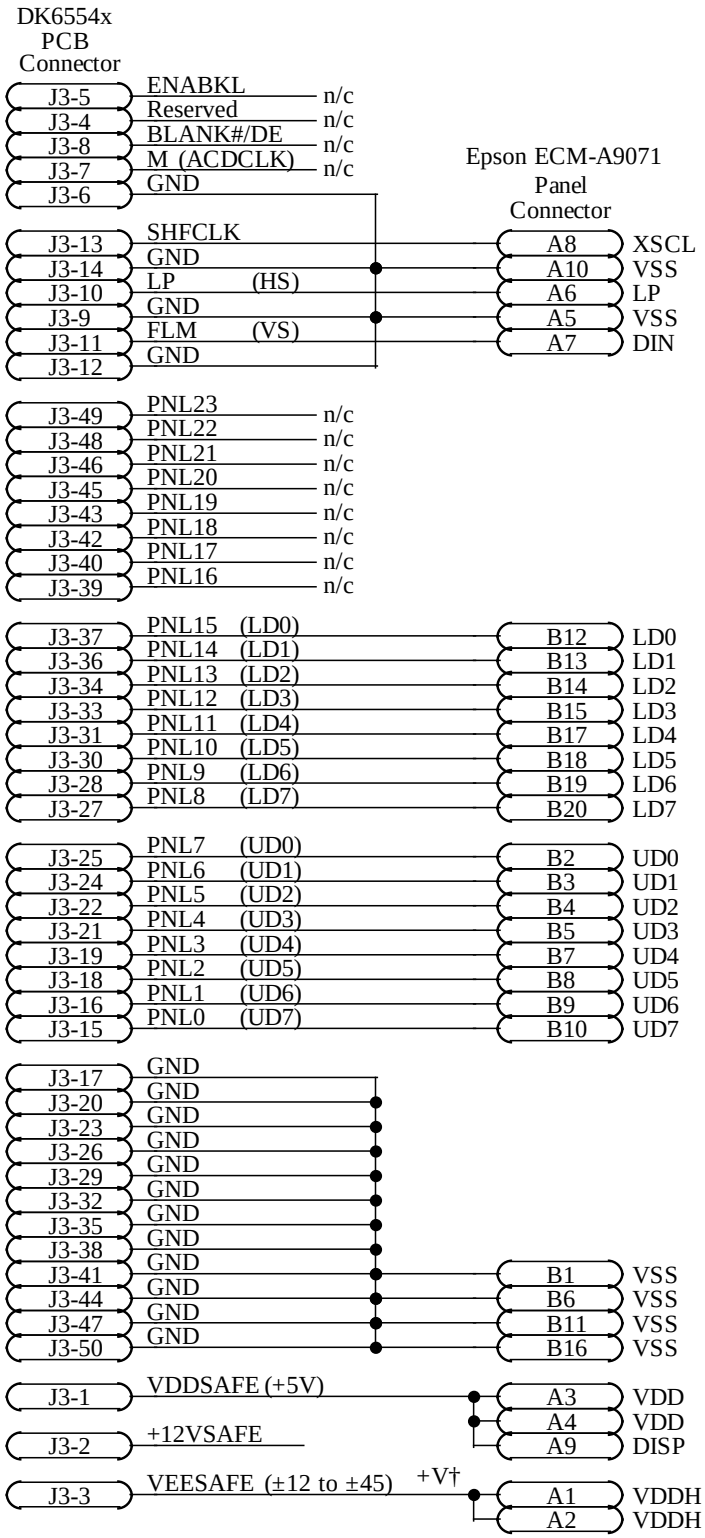
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Hitachi LMG5364XUFC (640x480 Monochrome LCD DD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Sanyo LCM-5491-24NAK (1024x768 LCD DD Panel)

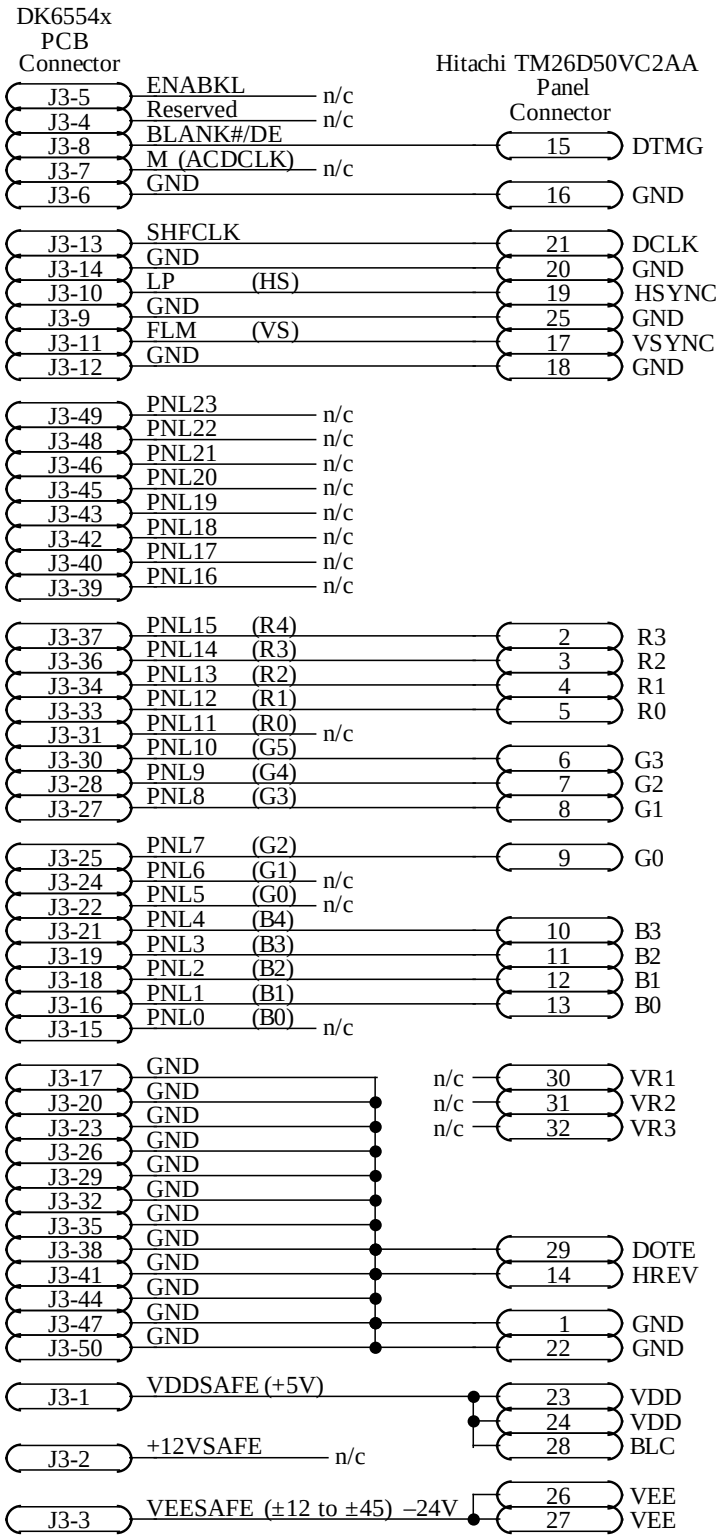


† Voltage not specified in panel data sheet; contact panel manufacturer for more information.

Programming Recommendations/Requirements

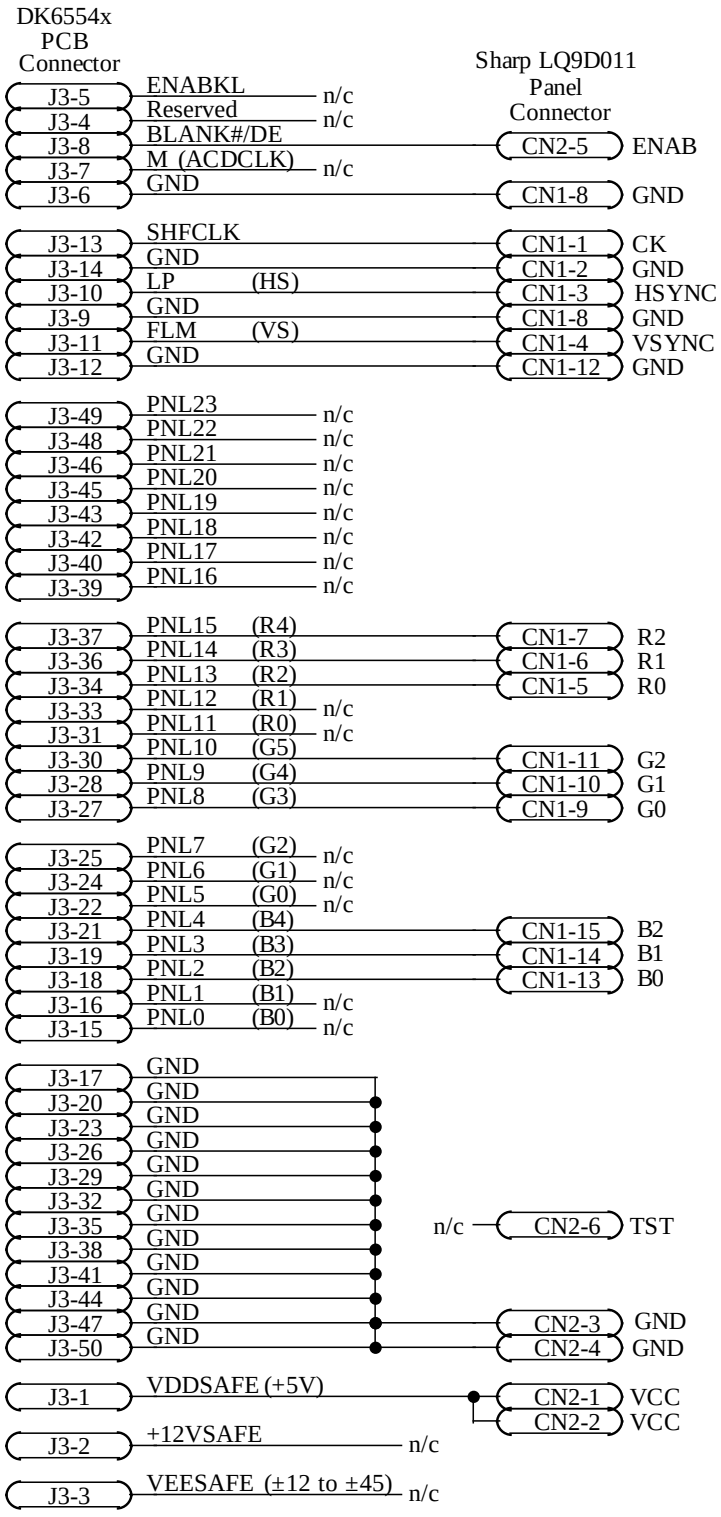
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Epson A9071 (1024x768 LCD DD Panel)



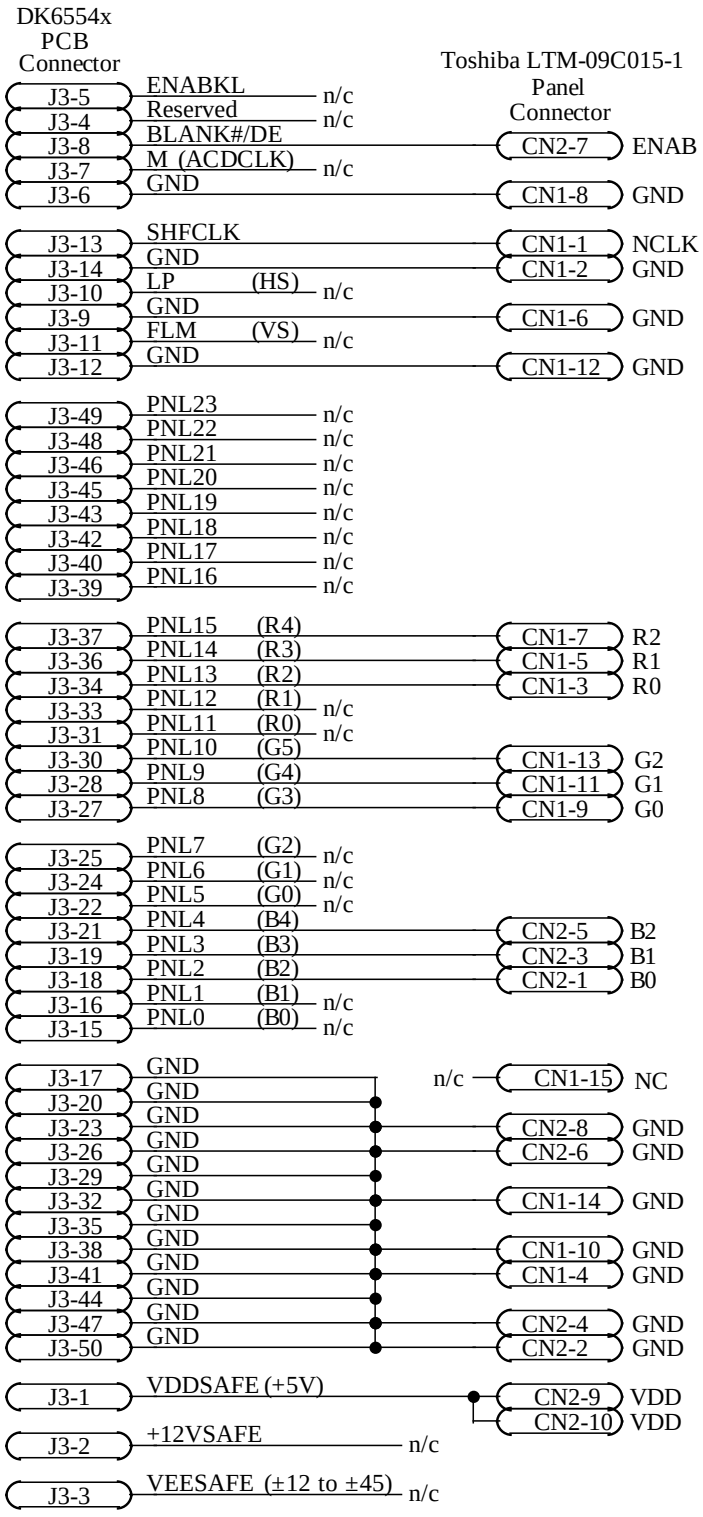
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (CMPR ena)	XR2F/2D	04Fh	
LP Delay (CMPR disa)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	1	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

6554x Interface - Hitachi TM26D50VC2AA (640x480 512-Color TFT LCD Panel)



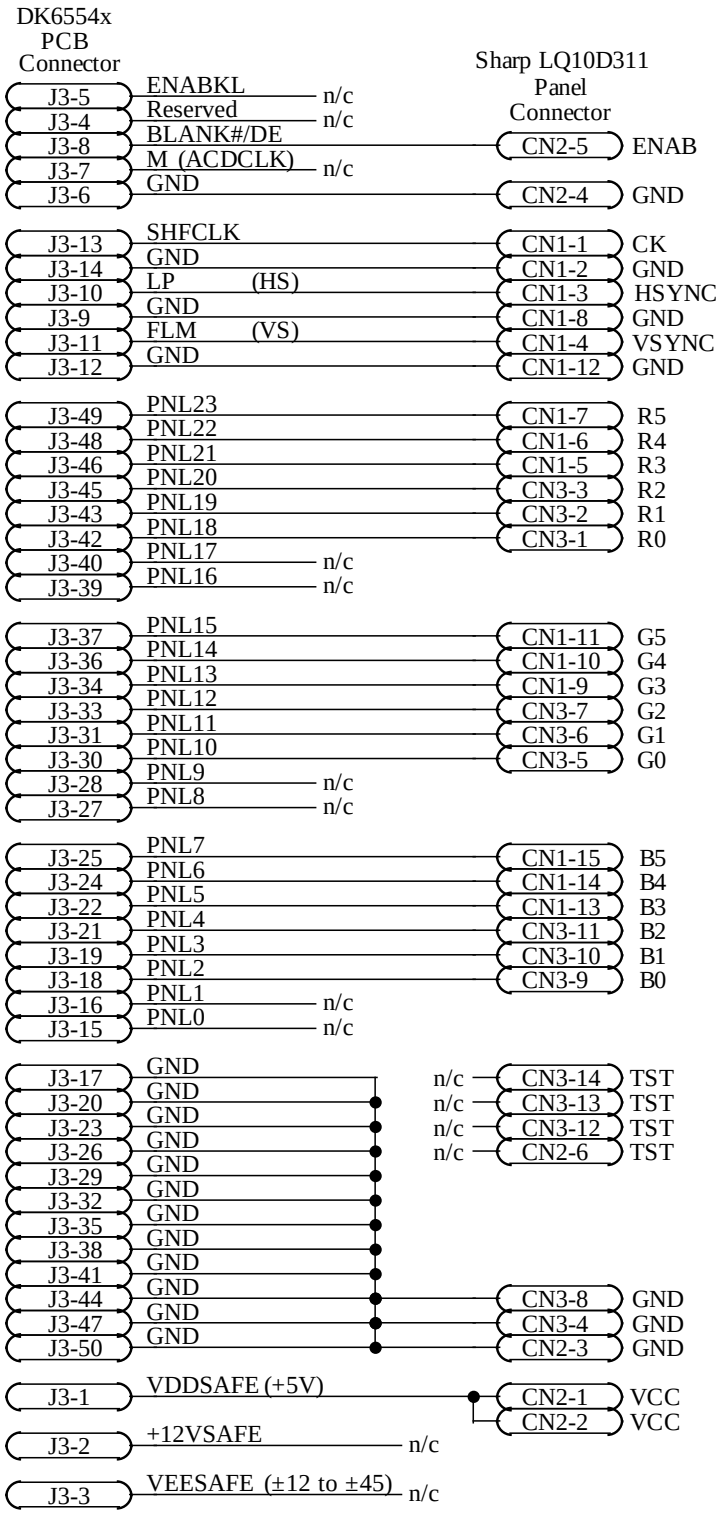
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (CMPR ena)	XR2F/2D	04Fh	
LP Delay (CMPR disa)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	1	
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

6554x Interface - Sharp LQ9D011 (640x480 512-Color TFT LCD Panel)



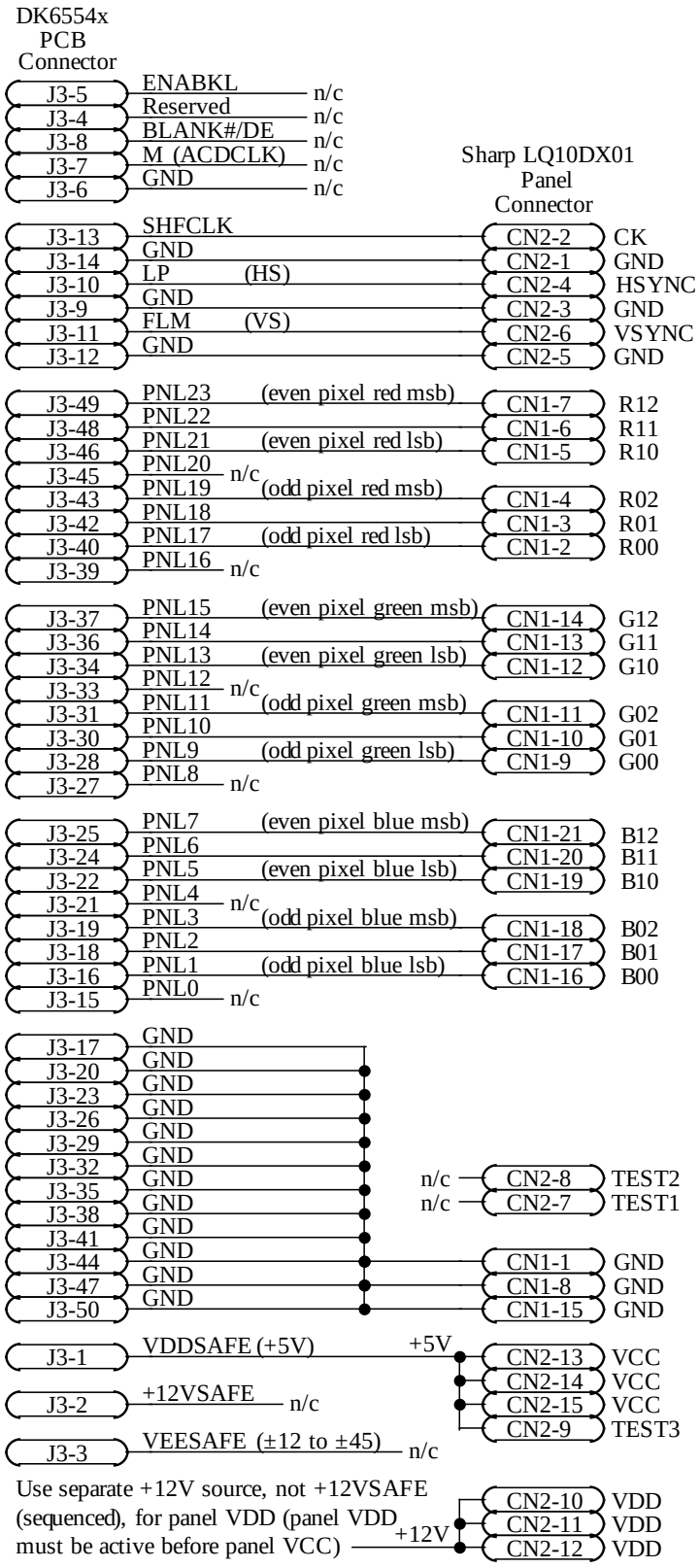
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]	00	
Clock Divide (CD)	XR50[6-4]	000	
Shiftclk Div (SD)	XR51[3]	0	
Gray/Color Levels	XR4F[2-0]	100	
TFT Data Width	XR50[7]	0	n/a
STN Pixel Packing	XR53[5-4]	00	n/a
Frame Accel Ena	XR6F[1]	0	Disabled
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]	0	
LP Delay Disable	XR2F[6]	0	
LP Delay (CMPR ena)	XR2F/2D	04Fh	
LP Delay (CMPR disa)	XR2F/2E	04Fh	
LP Pulse Width	XR2F[3-0]	0Fh	
LP Polarity	XR54[6]	1	
LP Blank	XR4F[7]	0	
LP Active during V	XR51[7]	1	
FLM Delay Disable	XR2F[7]	0	
FLM Delay	XR2C	04h	
FLM Polarity	XR54[7]	1	
Blank#/DE Polarity	XR54[0]	1	
Blank#/DE H-Only	XR54[1]	0	Reqd for this panel
Blank#/DE CRT/FP	XR51[2]	1	
Alt Hsync Start (CR04)	XR19	56h	
Alt Hsync End (CR05)	XR1A	13h	
Alt H Total (CR00)	XR1B	5Fh	
Alt V Total (CR06)	XR65/64	201h	
Alt Vsync Start (CR10)	XR65/66	1DFh	
Alt Vsync End (CR11)	XR67[3-0]	5h	
Alt Hsync Polarity	XR55[6]	1	
Alt Vsync Polarity	XR55[7]	1	
Display Quality Recommendations			
FRC	XR50[1-0]	10	
FRC Option 1	XR53[2]	1	Set to 1
FRC Option 2	XR53[3]	1	Set to 1
FRC Option 3	XR53[6]	0	
FRC Polynomial	XR6E[7-0]		n/a
Dither	XR50[3-2]	01	
M Phase Change	XR5E[7]		n/a
M Phase Change Count	XR5E[6-0]		n/a
Compensation Typical Settings			
H Compensation	XR55[0]	1	
V Compensation	XR57[0]	1	
Fast Centering Disable	XR57[7]	0	
H AutoCentering	XR55[1]	0	
V AutoCentering	XR57[1]	0	
H Centering	XR56	00h	
V Centering	XR59/58	000h	
H Text Compression	XR55[2]	1	
H AutoDoubling	XR55[5]	1	
V Text Stretching	XR57[2]	1	
V Text Stretch Mode	XR57[4-3]	11	
V Stretching	XR57[5]	0	
V Stretching Mode	XR57[6]	0	
V Line Insertion Height	XR59[3-0]	0Fh	
V H/W Line Replication	XR59[7]	0	
V Line Repl Height	XR5A[3-0]	0	

6554x Interface - Toshiba LTM-09C015-1 (640x480 512-Color TFT LCD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

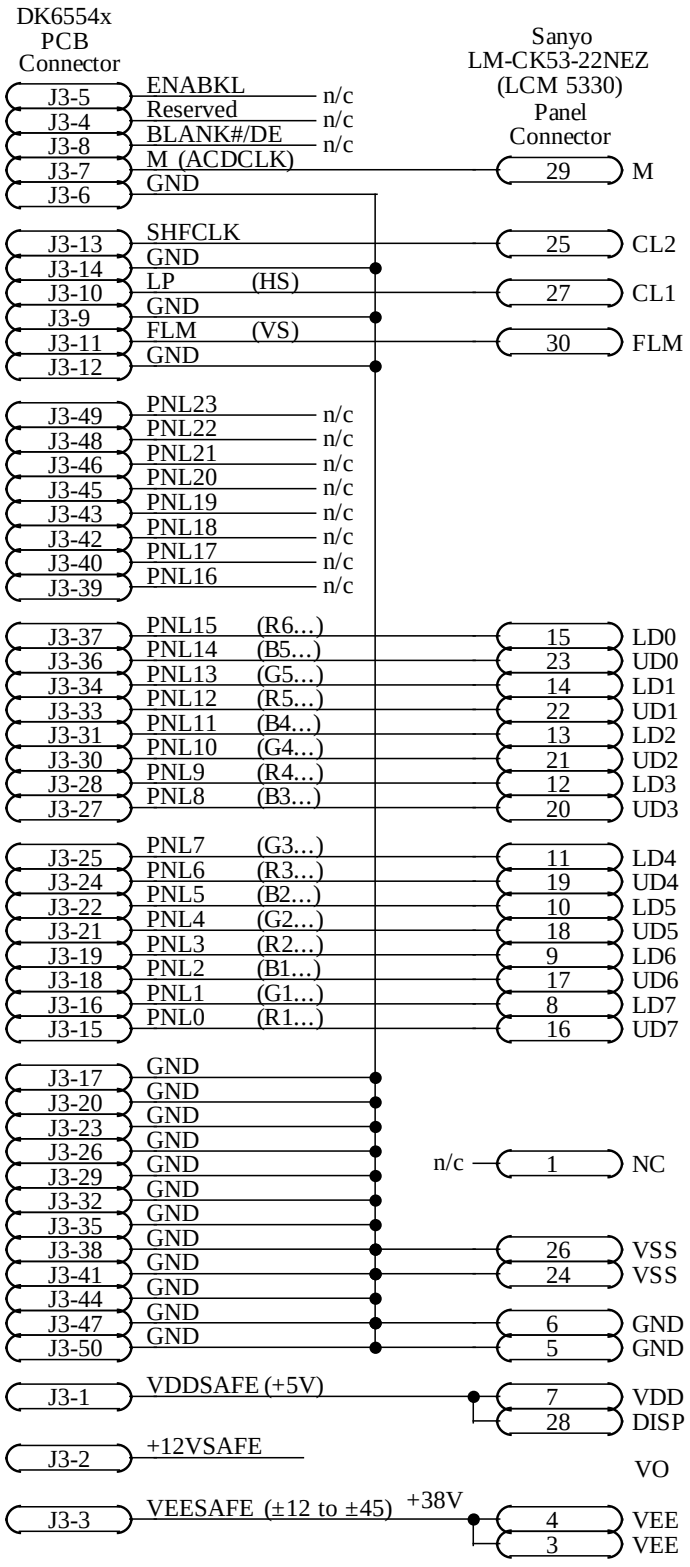
6554x Interface - Sharp LQ10D311 (640x480 256K-Color TFT LCD Panel)



Programming Recommendations/Requirements

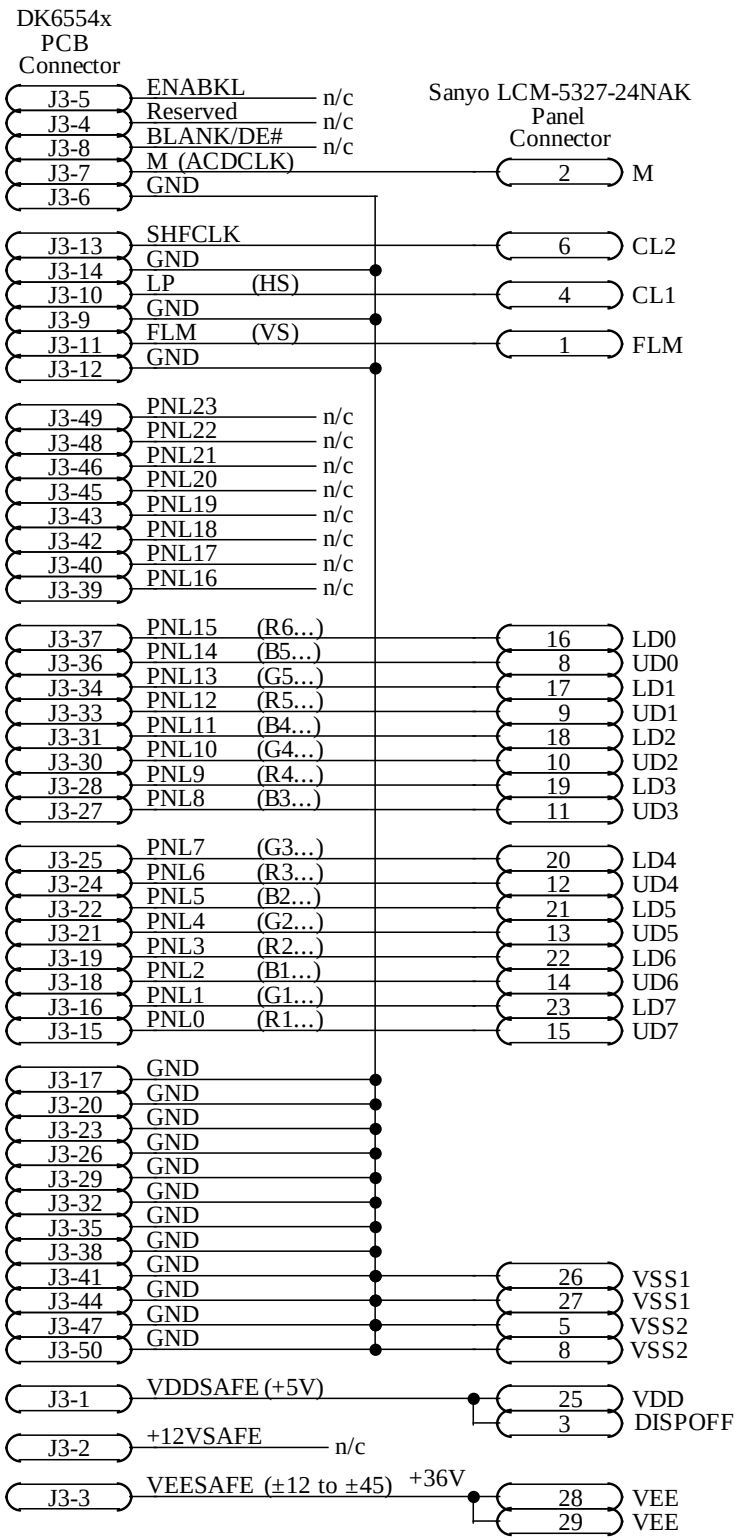
Parameter	Register	Value	Comment
Panel Width	XR1C	7Fh	(1024 / 8) – 1
Panel Height	XR65/68	2FFh	768 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Sharp LQ10DX01 (1024x768 512-Color TFT LCD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

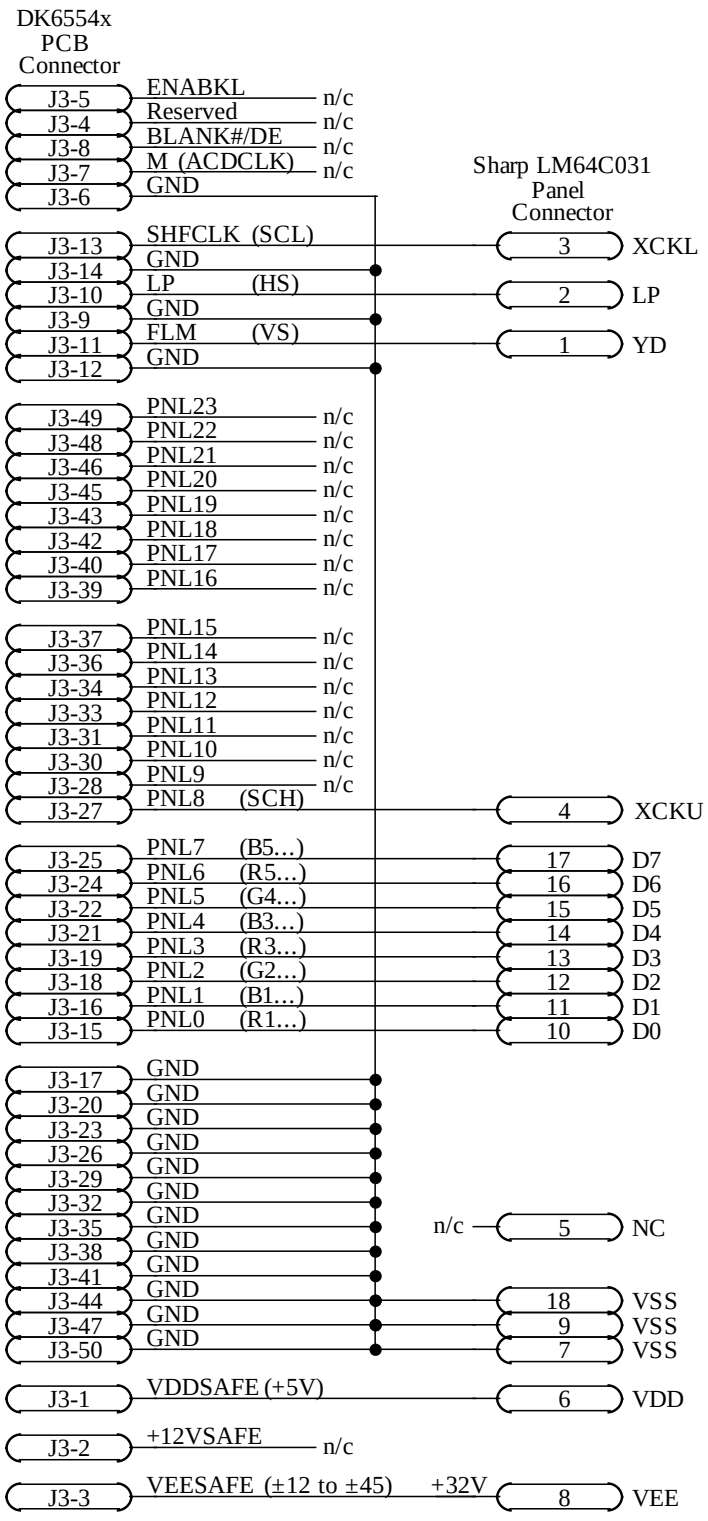
6554x Interface - Sanyo LM-CK53-22NEZ (LCM 5330) (640x480 Color STN LCD Panel)



Programming Recommendations/Requirements

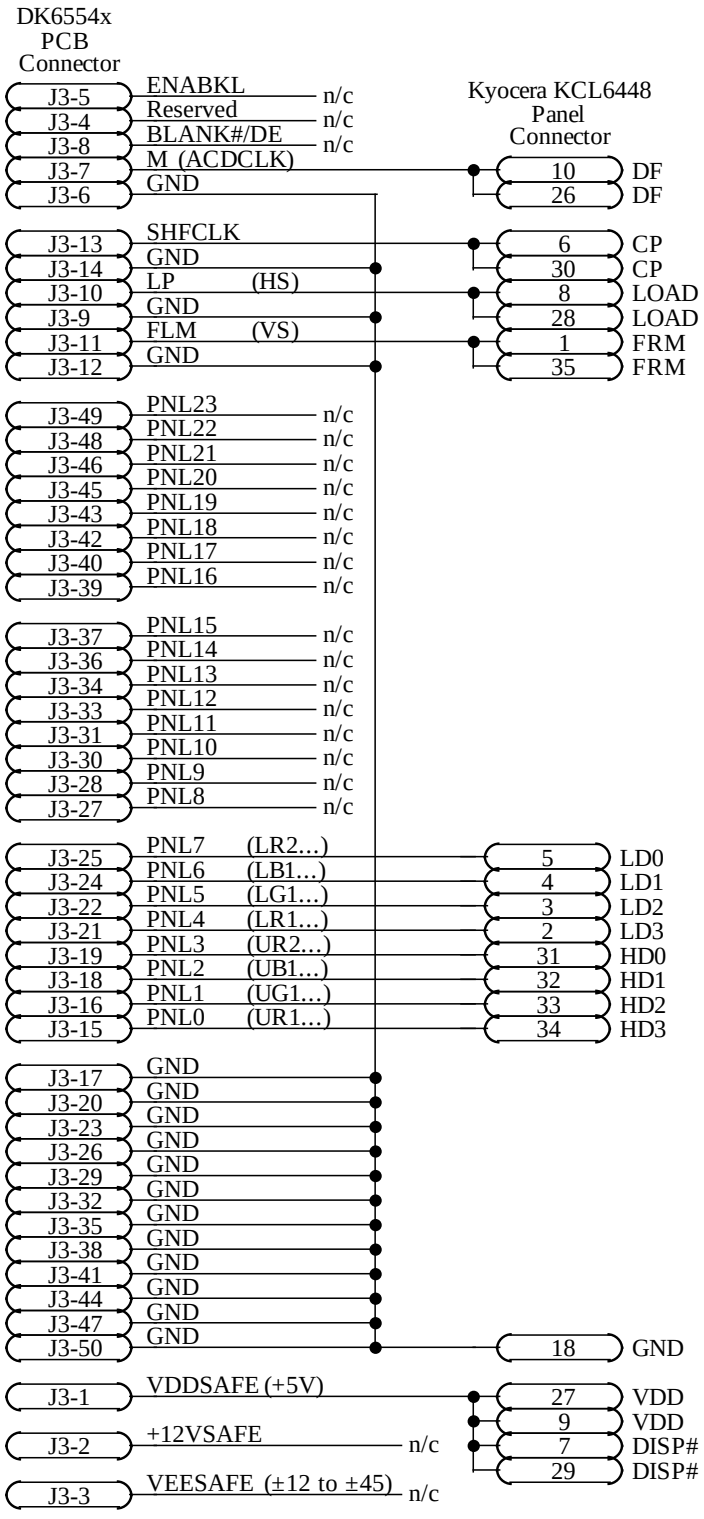
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Sanyo LCM5327-24NAK (640x480 Color STN LCD Panel)



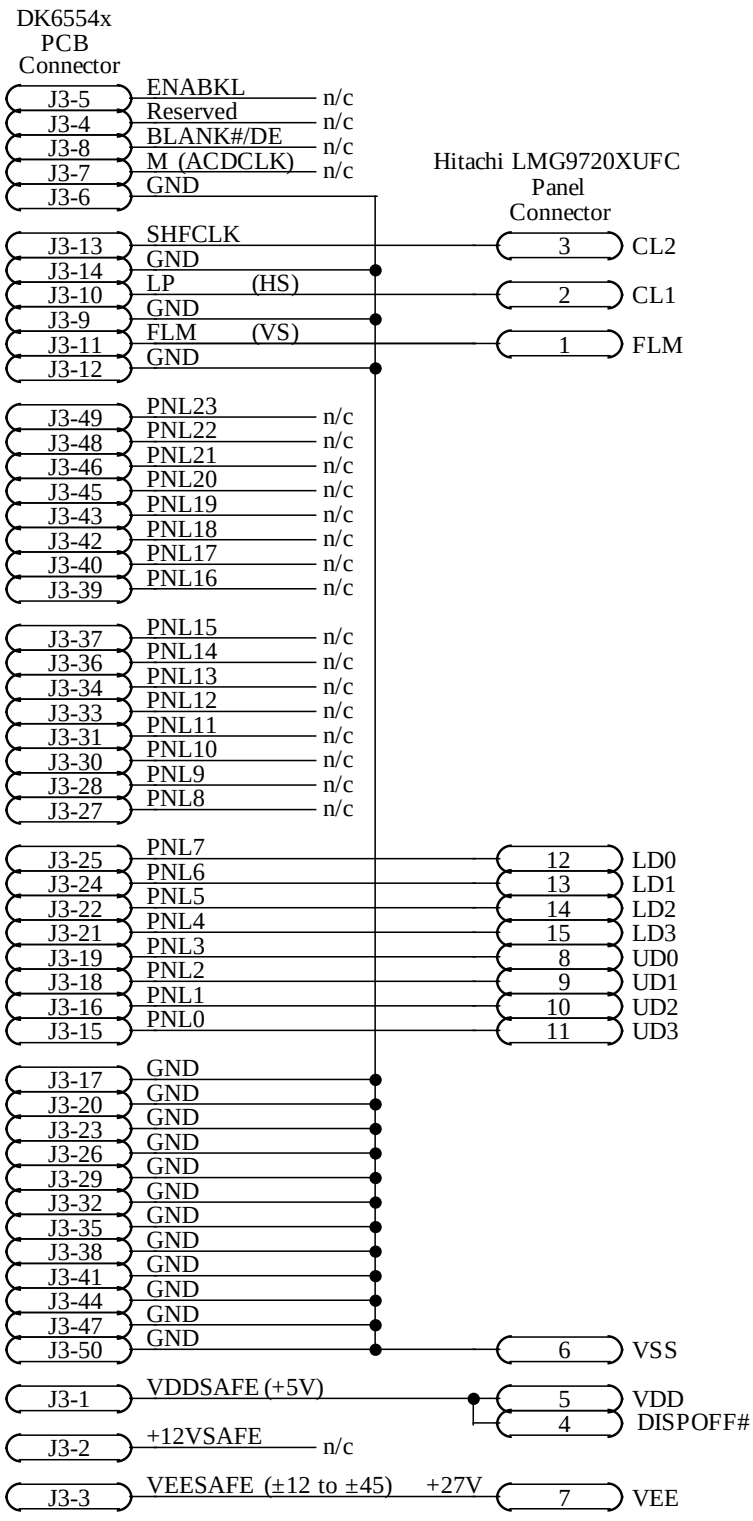
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Sharp LM64C031 (640x480 Color STN LCD Panel)



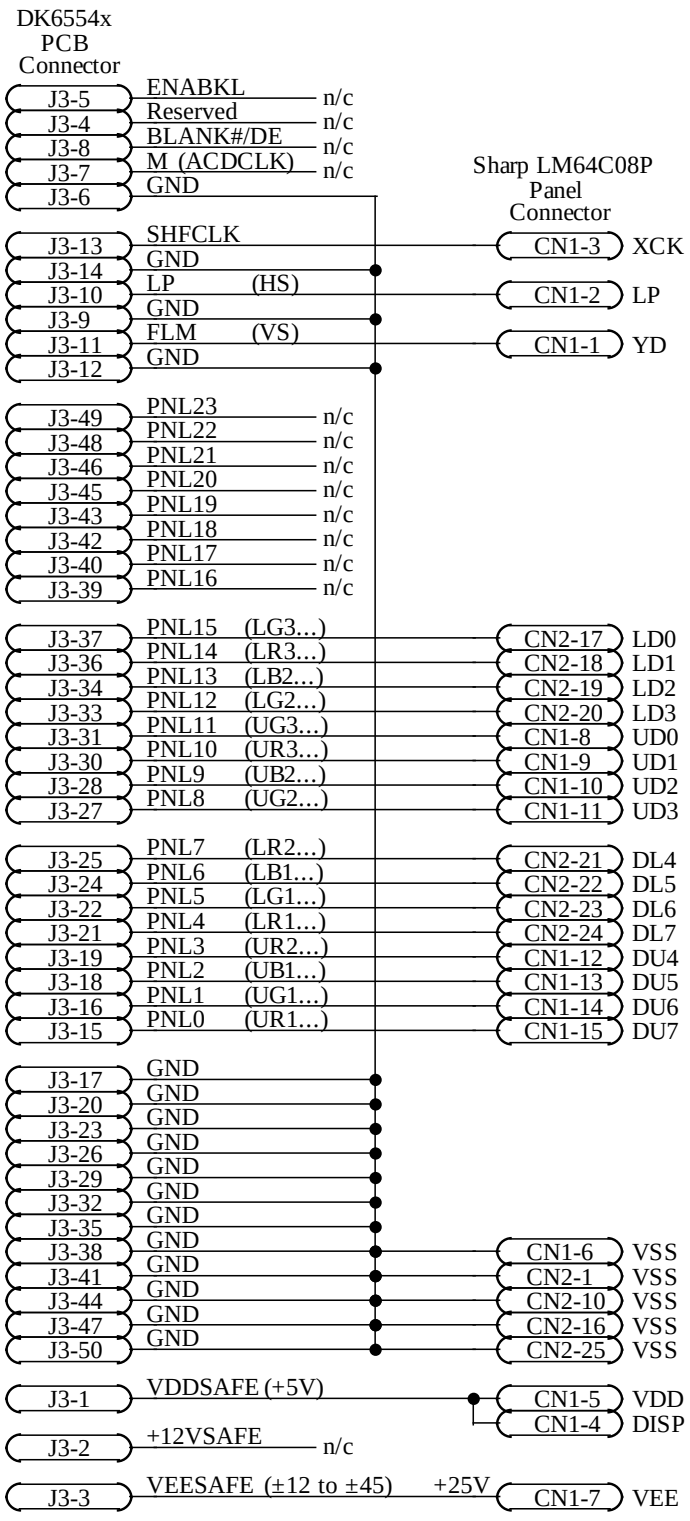
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Kyocera KCL6448 (640x480 Color STN-DD LCD Panel)



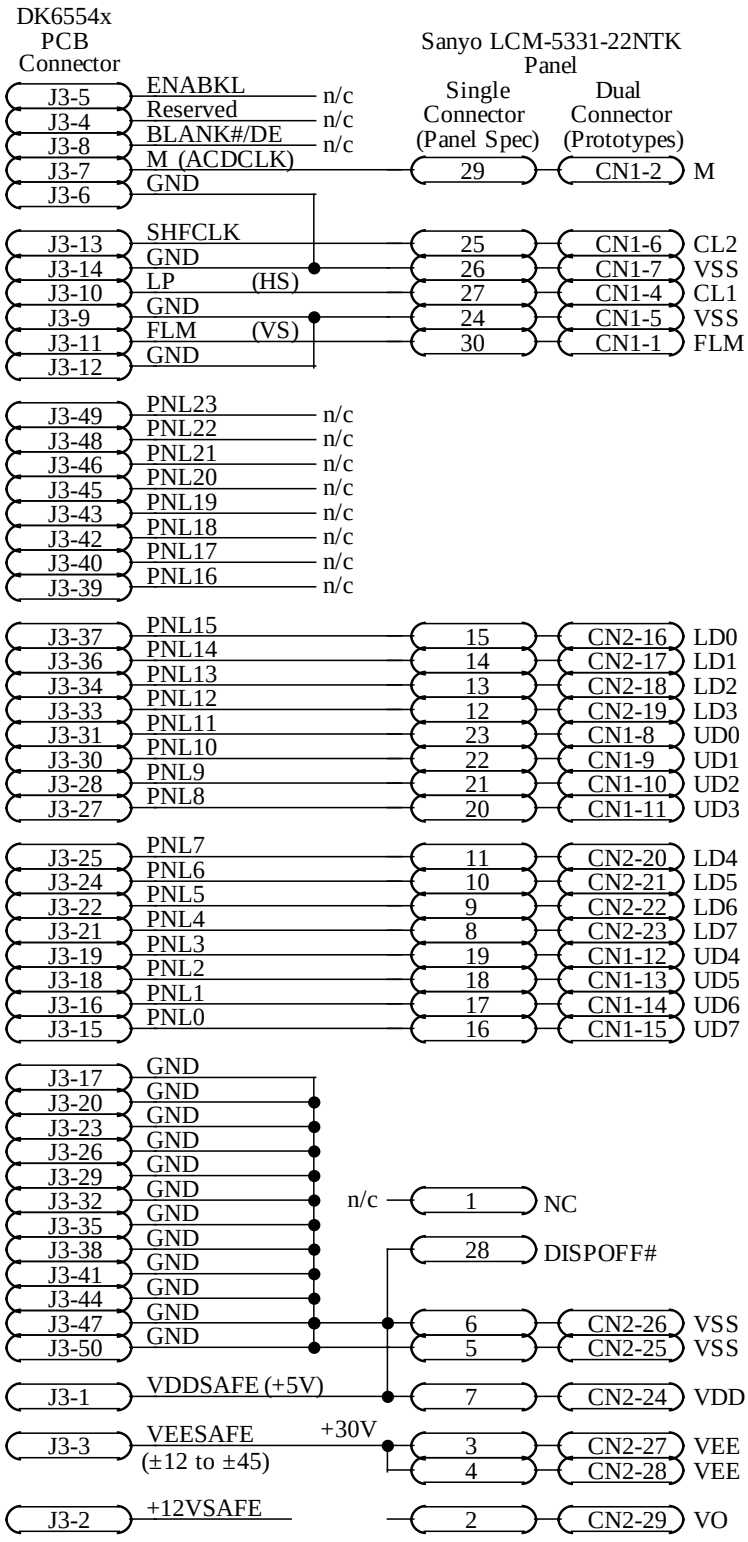
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Hitachi LMG9720XUFC (640x480 Color STN-DD LCD Panel)



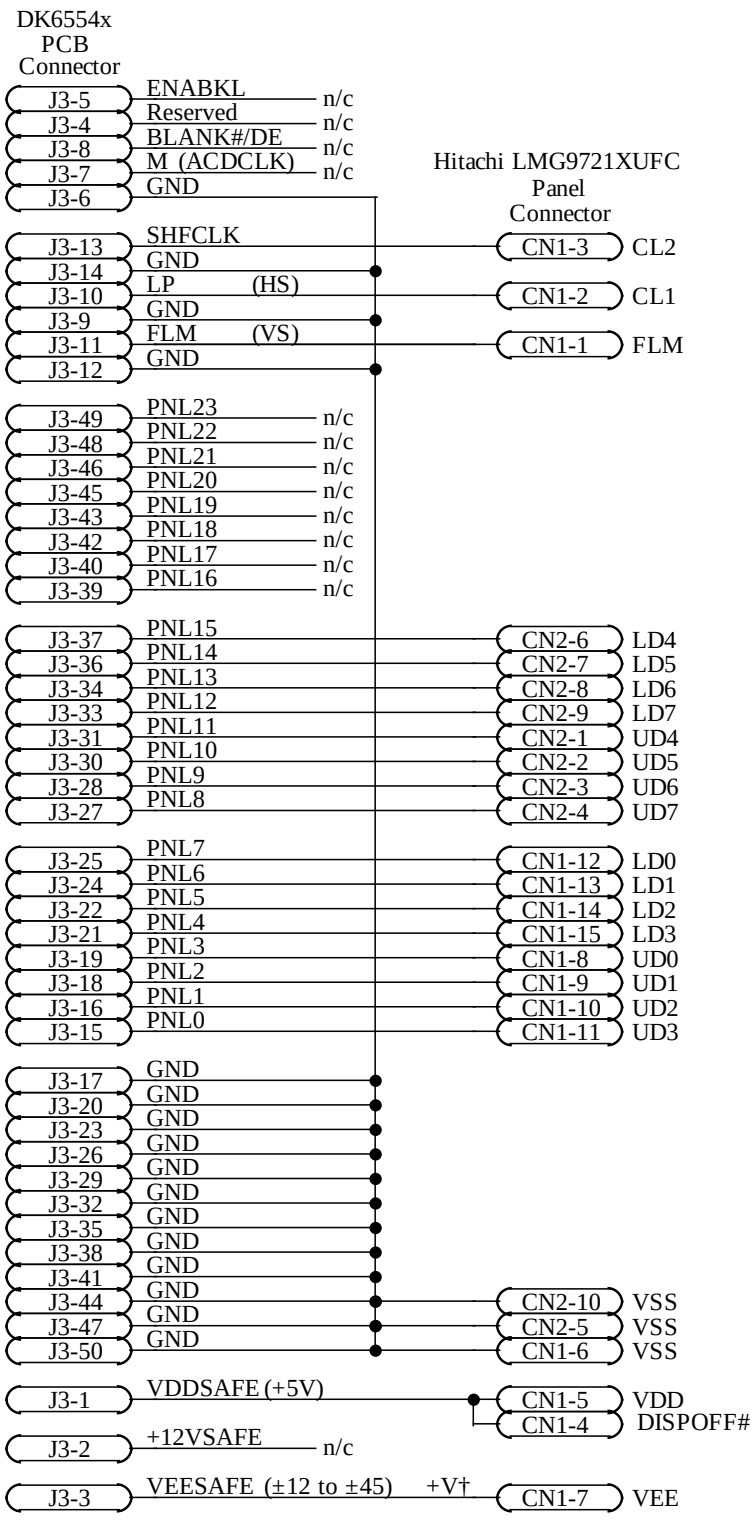
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]	0BAh	**** Important ****
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Sharp LM64C08P (640x480 Color STN-DD LCD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

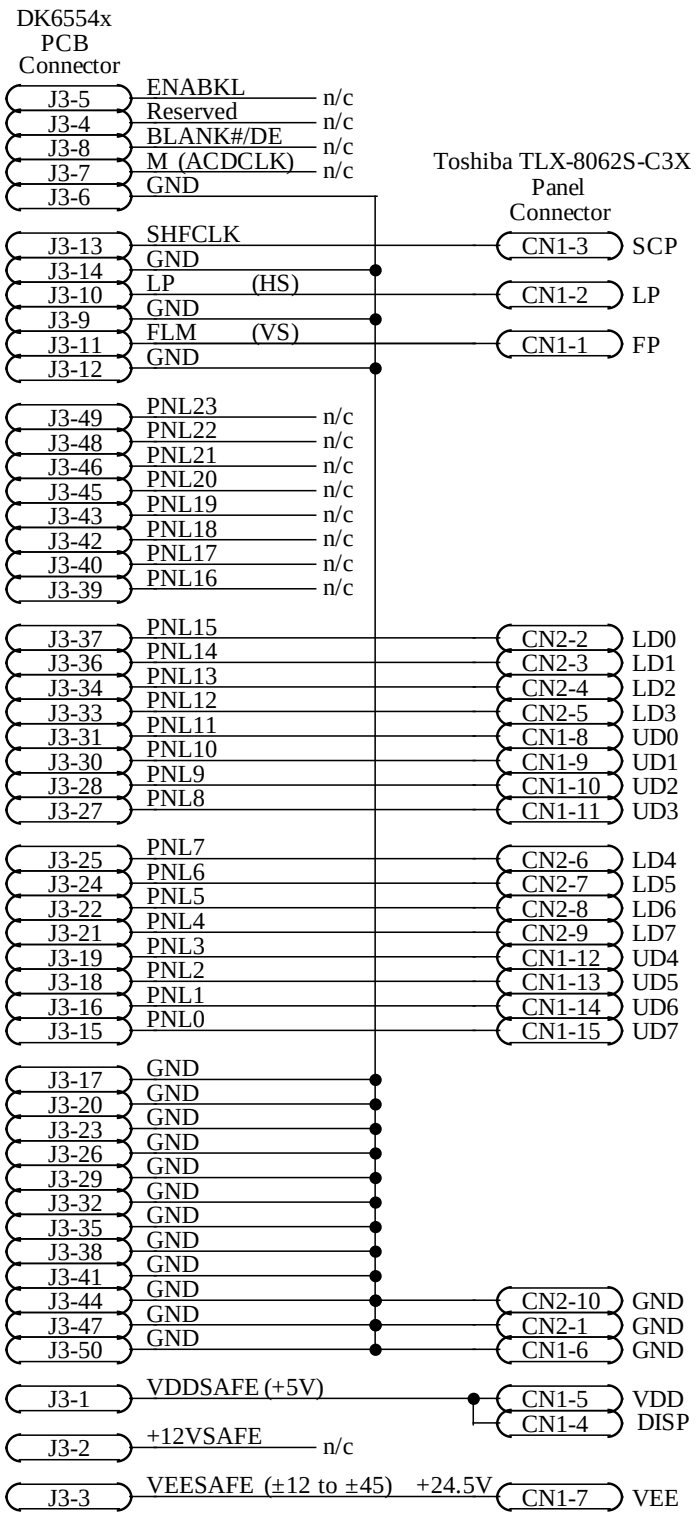
6554x Interface - Sanyo LCM-5331-22NTK (640x480 Color STN-DD LCD Panel)



† Voltage not specified in panel data sheet; contact panel manufacturer for more information.

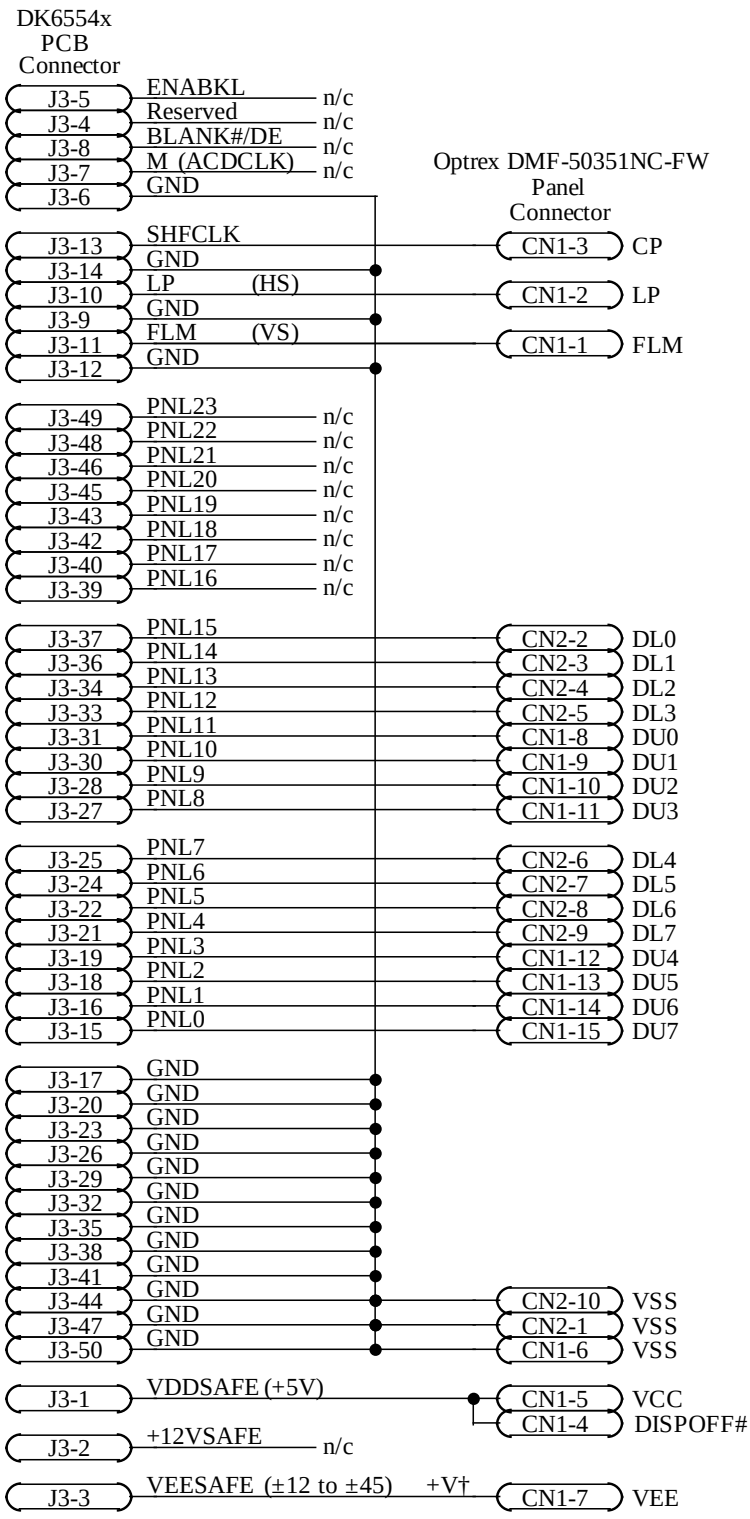
Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Hitachi LMG9721XUFC (640x480 Color STN-DD LCD Panel)



Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Toshiba TLX-8062S-C3X (640x480 Color STN-DD LCD Panel)



† Voltage not specified in panel data sheet; contact panel manufacturer for more information.

Programming Recommendations/Requirements			
Parameter	Register	Value	Comment
Panel Width	XR1C	4Fh	(640 / 8) – 1
Panel Height	XR65/68	1DFh	480 – 1
Panel Type	XR51[1-0]		
Clock Divide (CD)	XR50[6-4]		
Shiftclk Div (SD)	XR51[3]		
Gray/Color Levels	XR4F[2-0]		
TFT Data Width	XR50[7]		
STN Pixel Packing	XR53[5-4]		
Frame Accel Ena	XR6F[1]		
Output Signal Timing			
Shift Clock Mask (SM)	XR51[5]		
LP Delay Disable	XR2F[6]		
LP Delay (CMPR ena)	XR2F/2D		
LP Delay (CMPR disa)	XR2F/2E		
LP Pulse Width	XR2F[3-0]		
LP Polarity	XR54[6]		
LP Blank	XR4F[7]		
LP Active during V	XR51[7]		
FLM Delay Disable	XR2F[7]		
FLM Delay	XR2C		
FLM Polarity	XR54[7]		
Blank#/DE Polarity	XR54[0]		
Blank#/DE H-Only	XR54[1]		
Blank#/DE CRT/FP	XR51[2]		
Alt Hsync Start (CR04)	XR19		
Alt Hsync End (CR05)	XR1A		
Alt H Total (CR00)	XR1B		
Alt V Total (CR06)	XR65/64		
Alt Vsync Start (CR10)	XR65/66		
Alt Vsync End (CR11)	XR67[3-0]		
Alt Hsync Polarity	XR55[6]		
Alt Vsync Polarity	XR55[7]		
Display Quality Recommendations			
FRC	XR50[1-0]		
FRC Option 1	XR53[2]		
FRC Option 2	XR53[3]		
FRC Option 3	XR53[6]		
FRC Polynomial	XR6E[7-0]		
Dither	XR50[3-2]		
M Phase Change	XR5E[7]		
M Phase Change Count	XR5E[6-0]		
Compensation Typical Settings			
H Compensation	XR55[0]		
V Compensation	XR57[0]		
Fast Centering Disable	XR57[7]		
H AutoCentering	XR55[1]		
V AutoCentering	XR57[1]		
H Centering	XR56		
V Centering	XR59/58		
H Text Compression	XR55[2]		
H AutoDoubling	XR55[5]		
V Text Stretching	XR57[2]		
V Text Stretch Mode	XR57[4-3]		
V Stretching	XR57[5]		
V Stretching Mode	XR57[6]		
V Line Insertion Height	XR59[3-0]		
V H/W Line Replication	XR59[7]		
V Line Repl Height	XR5A[3-0]		

6554x Interface - Optrex DMF-50351NC-FW (640x480 Color STN-DD LCD Panel)

Electrical Specifications

65540/545 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	– 0.5	–	7.0	V
V_I	Input Voltage	– 0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	– 0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	– 25	–	85	° C
T_{STG}	Storage Temperature	– 40	–	125	° C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

65540/545 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage **(5V ± 10%)**	4.5	5	5.5	V
V_{CC}	Supply Voltage **(3.3V ± 10%)**	3.1	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	° C

65540/545 DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_O	Output Voltage	$I_O \leq 10$ mA	1.5	–	–	V
I_O	Output Current	$V_O \leq 1V$ @ 37.5Ω Load	21	–	–	mA
	Full Scale Error		–	–	± 5	%
	DAC to DAC Correlation		–	1.27	–	%
	DAC Linearity		± 2	–	–	LSB
	Full Scale Settling Time		–	–	28	nS
	Rise Time	10% to 90%	–	–	6	nS
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	mV

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz.
Electrical specifications contained herein are preliminary and subject to change without notice.

65540/545 DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, **5.5V**, 68 MHz, DAC on, 65540	–	180	230	mA
I_{CCDO}	Power Supply Current	0°C, **5.5V**, 68 MHz, DAC off, 65540	–	140	200	mA
I_{CCDO}	Power Supply Current	0°C, **3.3V**, 62 MHz, DAC off, 65540	–	78	132	mA
I_{CCDE}	Power Supply Current	0°C, **5.5V**, 68 MHz, DAC on, 65545	–	TBD	TBD	mA
I_{CCDO}	Power Supply Current	0°C, **5.5V**, 68 MHz, DAC off, 65545	–	TBD	TBD	mA
I_{CCDO}	Power Supply Current	0°C, **3.3V**, 56 MHz, DAC off, 65545	–	TBD	TBD	mA
I_{CCS}	Power Supply Current	0°C, **5.5V**, Standby†, 65540	–	–	200	µA
I_{CCS}	Power Supply Current	0°C, **5.5V**, Standby†, 65545	–	–	TBD	µA
I_{IL}	Input Leakage Current		– 100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	– 100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	– 100	–	+100	uA
V_{IL}	Input Low Voltage	All input pins	– 0.5	–	0.8	V
V_{OL}	Output Low Voltage	Under max load per table below **(5V)**	–	–	0.5	V
V_{OL}	Output Low Voltage	Under max load per table below **(3.3V)**	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below **(5V)**	V_{CC}– 0.5	–	–	V
V_{OH}	Output High Voltage	Under max load per table below **(3.3V)**	2.4	–	–	V
V_{IH}	Input High Voltage	All pins except XTALI	2.0	–	V_{CC}+0.5	V
V_{IH}	Input High Voltage	All pins except XTALI	2.0	–	V_{CC}+0.5	V

65540/545 DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	H/VSYNC, LDEV#, LRDY#, ROMCS#, IRQ	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	12	mA
		FLM, LP, M, P0-15, SHFCLK, D0-31	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		ENAVEE, ENAVDD, ENABKL, ACTI	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		RASA#, CASAH/L#, WEA#, PAR (65545 only)	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		RASB#, CASBH/L#, WEB#, OEAB#, AA0-9	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		RASC#, CASCH/L#, WEC#, OEC#, CA0-9	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	2	mA
I_{OH}	Output High Drive	H/VSYNC, LDEV#, LRDY#, ROMCS#, IRQ	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	12	mA
		FLM, LP, M, P0-15, SHFCLK, D0-31	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		ENAVEE, ENAVDD, ENABKL, ACTI	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		RASA#, CASAH/L#, WEA#, PAR (65545 only)	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RASB#, CASBH/L#, WEB#, OEAB#, AA0-9	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RASC#, CASCH/L#, WEC#, OEC#, CA0-9	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	2	mA

Note: IOL and IOH drive listed above indicates 5V low drive and 3.3V high drive (see also XR6C)

Note: †Standby power was measured using Self Refresh DRAMs with all chip inputs driven to inactive levels and outputs not connected (or connected to typical external loads).

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

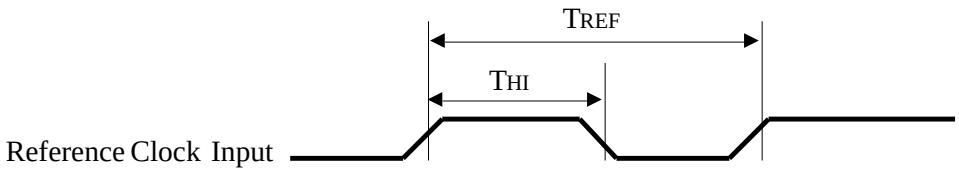
65540 / 545 AC TEST CONDITIONS

(Under Normal Operating Conditions Unless Noted Otherwise)

Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
All 12mA and 8mA outputs plus PAR for PCI bus in the 65545	V_{OL}	2.4V	80pF
All Other 4mA output pads	V_{OL}	2.4V	50pF
All Other 2mA output pads	V_{OL}	2.4V	30pF

65540 / 65545 AC TIMING CHARACTERISTICS - REFERENCE CLOCK

Symbol	Parameter	Notes	Min	Typ	Max	Units
F_{REF}	Reference Frequency	(±100 ppm)	1	14.31818	60	MHz
T_{REF}	Reference Clock Period	$1/F_{REF}$	16.6	69.84128	1000	nS
T_{HI}/T_{REF}	Reference Clock Duty Cycle		25	–	75	%

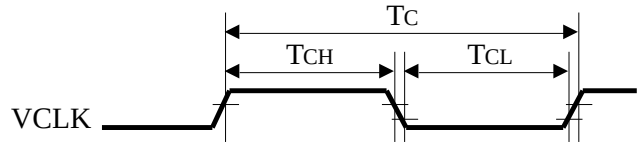


Reference Clock Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540/545 AC TIMING CHARACTERISTICS - CLOCK GENERATOR

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	VCLK Period **(5V)**	68 MHz	14.7	–	–	nS
T_C	VCLK Period **(3.3V)**	56 MHz	17.6	–	–	nS
T_{CH}	VCLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	VCLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period **(5V)**	68 MHz	14.7	–	–	nS
T_M	MCLK Period **(3.3V)**	56 MHz	17.6	–	–	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS
–	MCLK Frequency for 100 ns DRAMs **(5V)**		–	50.350	–	MHz
–	MCLK Frequency for 80 ns DRAMs **(5V)**		–	56.644	–	MHz
–	MCLK Frequency for 70 ns DRAMs **(5V)**		–	65	–	MHz



Clock Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540/545 AC TIMING CHARACTERISTICS - RESET

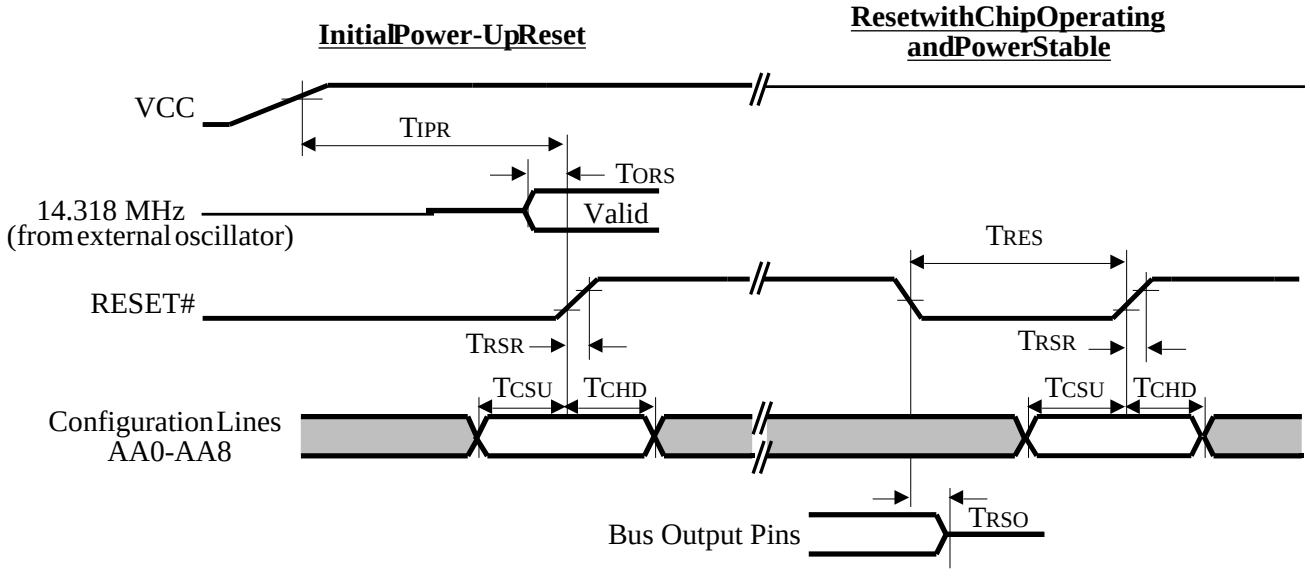
Symbol	Parameter	Notes	Min	Max	Units
T_{IPR}	Reset Active Time from Power Stable	See Note 1	5	–	**mS**
T_{ORS}	Reset Active Time from Ext. Osc. Stable	See Note 2	0	–	nS
T_{RES}	Reset Active Time with Power Stable	See Note 3	2	–	**mS**
T_{RSR}	Reset Rise Time	Reset fall time is non-critical	–	20	nS
T_{RSO}	Reset Active to Output Float Delay		–	40	nS
T_{CSU}	Configuration Setup Time	See Note 4	20	–	nS
T_{CHD}	Configuration Hold Time		5	–	nS

Note 1: This parameter includes time for internal voltage stabilization of all sections of the chip, startup and stabilization of the internal clock synthesizer, and setting of all internal logic to a known state.

Note 2: The external oscillator input is optional, it may be selected by XR01 bit 5.

Note 3: This parameter includes time for the internal clock synthesizer to reset to its default frequency and time to set all internal logic to a known state. It assumes power is stable and the internal clock synthesizer is already operating at some stable frequency.

Note 4: Setup time to latch the state of the configuration bits reliably into XR01 and XR6C is specified by this parameter. Changes in some configuration bits may take longer to stabilize inside the chip (such as internal clock synthesizer-related bits 4 and 5). It is therefore recommended that configuration bit setup time be TRES (2mS) to insure that the chip is in a completely stable state when Reset goes inactive.

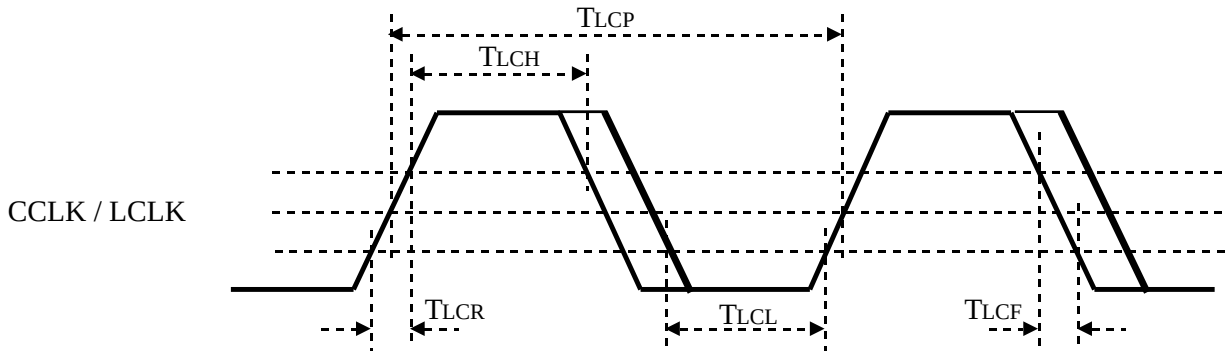


Reset Timing

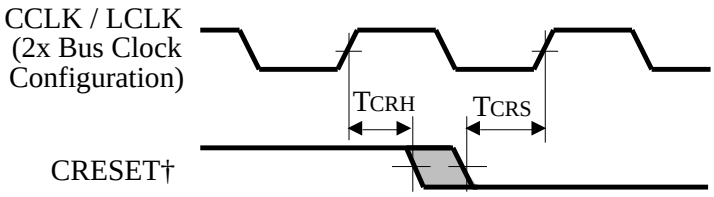
Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - LOCAL BUS CLOCK (33 MHz)

Symbol	Parameter	Notes	Min	Max	Units
T_{LCP}	Local Bus Clock Period **(33MHz)**	0.1% stability at 2.0V / 0.8V	30	30	nS
T_{LCH}	Local Bus Clock High Time		12	–	nS
T_{LCL}	Local Bus Clock Low Time		12	–	nS
T_{LCR}	Local Bus Clock Rise Time		–	3	nS
T_{LCF}	Local Bus Clock Fall Time		–	3	nS
—	Local Bus Clock Slew Rate		1	4	**V / nS**
T_{CRS}	CPU Reset Setup Time to Local Bus Clock	For 2x Clock Sync	2	–	nS
T_{CRH}	CPU Reset Hold Time from Local Bus Clock	For 2x Clock Sync	5	–	nS



Local Bus Clock Timing



† 65540/545 CRESET to CCLK timing should match CPU RESET to CLK2 timing of the CPU.

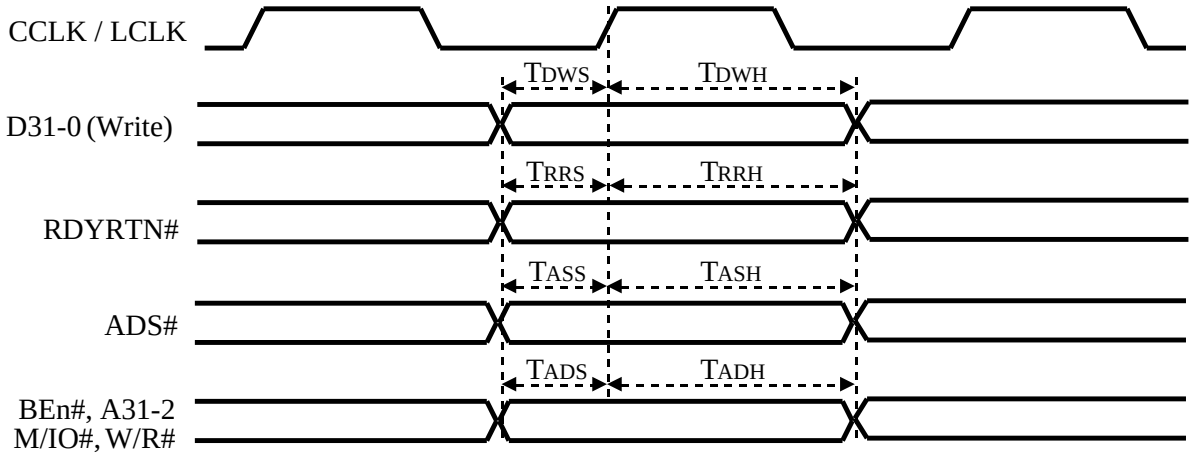
Local Bus '2x' Clock Synchronization Timing

Note: VL-Bus timing is compatible with VL-Bus Specification 2.0.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - LOCAL BUS INPUT SETUP & HOLD (33 MHz)

Symbol	Parameter	Notes	Min	Max	Units
T_{ADS}	Setup Time - A2-31, BEn#, M/IO#, W/R#		7	–	nS
T_{ASS}	Setup Time - ADS#		7	–	nS
T_{DWS}	Setup Time - D0-31 (Write)		7	–	nS
T_{RRS}	Setup Time - RDYRTN#		5	–	nS
T_{ADH}	Hold Time - A2-31, BEn#, M/IO#, W/R#		2	–	nS
T_{ASH}	Hold Time - ADS#		2	–	nS
T_{DWH}	Hold Time - D0-31 (Write)		2	–	nS
T_{RRH}	Hold Time - RDYRTN#		2	–	nS

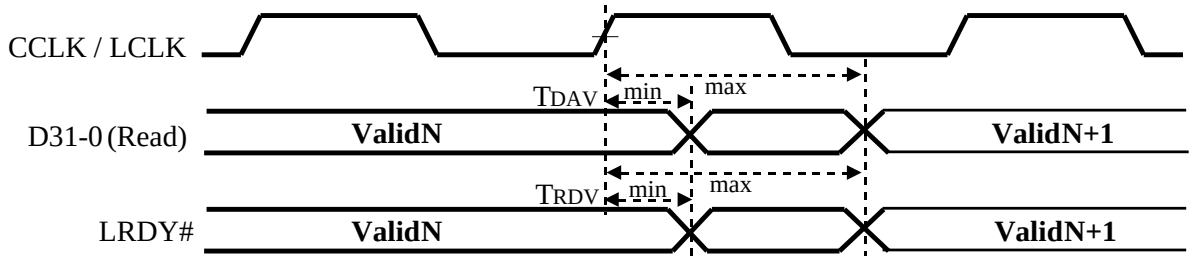


Local Bus Input Setup & Hold Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - LOCAL BUS OUTPUT VALID (33 MHz)

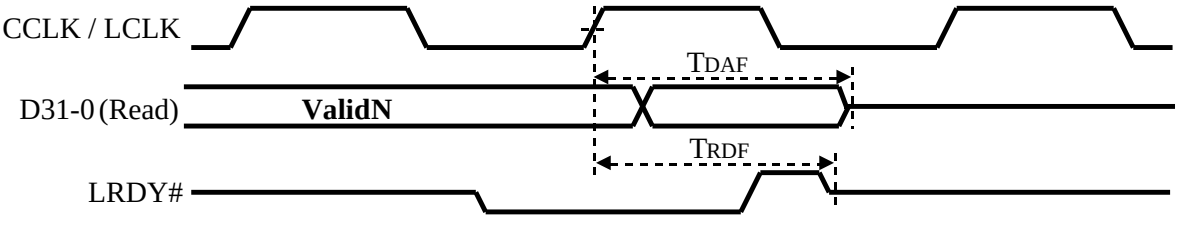
Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{DAV}	Bus Clock to Output Valid - D0-31 (Read)		125pF	3	18	nS
T_{RDV}	Bus Clock to Output Valid - LRDY#		100pF	3	14	nS



Local Bus Output Valid Timing

65540/65545 AC TIMING CHARACTERISTICS - LOCAL BUS FLOAT DELAY (33MHz)

Symbol	Parameter	Notes	C_L Max	Min	Max	Units
T_{DAF}	Float Delay - D0-31 (Read)		125pF	–	20	nS
T_{RDF}	Float Delay - LRDY#	Driven high before floating	100pF	–	30	nS

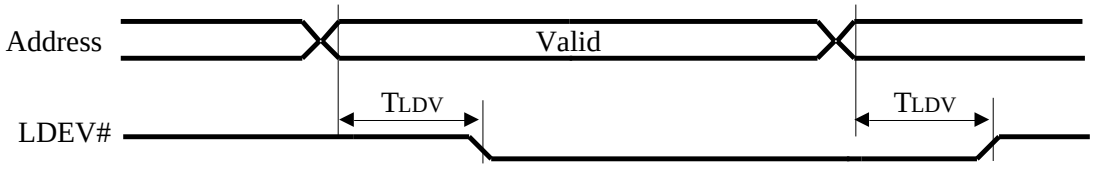


Local Bus Output Float Delay Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - VL-BUS LDEV#

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{LDV}	Address to LDEV# change		3	–	20	nS



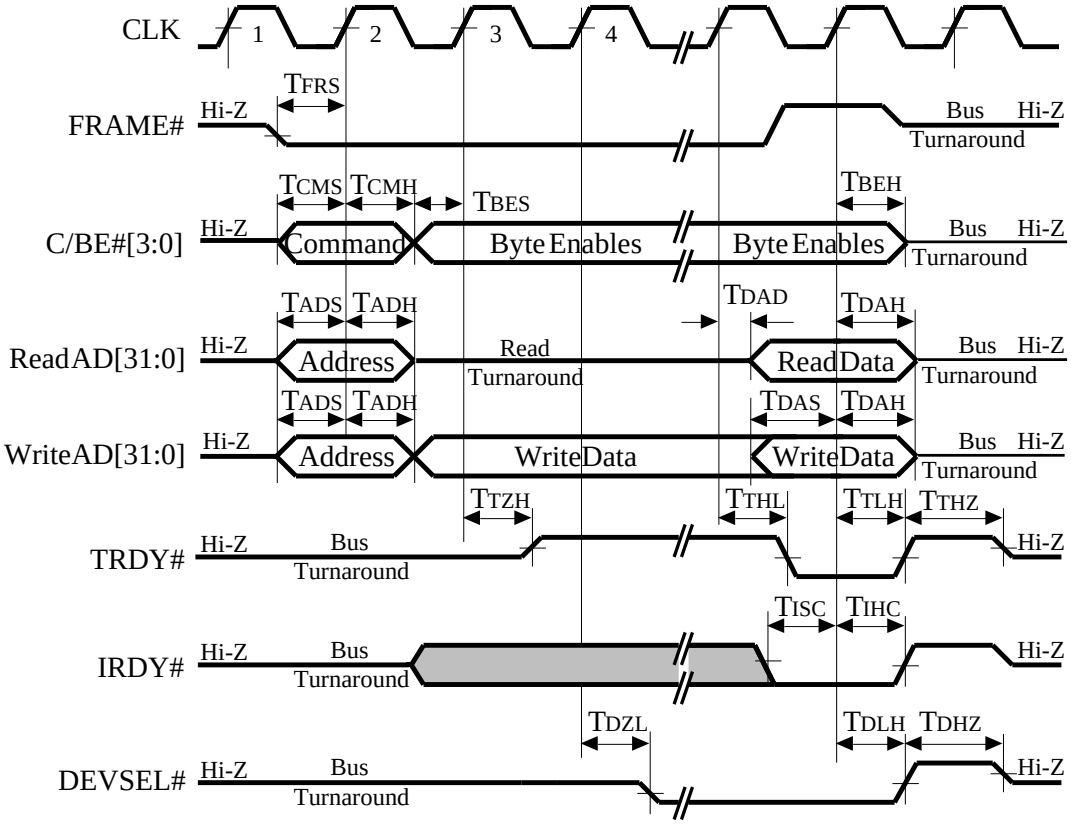
VL-Bus LDEV# Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 545 AC TIMING CHARACTERISTICS - PCI BUS FRAME

Symbol	Parameter	Notes	Min	Max	Units
T_{FRS}	FRAME# Setup to CLK		7	–	nS
T_{CMS}	C/BE#[3:0] (Bus CMD) Setup to CLK		7	–	nS
T_{CMH}	C/BE#[31:0] (Bus CMD) Hold from CLK		2	–	nS
T_{BES}	C/BE#[3:0] (Byte Enable) Setup to CLK		7	–	nS
T_{BEH}	C/BE#[3:0] (Byte Enable) Hold from CLK		2	–	nS
T_{ADS}	AD[31:0] (Address) Setup to CLK		7	–	nS
T_{ADH}	AD[31:0] (Address) Hold from CLK		2	–	nS
T_{DAD}	AD[31:0] (Data) Valid from CLK	Read Cycles	–	11	nS
T_{DAS}	AD[31:0] (Data) Setup to CLK	Write Cycles	7	–	nS
T_{DAH}	AD[31:0] (Data) Hold from CLK		2	–	nS
T_{TZH}	TRDY# High Z to High from CLK		–	11	nS
T_{THL}	TRDY# Active from CLK		–	11	nS
T_{TLH}	TRDY# Inactive from CLK		–	11	nS
T_{THZ}	TRDY# High before High Z		1	1	**CLK**
T_{DZL}	DEVSEL# Active from CLK		–	11	nS
T_{DLH}	DEVSEL# Inactive from CLK		–	11	nS
T_{DHZ}	DEVSEL# High before High Z		1	1	**CLK**
T_{ISC}	IRDY# Setup to CLK		7	–	nS
T_{IHC}	IRDY# Hold from CLK		2	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.



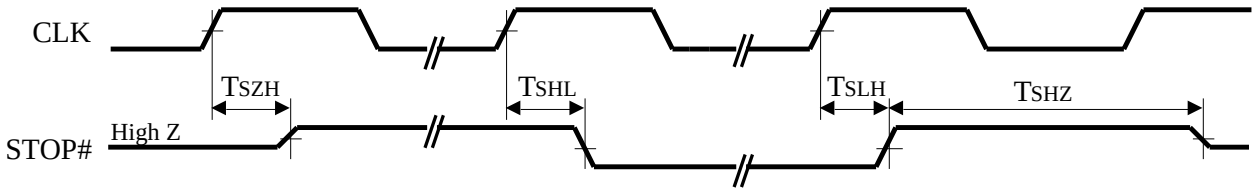
PCI Bus Frame Timing

Note: The above diagram shows a typical PCI bus cycle. PCI bus read cycles require a bus turn-around cycle between address output and data input on AD31:0. PCI bus write cycles do not require this bus turnaround cycle so the write data is available from the bus master immediately after address output (in clock cycle 2 instead of clock cycle 3).

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 545 AC TIMING CHARACTERISTICS - PCI BUS STOP

Symbol	Parameter	Notes	Min	Max	Units
T_{SZH}	STOP# High Z to High from CLK		–	11	nS
T_{SHL}	STOP# Active from CLK		–	11	nS
T_{SLH}	STOP# Inactive from CLK		–	11	nS
T_{SHZ}	STOP# High before High Z		1	1	CLK

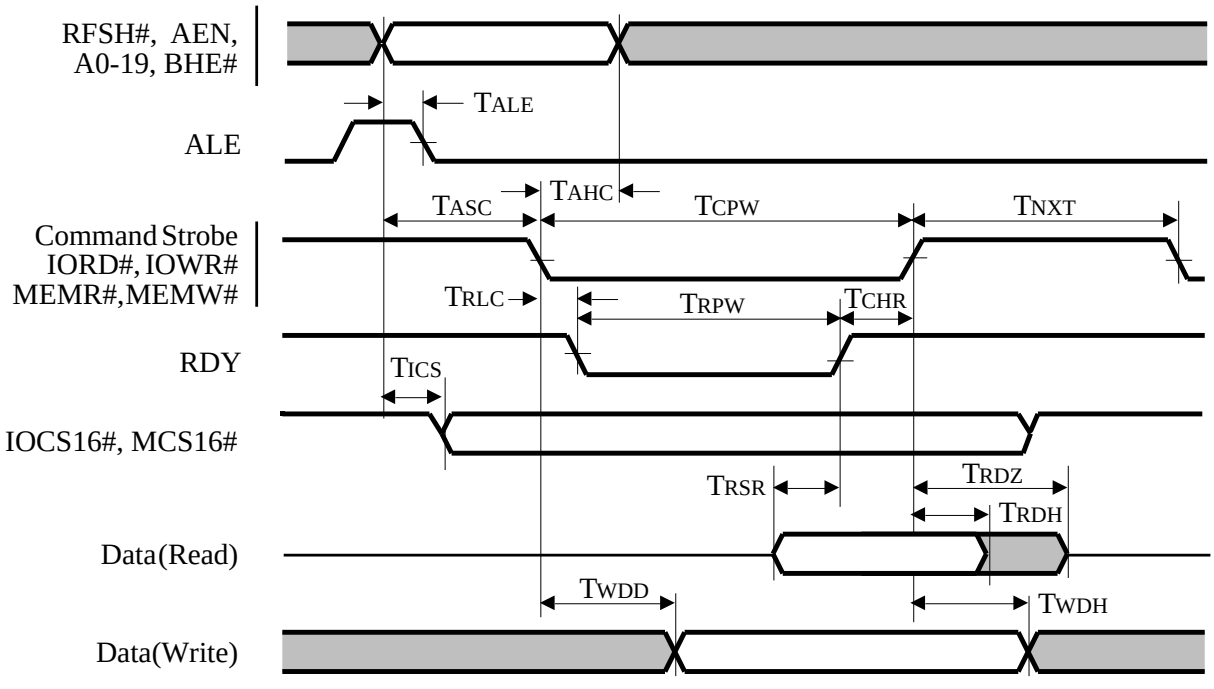


PCI Bus Stop Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - ISA BUS

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width		6Tm	–	–	nS
T_{CHR}	Command Strobe Hold from Ready		0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		3Tm	–	–	nS
T_{ALE}	Address Setup to ALE Inactive		29	–	–	nS
T_{ASC}	Address Setup to Command Strobe		30	–	–	nS
T_{ICS}	Address to IOCS16# & MEMCS16# Delay		–	–	2Tm	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	100Tm	nS
T_{AHC}	Address Hold to Command Strobe		20	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		10	–	–	nS
T_{RDZ}	Read Data Tri-Stated from Command Strobe		–	–	30	nS
T_{WDD}	Write Data Delay from Command Strobe		–	–	20	nS
T_{WDH}	Write Data Hold from Command Strobe		10	–	–	nS
T_{RLC}	RDY Low Delay from Command Strobe **(+5V)**	Mem Accesses Only	–	–	40	nS
T_{RLC}	RDY Low Delay from Command Strobe **(+3.3V)**	Mem Accesses Only	–	–	55	nS



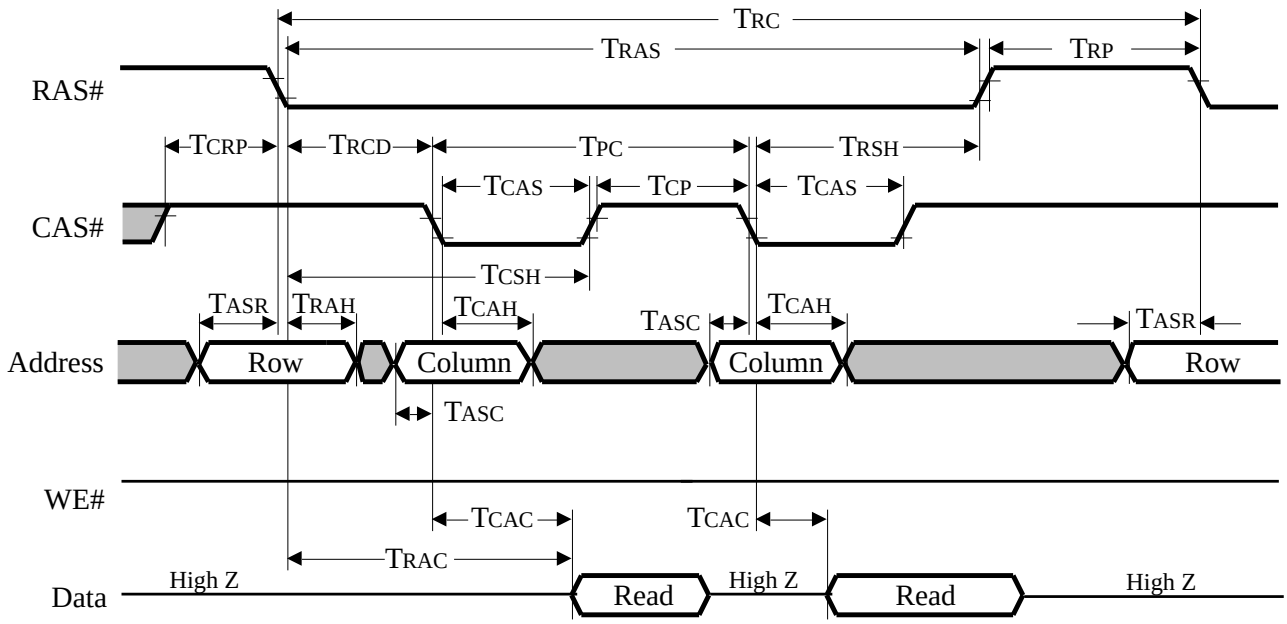
ISA Bus Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

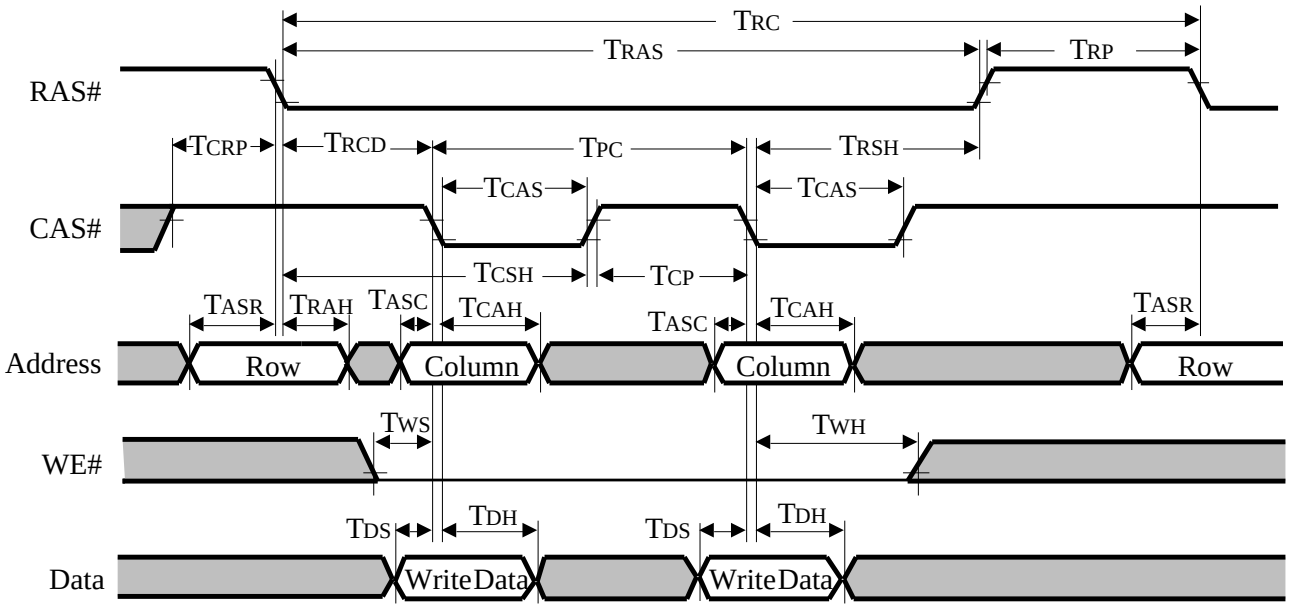
65540/65545 AC TIMING CHARACTERISTICS - DRAM READ/WRITE

Symbol	Parameter	Notes	Min	Max	Units
T_{RC}	Read/Write Cycle Time		12Tm – 5	–	nS
T_{RAS}	RAS# Pulse Width		8Tm – 5	–	nS
T_{RP}	RAS# Precharge		4Tm – 3	–	nS
T_{CRP}	CAS# to RAS# Precharge		4Tm – 5	–	nS
T_{CSH}	CAS# Hold from RAS#		5Tm – 2	–	nS
T_{RCD}	RAS# to CAS# Delay		3Tm – 5	–	nS
T_{RSH}	RAS# Hold from CAS#		2Tm – 5	–	nS
T_{CP}	CAS# Precharge		Tm – 5	–	nS
T_{CAS}	CAS# Pulse Width		2Tm – 5	–	nS
T_{ASR}	Row Address Setup to RAS#		Tm – 5	–	nS
T_{ASC}	Column Address Setup to CAS#		2Tm – 8	–	nS
T_{RAH}	Row Address Hold from RAS#		Tm – 2	–	nS
T_{CAH}	Column Address Hold from CAS#		Tm – 2	–	nS
T_{CAC}	Data Access Time from CAS#	XR05[2-1]=0 (3MCLK CAS Cycle)	–	2Tm – 5	nS
		XR05[2-1]=1 (4MCLK CAS Cycle)	–	3Tm – 5	nS
T_{RAC}	Data Access Time from RAS#	XR05[2-1]=0 (3MCLK CAS Cycle)	–	5Tm – 2	nS
		XR05[2-1]=1 (4MCLK CAS Cycle)	–	6Tm – 2	nS
T_{DS}	Write Data Setup to CAS#		Tm – 5	–	nS
T_{DH}	Write Data Hold from CAS#		Tm – 2	–	nS
T_{PC}	CAS Cycle Time		3Tm – 1	–	nS
T_{WS}	WE# Setup to CAS#		1Tm – 5	–	nS
T_{WH}	WE# Hold from CAS#		2Tm – 5	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.



DRAM Page Mode Read Cycle Timing



DRAM Page Mode Write Cycle Timing

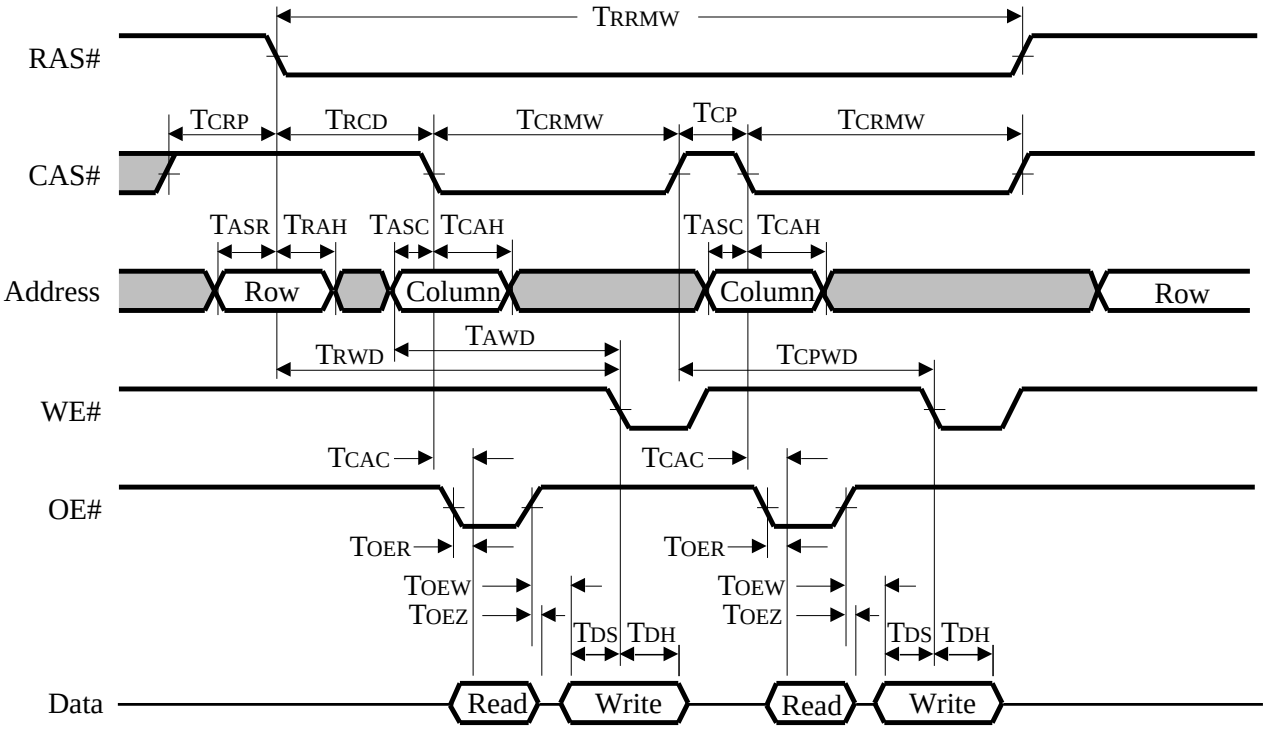
Note: The above diagrams represent typical page mode cycles. The number of actual CAS cycles may vary.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65545 AC TIMING CHARACTERISTICS - DRAM READ/MODIFY/WRITE

Symbol	Parameter	Notes	Min	Max	Units
T_{RRMW}	RAS# Pulse Width		16Tm – 5	–	nS
T_{CRMW}	CAS# Pulse Width		6Tm – 5	–	nS
T_{AWD}	Col Address to WE# Delay		6Tm – 8	–	nS
T_{RWD}	RAS# to WE# Delay		7Tm – 5	–	nS
T_{CPWD}	CAS# Precharge to WE# Delay		5Tm – 5	–	nS
T_{OEZ}	Output Turnoff Delay from OE#		–	Tm	nS
T_{OEW}	OE# Write Data Delay		Tm + 3	–	nS
T_{OER}	OE# Read Data Delay	XR05[1] = 0 (3 MCLK CAS Cycle)	–	2Tm – 5	nS
T_{OER}	OE# Read Data Delay	XR05[1] = 1 (4 MCLK CAS Cycle)	–	3Tm – 5	nS

Note: Read Modify Write timing for 65545 only.



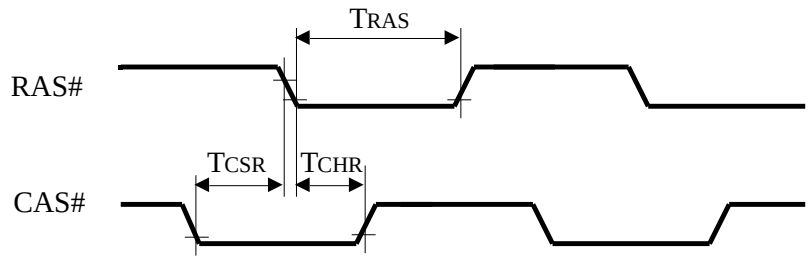
DRAM Page Mode Read Modify Write Cycle Timing

Note: The above diagrams represent typical page mode cycles. The number of actual CAS cycles may vary.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 65545 AC TIMING CHARACTERISTICS - CBR REFRESH

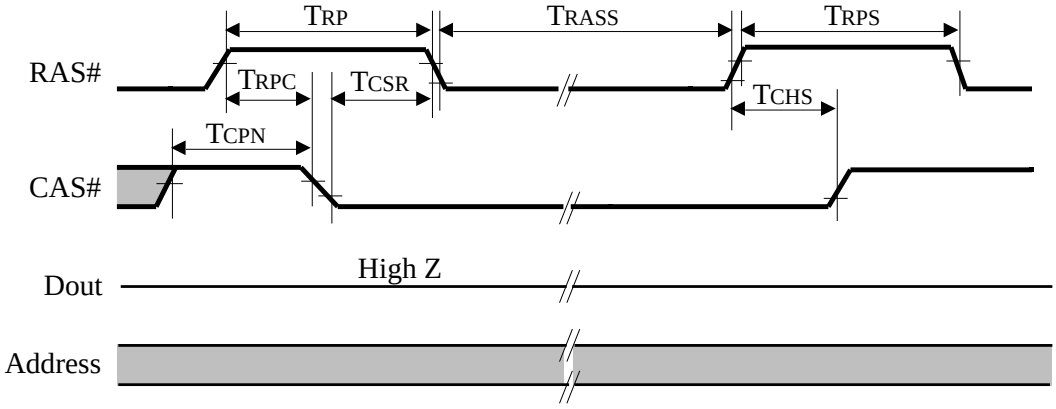
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS# to CAS# Delay	Tm = 15.4 @ 65 MHz	5Tm – 5	–	–	nS
T_{CSR}	CAS# to RAS# Delay	Normal Operation	Tm – 5	–	–	nS
		Standby Mode	2Tm – 5	–	–	nS
T_{RAS}	RAS# Pulse Width	5Tm = 89 ns (56 MHz) or 77 ns (65 MHz)	5Tm – 5	–	–	nS



CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

65540/65545 AC TIMING CHARACTERISTICS - SELF REFRESH

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RASS}	RAS# Pulse Width for Self-Refresh		100	–	–	µS
T_{RP}	RAS# Precharge		4Tm – 3	–	–	nS
T_{RPS}	RAS# Precharge for Self-Refresh		10Tm	–	–	nS
T_{RPC}	RAS# to CAS# Delay		3Tm – 5	–	–	nS
T_{CSR}	CAS# to RAS# Delay	Normal Operation	Tm – 5	–	–	nS
		Standby Mode	2Tm – 5	–	–	nS
T_{CHS}	CAS# Hold Time		0	–	–	nS
T_{CPN}	CAS# Precharge		Tm – 5	–	–	nS



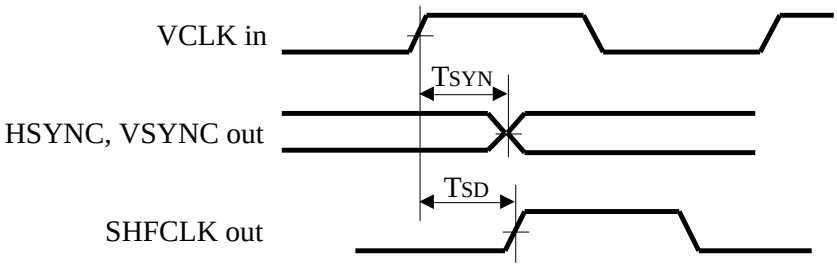
'Self-Refresh DRAM' Refresh Cycle Timing

Note: Upon exiting self-refresh mode, the 65540 / 65545 will perform a complete set of CBR refresh cycles before resuming normal DRAM activity. The duration of the burst refresh will equal the panel power sequencing delay, programmed in XR5B bits 7-4.

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540/545 AC TIMING CHARACTERISTICS - CRT OUTPUT TIMING

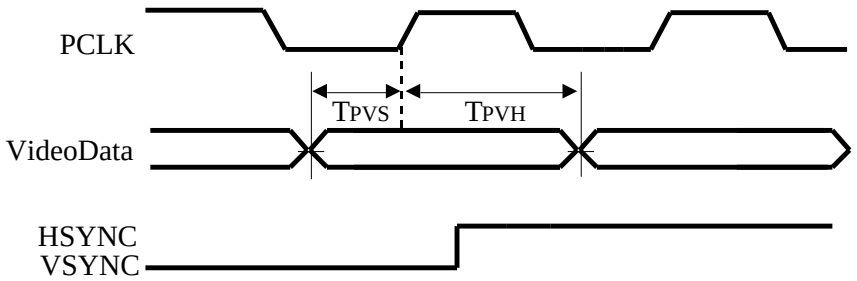
Symbol	Parameter	Notes	Min	Max	Units
T_{SYN}	HSYNC, VSYNC delay from VCLK in		–	50	nS
T_{SYN}	HSYNC, VSYNC delay from VCLK in **(3.3V)**		–	80	nS
T_{SD}	VCLK in to SHFCLK delay		–	30	nS
T_{SD}	VCLK in to SHFCLK delay **(3.3V)**		–	50	nS



CRT Output Timing

65540/545 AC TIMING CHARACTERISTICS - PC VIDEO TIMING

Symbol	Parameter	Notes	Min	Max	Units
T_{PVS}	Video Data setup to PCLK		12	–	nS
T_{PVH}	Video Data hold to PCLK		0	–	nS

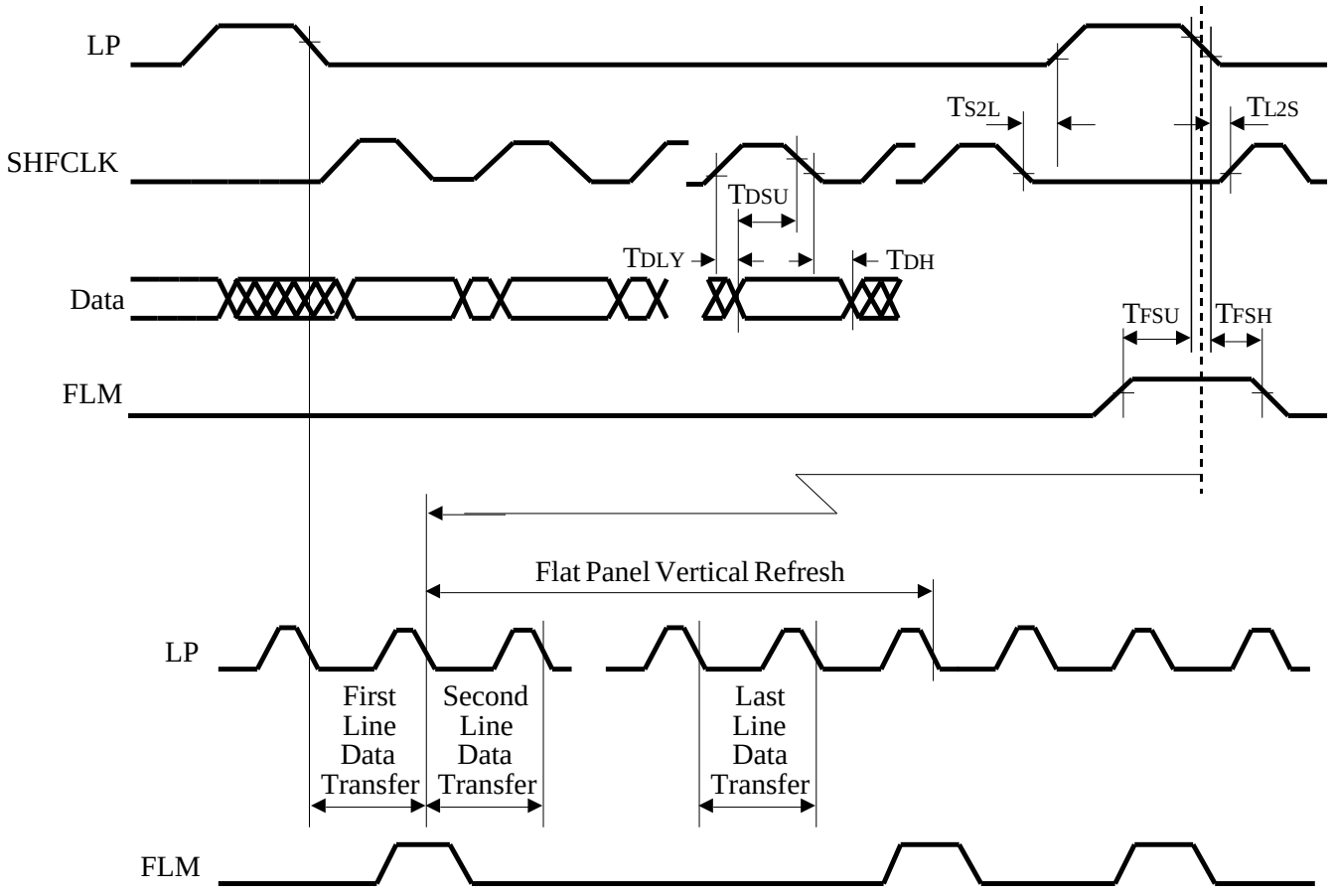


PC Video Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

65540 / 545 AC TIMING CHARACTERISTICS - PANEL OUTPUT TIMING

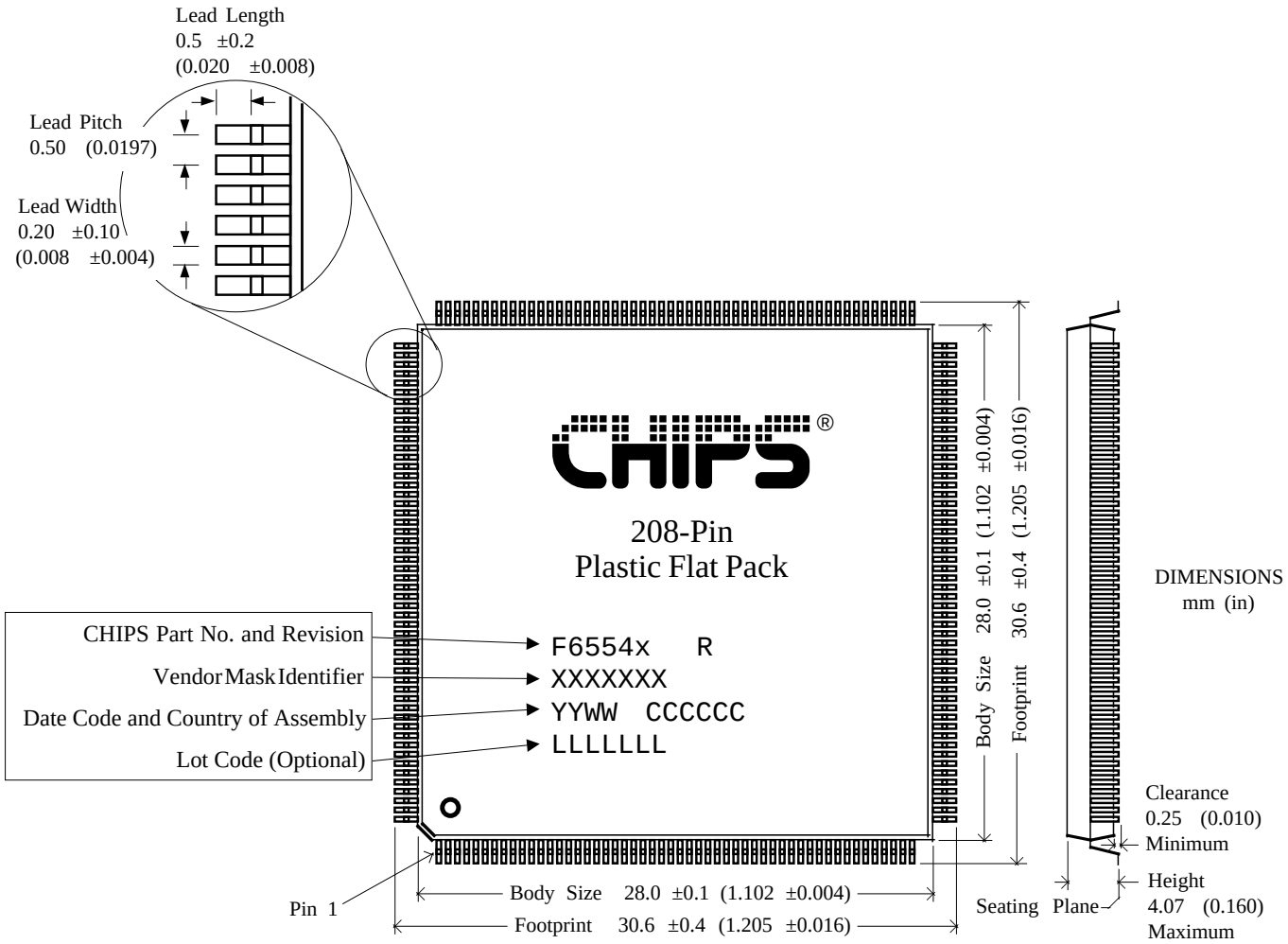
Symbol	Parameter	Notes	Min	Max	Units
T_{DSU}	Panel Data Setup to SHFCLK		5	–	nS
T_{DH}	Panel Data Hold to SHFCLK		10	–	nS
T_{DLY}	Panel Data Delay from SHFCLK		10	–	nS
T_{L2S}	SHFCLK Allowance Time from LP		Tc	–	nS
T_{S2L}	LP Allowance Time from SHFCLK		Tc	–	nS
T_{FSU}	FLM Setup Time		8 Tc	–	nS
T_{FSH}	FLM Hold Time		8 Tc	–	nS



Panel Output Timing

Note: Unless otherwise specified, specifications above apply to both 5V & 3.3V operation & memory clock is assumed to be 68MHz. Electrical specifications contained herein are preliminary and subject to change without notice.

Mechanical Specifications



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