CMOS Digital Integrated Circuits Silicon Monolithic

74HC573D

1. Functional Description

- Octal D-Type Latch with 3-State Outputs

2. General

The 74HC573D is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

3. Features

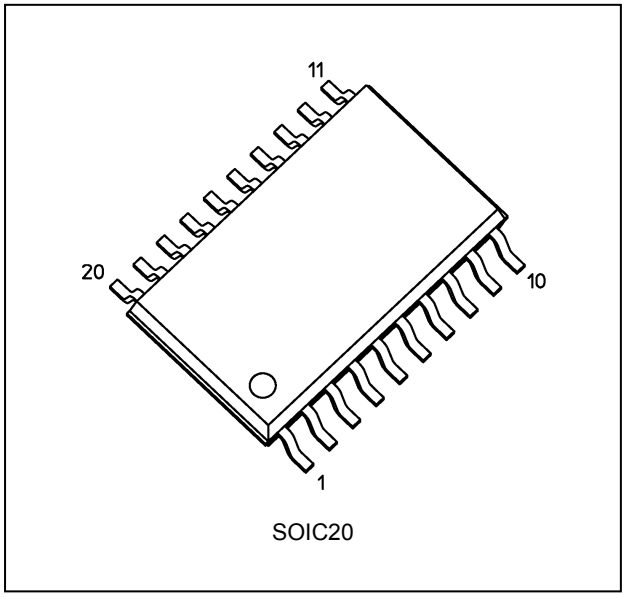
(1) High speed: t_{pd} = 13 ns (typ.) at V_{CC} = 6.0 V

(2) Low power dissipation: I_{CC} = 4.0 μA (max) at T_a = 25 °C

(3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(4) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 6.0 V

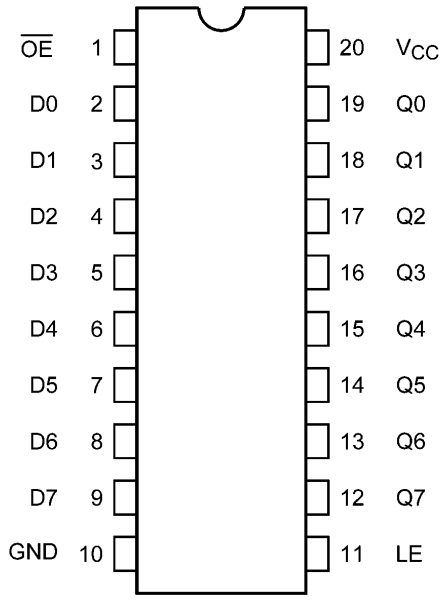
4. Packaging



SOIC20

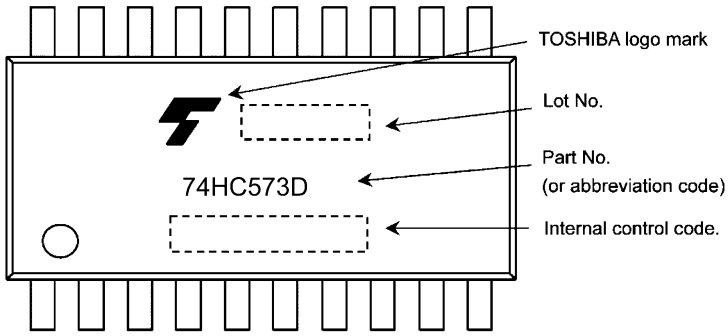
Start of commercial production
2016-03

5. Pin Assignment

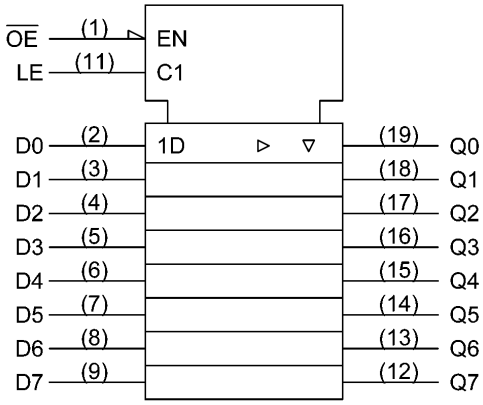


(top view)

6. Marking



7. IEC Logic Symbol

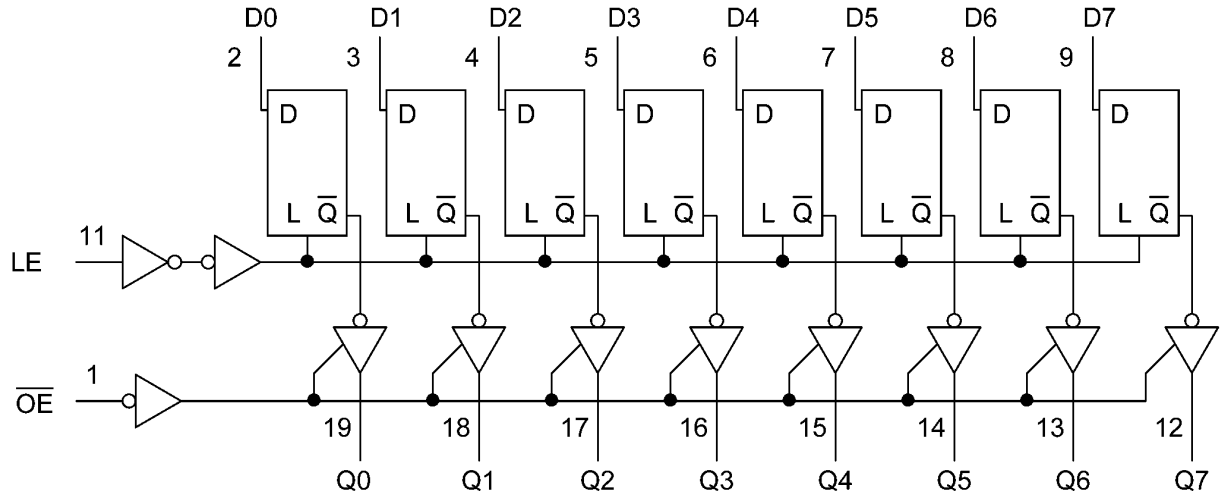


8. Truth Table

INPUT $\overline{OE}$	INPUT LE	INPUT D	OUTPUT Q
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't Care
Z: High Impedance
Qn: Q outputs are latched at the time when the LE input is taken to low logic level.

9. System Diagram



10. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		±20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±35	mA
V_{CC}/ground current	I_{CC}		±75	mA
Power dissipation	P_D	(Note 1)	500	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: P_D derates linearly with -8 mW/°C above 85°C

11. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 6.0	V
Input voltage	V_{IN}		0 to V_{CC}	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 85	°C
Input rise and fall times	t_r,t_f	V_{CC} = 2.0 V	0 to 1000	ns
		V_{CC} = 4.5 V	0 to 500	
		V_{CC} = 6.0 V	0 to 400	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

12. Electrical Characteristics

12.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				4.5	3.15	—	—	V
				6.0	4.20	—	—	V
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				4.5	—	—	1.35	V
				6.0	—	—	1.80	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	V
				4.5	4.4	4.5	—	
				6.0	5.9	6.0	—	
			I_{OH} = -6 mA	4.5	4.18	4.31	—	
			I_{OH} = -7.8 mA	6.0	5.68	5.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	V
				4.5	—	0.0	0.1	
				6.0	—	0.0	0.1	
			I_{OL} = 6 mA	4.5	—	0.17	0.26	
			I_{OL} = 7.8 mA	6.0	—	0.18	0.26	V
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	—	±0.5	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND I_O = 0 A		6.0	—	—	4.0	μA

12.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				4.5	3.15	—	
				6.0	4.20	—	V
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				4.5	—	1.35	
				6.0	—	1.80	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	—	V
				4.5	4.4	—	
				6.0	5.9	—	
			I_{OH} = -6 mA	4.5	4.13	—	
			I_{OH} = -7.8 mA	6.0	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.1	V
				4.5	—	0.1	
				6.0	—	0.1	
			I_{OL} = 6 mA	4.5	—	0.33	
			I_{OL} = 7.8 mA	6.0	—	0.33	V
3-state output OFF-state leakage current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND I_O = 0 A		6.0	—	40.0	μA

12.3. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (LE)	$t_{w(H)}$	—	2.0	75	ns
			4.5	15	
			6.0	13	
Minimum setup time	t_S	—	2.0	50	ns
			4.5	10	
			6.0	9	
Minimum hold time	t_h	—	2.0	5	ns
			4.5	5	
			6.0	5	

12.4. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (LE)	$t_{w(H)}$	—	2.0	95	ns
			4.5	19	
			6.0	16	
Minimum setup time	t_S	—	2.0	65	ns
			4.5	13	
			6.0	11	
Minimum hold time	t_h	—	2.0	5	ns
			4.5	5	
			6.0	5	

12.5. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	2.0	50	—	20	60	ns
				4.5		—	6	12	
				6.0		—	5	10	
Propagation delay time (LE-Q)	t_{PLH},t_{PHL}		—	2.0	50	—	50	115	ns
				4.5		—	15	23	
				6.0		—	13	20	
				2.0	150	—	60	155	ns
				4.5		—	20	31	
				6.0		—	17	26	
Propagation delay time (D-Q)	t_{PLH},t_{PHL}		—	2.0	50	—	42	110	ns
				4.5		—	14	22	
				6.0		—	12	19	
				2.0	150	—	57	150	ns
				4.5		—	19	30	
				6.0		—	16	26	
Output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	2.0	50	—	55	140	ns
				4.5		—	17	28	
				6.0		—	14	24	
				2.0	150	—	66	180	ns
				4.5		—	22	36	
				6.0		—	19	31	
Output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	2.0	50	—	40	125	ns
				4.5		—	17	25	
				6.0		—	15	21	
Input capacitance	C_{IN}		—			—	5	10	pF
Output capacitance	C_{OUT}		—			—	10	—	pF
Power dissipation capacitance	C_{PD}	(Note 1)	—			—	51	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per latch)

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

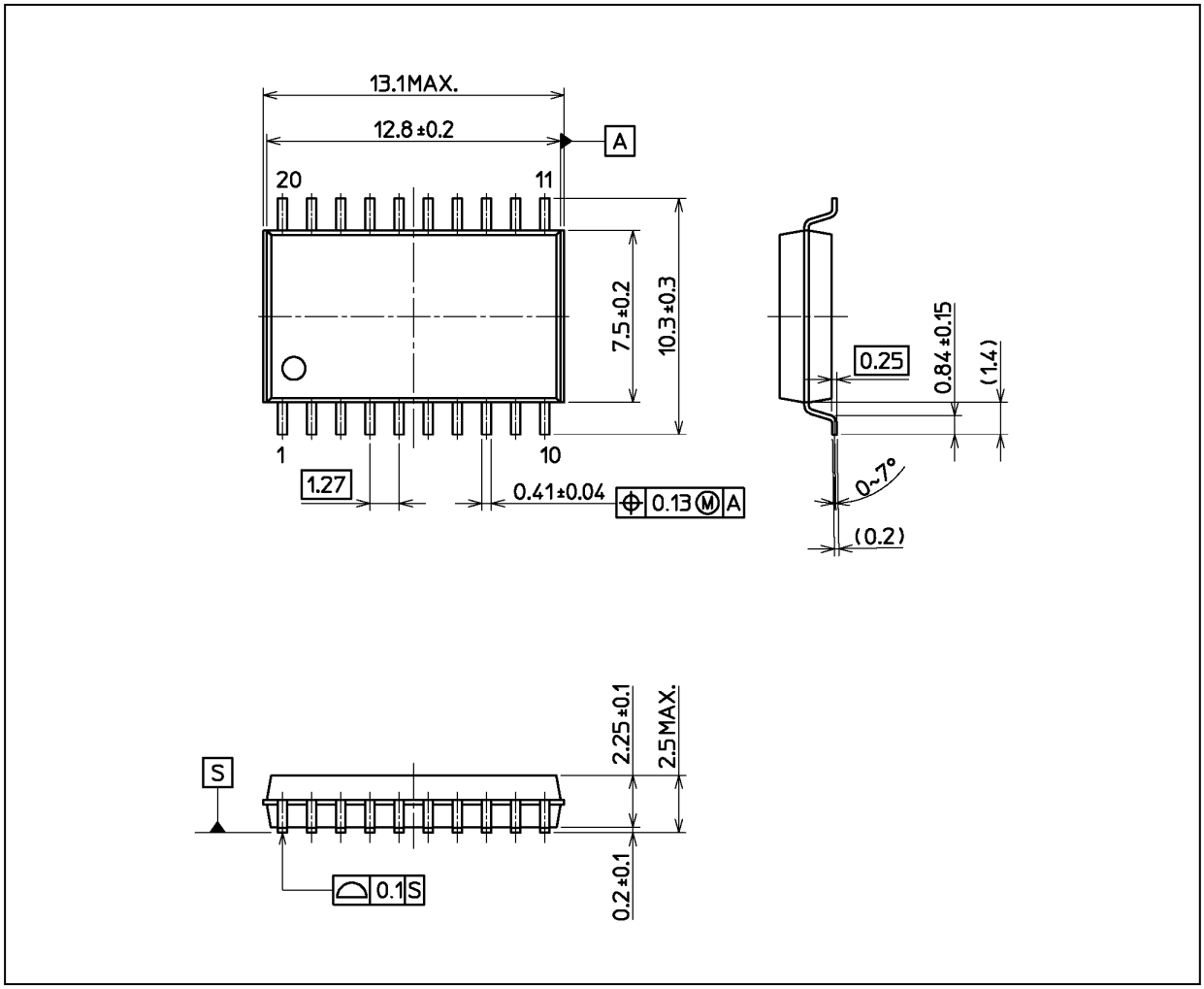
C_{PD} (total) = 33 + 18 × n

12.6. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Output transition time	t_{TLH},t_{THL}		—	2.0	50	—	75	ns
				4.5		—	15	
				6.0		—	13	
Propagation delay time (LE-Q)	t_{PLH},t_{PHL}		—	2.0	50	—	145	ns
				4.5		—	29	
				6.0		—	25	
				2.0	150	—	195	ns
				4.5		—	39	
				6.0		—	33	
Propagation delay time (D-Q)	t_{PLH},t_{PHL}		—	2.0	50	—	140	ns
				4.5		—	28	
				6.0		—	24	
				2.0	150	—	190	ns
				4.5		—	38	
				6.0		—	32	
Output enable time	t_{PZL},t_{PZH}		R_L = 1 kΩ	2.0	50	—	175	ns
				4.5		—	35	
				6.0		—	30	
				2.0	150	—	225	ns
				4.5		—	45	
				6.0		—	38	
Output disable time	t_{PLZ},t_{PHZ}		R_L = 1 kΩ	2.0	50	—	155	ns
				4.5		—	31	
				6.0		—	26	
Input capacitance	C_{IN}		—			—	10	pF

Package Dimensions

Unit: mm



Weight: 0.51 g (typ.)

Package Name(s)
Nickname: SOIC20

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