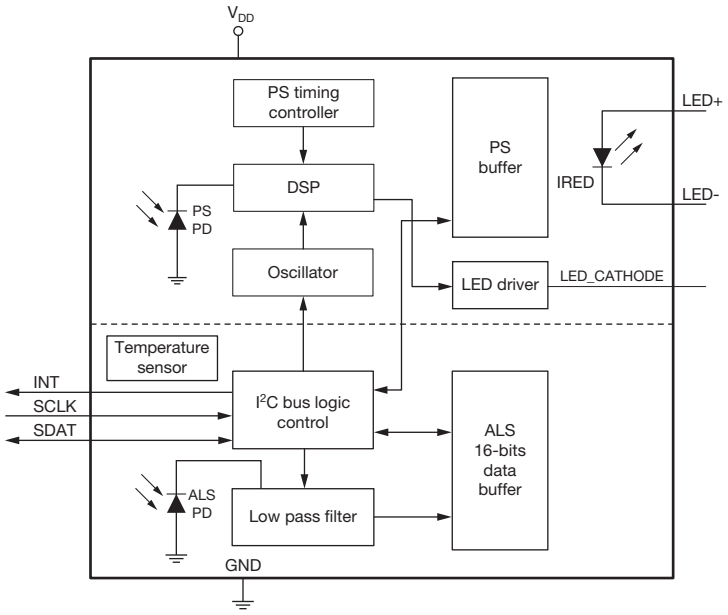
BLOCK DIAGRAM



BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)							
PARAMETER		**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Supply voltage			V_{DD}	2.5	-	3.6	V
Supply voltage for IRED			V_{IRED}	3.8	-	5.5	V
Supply current		Excluded LED driving	I_{DD}	-	350	-	µA
Shutdown current		Light condition = dark, V_{DD} = 3.3 V	I_{DD} (SD)	-	0.2	-	µA
ALS shut down		ALS disable, PS enable	I_{ALSSD}	-	300	-	µA
PS shut down		ALS enable, PS disable	I_{PSSD}	-	213	-	µA
I^2C signal input	Logic high	V_{DD} = 3.3 V	V_{IH}	1.5	-	-	V
	Logic low		V_{IL}	-	-	0.8	
	Logic high	V_{DD} = 2.6 V	V_{IH}	1.4	-	-	V
	Logic low		V_{IL}	-	-	0.6	
Peak sensitivity wavelength of ALS			λ_p	-	550	-	nm
Peak sensitivity wavelength of PS			λ_{pps}	-	940	-	nm
Full ALS counts		16-bit resolution		-	-	65 535	steps
Full PS counts		12-bit / 16-bit resolution		-	-	4095 / 65 535	steps
Detectable intensity	Minimum	IT = 400 ms, V_{DD} = 3.3 V, 1 step (1)(2)		-	0.003	-	lx
	Maximum	IT = 50 ms, V_{DD} = 3.3 V, 65 535 steps (1)(2)		-	1573	-	
ALS dark offset		IT = 50 ms, V_{DD} = 3.3 V, normal sensitivity (1)		0	-	3	steps
Operating temperature range			T_{amb}	-40	-	+85	°C
IRED driving current		(3)		-	-	800	mA

Notes

(1) Light source: white LED

(2) Maximum detection range to ambient light can be determined by ALS refresh time adjustment. Refer to table 17 “ALS Resolution and Maximum Detection Range”

(3) Based on IRED on / off duty ratio = 1/160, 1/320, 1/640, and 1/1280. The circuitry should use an external MOSFET as shown with Fig.11. Please see also the Application Note “Designing the VCNL4200 into an Application” (www.vishay.com/doc?84327)

I²C BUS TIMING CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**SYMBOL**	**STANDARD MODE**		**FAST MODE**		**UNIT**
		MIN.	**MAX.**	**MIN.**	**MAX.**	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	µs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	µs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	µs
Data hold time	$t_{(HDDAT)}$		3450	-	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I²C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	µs
I²C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	µs
Clock / data fall time	$t_{(F)}$	-	300	-	300	ns
Clock / data rise time	$t_{(R)}$	-	1000	-	300	ns

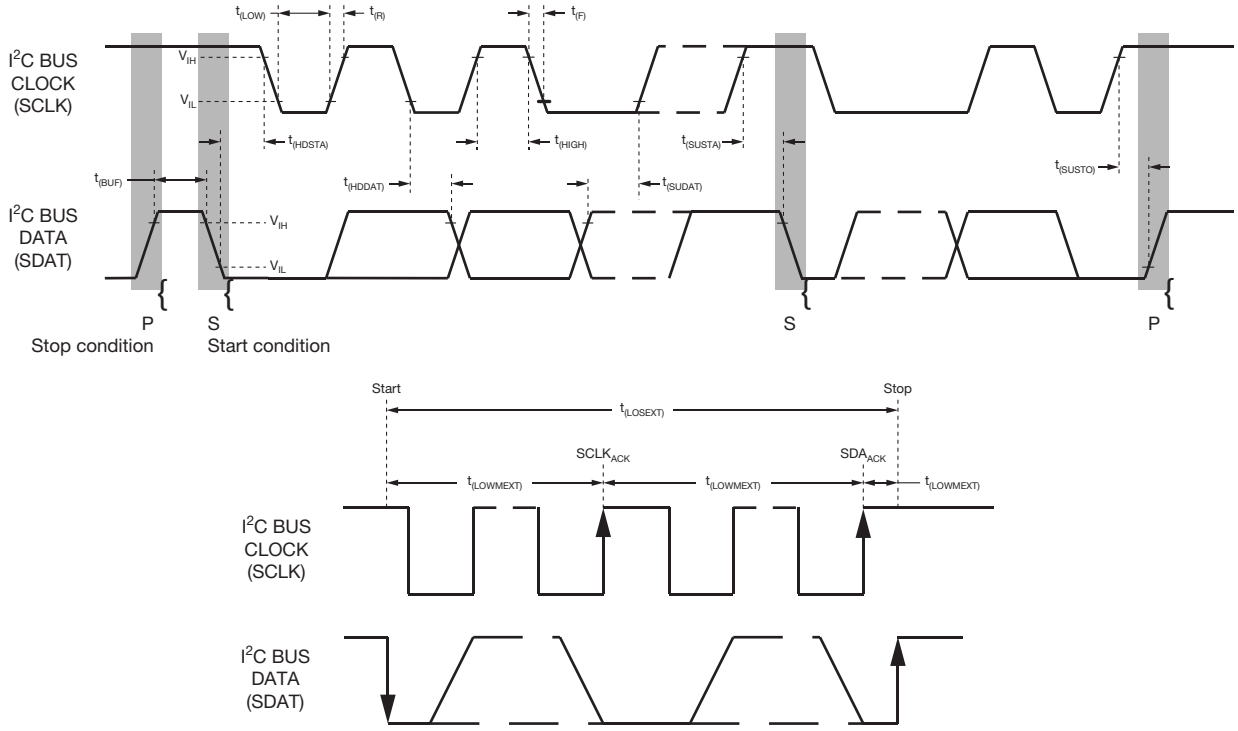


Fig. 1 - I²C Bus Timing Diagram