

TLP719

- Digital logic ground isolation
- Line receivers
- Microprocessor system interfaces
- Switching power supply feedback control
- Industrial invertors

The TOSHIBA TLP719 consists of a GaAlAs high-output light-emitting diode and a high-speed detector.

This unit is a 6-lead SDIP. The TLP719 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

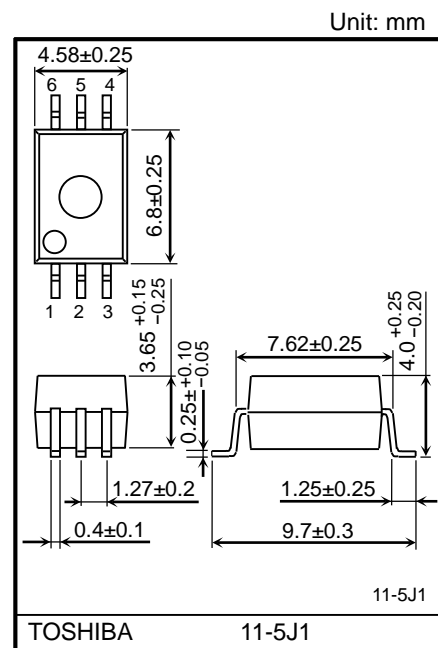
The TLP719 has a Faraday shield integrated on the photodetector chip to provide an effective common mode noise transient immunity. Therefore this product is suitable for application in noisy environmental conditions.

- Open collector
- Package type : SDIP6
- Isolation voltage : 5000 Vrms (min)
- Common mode transient immunity : ± 10 kV/ μ s (min) @ $V_{CM} = 400$ V
- Switching speed : $t_{PHL}/t_{PLH} = 0.8$ μ s (max)
@ $I_F = 16$ mA, $V_{CC} = 5$ V,
 $R_L = 1.9$ k Ω , $T_a = 25$ °C
- TTL compatible
- Construction mechanical rating

	7.62-mm pitch standard type	10.16-mm pitch TLPXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

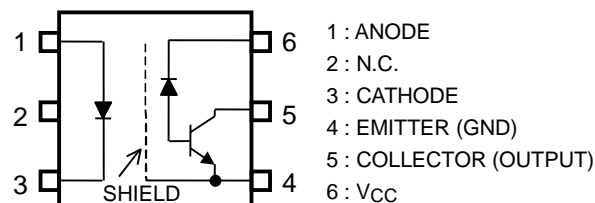
- UL recognized : UL1577, File No. E67349
- c-UL approved : CSA Component Acceptance Service
No. 5A, File No. E67349
- Option (D4) VDE approved : EN60747-5-5 (Note 1)

Note 1: When a EN60747-5-5 approved type is needed, please designate the "Option(D4)"

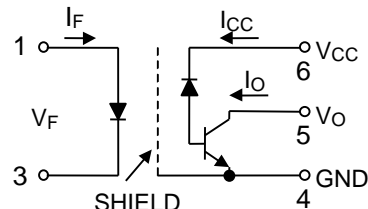


Weight: 0.26 g (typ.)

PIN CONFIGURATION (Top View)



SCHEMATIC



A 0.1- μ F bypass capacitor must be connected between pins 4 and 6.

Start of commercial production
2007-09

Absolute Maximum Ratings (Ta = 25 °C)

Characteristic		Symbol	Rating	Unit
LED	Forward current	I _F	25	mA
	Forward current derating (Ta ≥ 70 °C)	I _F / Ta	-0.45	mA / °C
	Pulse forward current (Note 1)	I _{FP}	50	mA
	Peak transient forward current (Note 2)	I _{FPT}	1	A
	Reverse voltage	V _R	5	V
	Diode power dissipation (Note 3)	P _D	45	mW
	Junction temperature	T _j	125	°C
Detector	Output current	I _O	8	mA
	Peak output current	I _{OP}	16	mA
	Output voltage	V _O	-0.5 to 20	V
	Supply voltage	V _{CC}	-0.5 to 30	V
	Output power dissipation	P _O	100	mW
	Output power dissipation derating (Ta ≥ 70 °C)	P _o / Ta	-1.8	mW / °C
	Junction Temperature	T _j	125	°C
Operating temperature range		T _{opr}	-55 to 100	°C
Storage temperature range		T _{stg}	-55 to 125	°C
Lead soldering temperature (10 s)		T _{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %)		BV _S	5000	V _{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note : A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high-gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: 50% duty cycle, 1 ms pulse width.
Derate 0.9 mA / °C above 70 °C.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: Derate 0.8 mW / °C above 70 °C.

Note 4: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Electrical Characteristics (Ta = 25 °C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
LED	Forward voltage	V _F	I _F = 16 mA	—	1.65	1.85	V
	Forward voltage Temperature coefficient	ΔV _F / ΔT _a	I _F = 16 mA	—	-2	—	mV / °C
	Reverse current	I _R	V _R = 5 V	—	—	10	μA
	Capacitance between terminals	C _T	V _F = 0 V, f = 1 MHz	—	45	—	pF
Detector	HIGH-level output current	I _{OH} (1)	I _F = 0 mA, V _{CC} = V _O = 5.5 V	—	3	500	nA
		I _{OH} (2)	I _F = 0 mA, V _{CC} = 30 V V _O = 20 V	—	—	5	μA
		I _{OH}	I _F = 0 mA, V _{CC} = 30 V V _O = 20 V, Ta = 70 °C	—	—	50	
	HIGH-level supply current	I _{CCH}	I _F = 0 mA, V _{CC} = 30 V	—	0.01	1	μA
	Supply voltage	V _{CC}	I _{CC} = 0.01 mA	30	—	—	V
	Output voltage	V _O	I _O = 0.5 mA	20	—	—	V

Coupled Electrical Characteristics (Ta = 25 °C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Current transfer ratio	I _O / I _F	I _F = 16 mA, V _{CC} = 4.5 V V _O = 0.4 V	20	—	—	%
LOW-level output voltage	V _{OL}	I _F = 16 mA, V _{CC} = 4.5 V I _O = 2.4 mA	—	—	0.4	V

Isolation Characteristics (Ta = 25 °C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Capacitance input to output	C _S	V = 0 V, f = 1 MHz (Note 1)	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60%, V _S = 500 V (Note 1)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s	5000	—	—	V _{rms}
		AC, 1 s, in oil	—	10000	—	
		DC, 60 s, in oil	—	10000	—	V _{dc}

Note 1: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Switching Characteristics (Ta = 25 °C, Vcc = 5 V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	tpHL	Fig1	IF = 0→16 mA RL = 1.9kΩ	—	—	0.8	μs
Propagation delay time (L→H)	tpLH		IF = 16→0 mA RL = 1.9kΩ	—	—	0.8	μs
Common mode transient immunity at logic HIGH output (Note 1)	CMH	Fig2	IF = 0 mA VCM = 400 Vp-p RL = 1.9kΩ	10000	—	—	V / μs
Common mode transient immunity at logic LOW output (Note 1)	CML		IF = 16 mA VCM = 400 Vp-p RL = 1.9 kΩ	-10000	—	—	V / μs

Note 1 : CML is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic LOW state (VO < 0.8 V).

CMH is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic HIGH state (VO > 2.0 V).

Figure 1. Switching Time Test Circuit

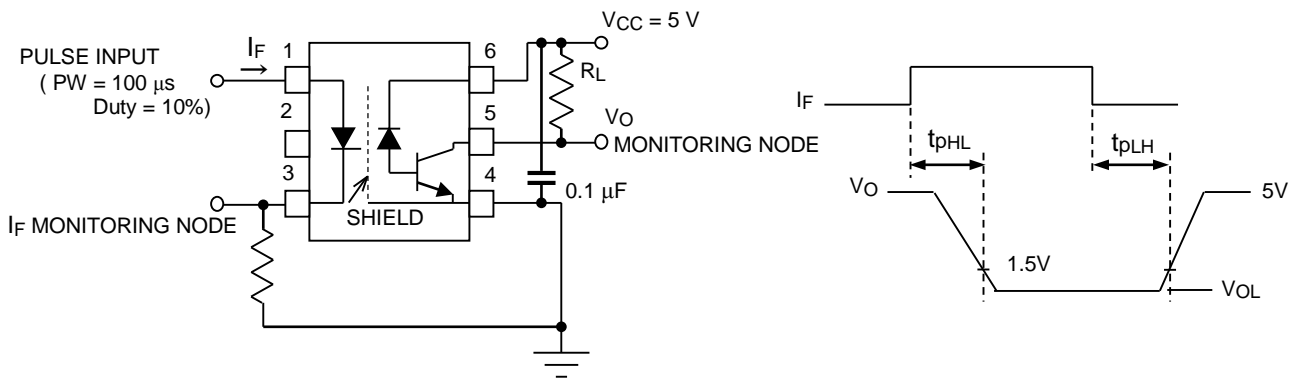
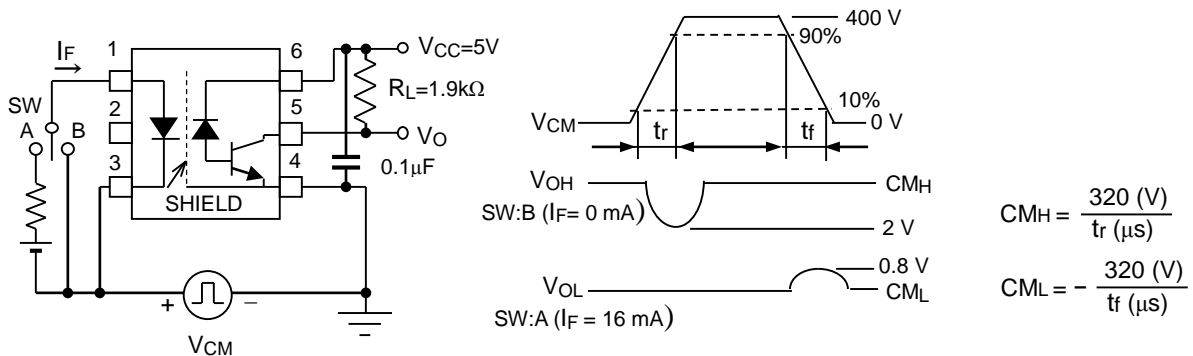
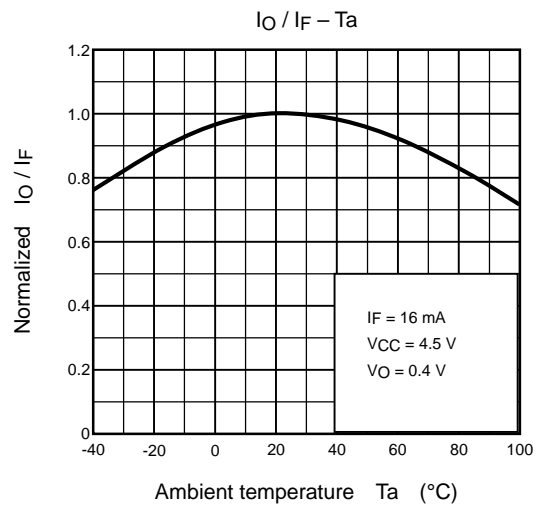
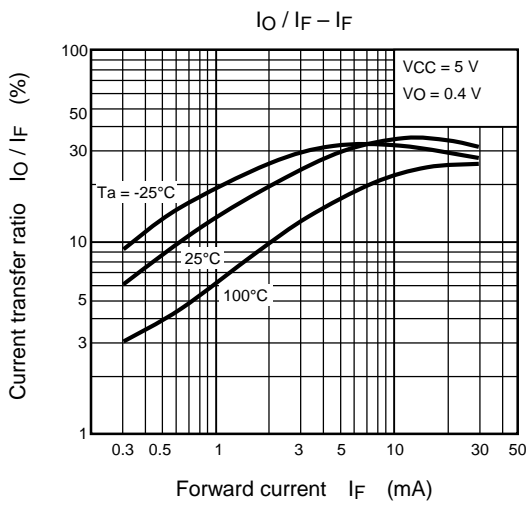
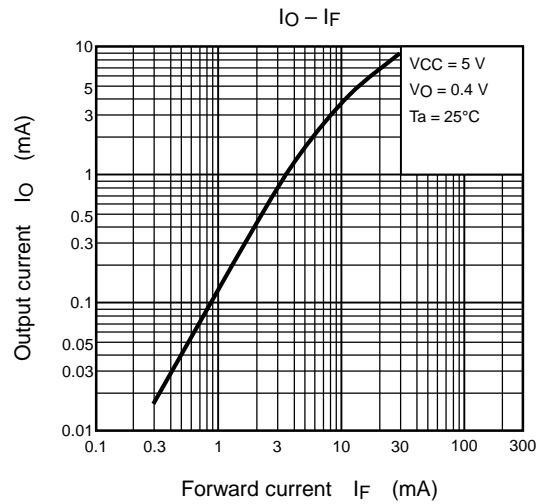
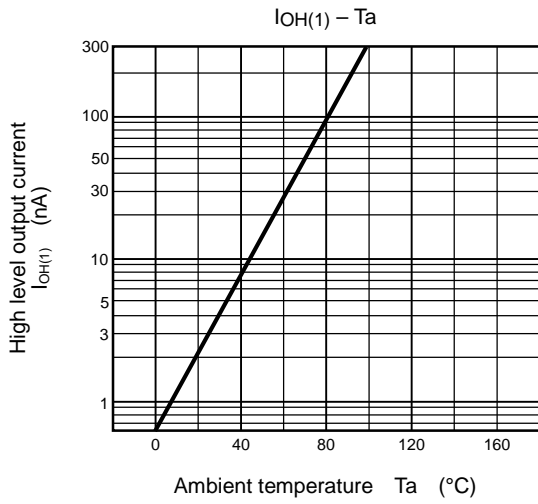
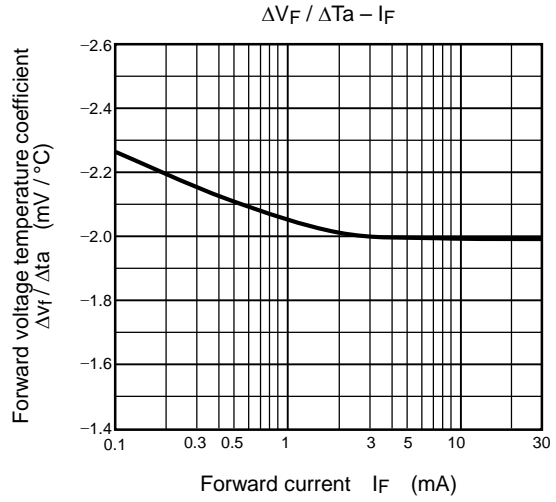
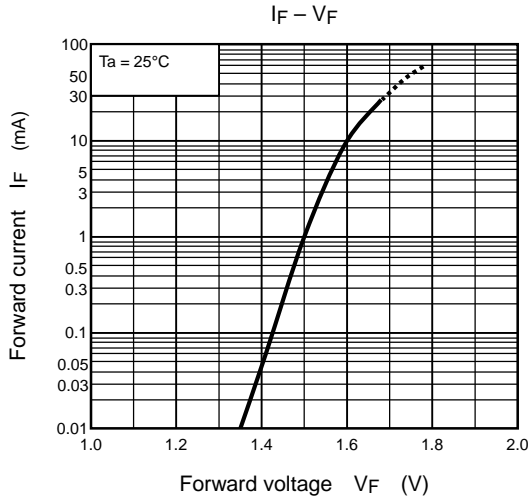
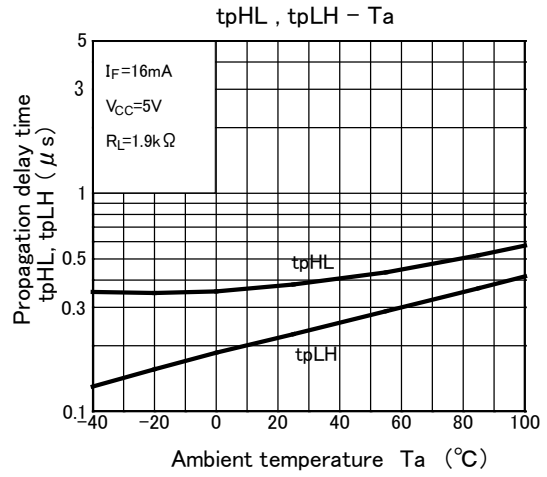
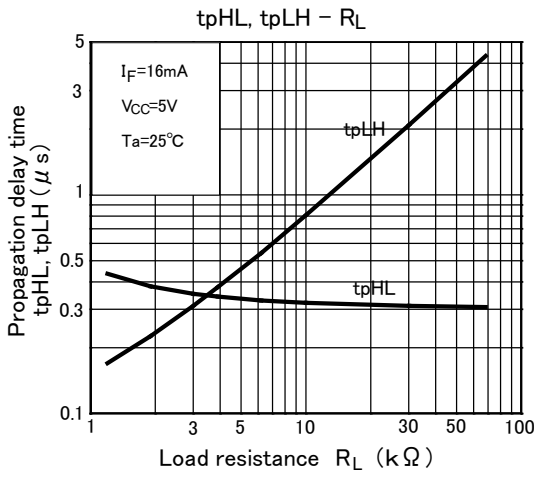
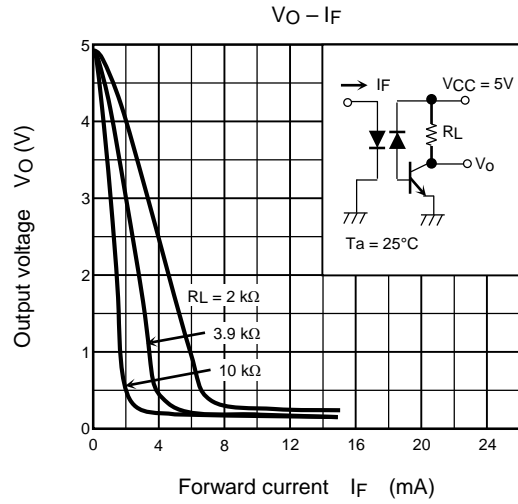
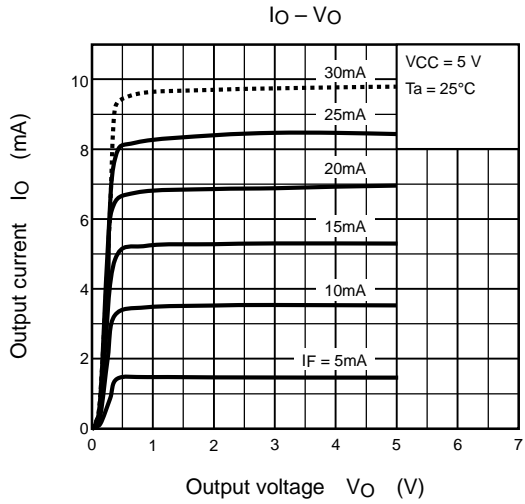


Figure 2. Common Mode Noise Immunity Test Circuit.







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