

## Absolute Maximum Ratings

VDD to GND	+4.0V
I <sup>2</sup> C Bus (SCL, SDA) Pin Voltage	-0.2V to 4.0V
I <sup>2</sup> C Bus (SCL, SDA) Pin Current	<10mA
Input Voltage Slew Rate (Maximum)	0.1V/μs
ESD Ratings	
Human Body Model	3kV

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)
4 Ld ODFN Package (Note 4)	287
Maximum Junction Temperature (T <sub>JMAX</sub> )	+90°C
Storage Temperature Range	-40°C to +100°C
Operating Temperature	40°C to +85°C
Pb-Free Reflow Profile	see <a href="#">TB477</a>

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.

## Electrical Specifications $V_{DD} = 3.0V, T_A = +25^\circ C$ , 16-bit ADC operation, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Power Supply Range	V <sub>DD</sub>		2.25		3.63	V
Supply Current	I <sub>DD</sub>			57	85	μA
Supply Current when Powered Down	I <sub>DD1</sub>	Software disabled or auto power-down		0.24	0.51	μA
Supply Voltage Range for I <sup>2</sup> C Interface	V <sub>I2C</sub>		1.70		3.63	V
ADC Integration/Conversion Time	t <sub>int</sub>	16-bit ADC data		105		ms
I <sup>2</sup> C Clock Rate Range	F <sub>I2C</sub>			400		kHz
Count Output When Dark	DATA_0	E = 0 Lux, Range 0 (1k Lux)		1	5	Counts
Full-Scale ADC Code	DATA_F				65535	Counts
Part-to-Part Variation (3σ population)	%/Value	E = 300 Lux, cold white LED Range 0 (1k Lux)		±5		%
Light Count Output with LSB of 0.015 Lux/Count	ADC <sub>R0</sub>	E = 300 Lux, fluorescent light (Note 5), ALS Range 0 (1k Lux)	15000	20473	25000	Counts
Light Count Output with LSB of 0.06 Lux/Count	ADC <sub>R1</sub>	E = 300 Lux, fluorescent light (Note 5), ALS Range 1 (4k Lux)		5100		Counts
Light Count Output with LSB of 0.24 Lux/Count	ADC <sub>R2</sub>	E = 300 Lux, fluorescent light (Note 5), ALS Range 2 (16k Lux)		1400		Counts
Light Count Output with LSB of 0.96 Lux/Count	ADC <sub>R3</sub>	E = 300 Lux, fluorescent light (Note 5), ALS Range 3 (64k Lux)		366		Counts
Infrared Count Output (Note 6)	ADC_IR <sub>R0</sub>	Range 0 (1k Lux)	1402	1997	2598	Counts
Infrared Count Output (Note 6)	ADC_IR <sub>R1</sub>	Range 1 (4k Lux)		481		Counts
Infrared Count Output (Note 6)	ADC_IR <sub>R2</sub>	Range 2 (16k Lux)		148		Counts
Infrared Count Output (Note 6)	ADC_IR <sub>R3</sub>	Range 3 (64k Lux)		42		Counts
SDA Current Sinking Capability	I <sub>SDA</sub>		4	5		mA

### NOTES:

- 550nm green LED is used in production test. The 550nm LED irradiance is calibrated to produce the same DATA count against an illuminance level of 300 Lux fluorescent light.
- 850 nm IR LED is used in production test.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**I<sup>2</sup>C Interface Specifications** $V_{DD} = 3.0V$ ,  $T_A = +25^\circ C$ , 16-bit ADC operation, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
SDA and SCL Input Buffer LOW Voltage	$V_{IL}$				0.55	V
SDA and SCL Input Buffer HIGH Voltage	$V_{IH}$		1.25			V
SDA and SCL Input Buffer Hysteresis	$V_{Hys}$ (Note 8)			$0.05 \times V_{DD}$		V
SDA Output Buffer LOW Voltage (open-drain), Sinking 4mA	$V_{OL}$ (Note 8)		0	0.06	0.40	V
SDA and SCL Pin Capacitance	$C_{PIN}$ (Note 8)	$T_A = +25^\circ C$ , $f = 1MHz$ , $V_{DD} = 5V$ , $V_{IN} = 0V$ , $V_{OUT} = 0V$			10	pF
SCL Frequency	$f_{SCL}$				400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	$t_{IN}$	Any pulse narrower than the maximum specification is suppressed			50	ns
SCL Falling Edge to SDA Output Data Valid	$t_{AA}$				900	ns
Time the Bus Must be Free Before the Start of a New Transmission	$t_{BUF}$		1300			ns
Clock LOW Time	$t_{LOW}$		1300			ns
Clock HIGH Time	$t_{HIGH}$		600			ns
START Condition Set-Up Time	$t_{SU:STA}$		600			ns
START Condition Hold Time	$t_{HD:STA}$		600			ns
Input Data Set-Up Time	$t_{SU:DAT}$		100			ns
Input Data Hold Time	$t_{HD:DAT}$		30			ns
STOP Condition Set-Up Time	$t_{SU:STO}$		600			ns
STOP Condition Hold Time	$t_{HD:STO}$		600			ns
Output Data Hold Time	$t_{DH}$		0			ns
SDA and SCL Rise Time	$t_R$ (Note 8)		$20 + 0.1 \times C_b$			ns
SDA and SCL Fall Time	$t_F$ (Note 8)		$20 + 0.1 \times C_b$			ns
Capacitive Loading of SDA or SCL	$C_b$ (Note 10)	Total on-chip and off-chip			400	pF
SDA and SCL Bus Pull-Up Resistor Off-chip	$R_{PU}$ (Note 8)	Maximum is determined by $t_R$ and $t_F$ For $C_b = 400pF$ , maximum is about $2k\Omega \sim 2.5k\Omega$ For $C_b = 40pF$ , maximum is about $15k\Omega \sim 20k\Omega$	1			k $\Omega$

## NOTES:

8. Limits should be considered typical and are not production tested.
9. These are I<sup>2</sup>C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
10.  $C_b$  is the capacitance of the bus in pF.