

Document Title

512K x16 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial draft	July 24, 2001	Preliminary
1.0	Finalize - lcc2 change : 30mA to 28mA for 55ns product 25mA to 22mA for 70ns product	September 27, 2001	Final

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512K x 16 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 512K x16
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three State Outputs
- Package Type: 48-TBGA-6.00x7.00

GENERAL DESCRIPTION

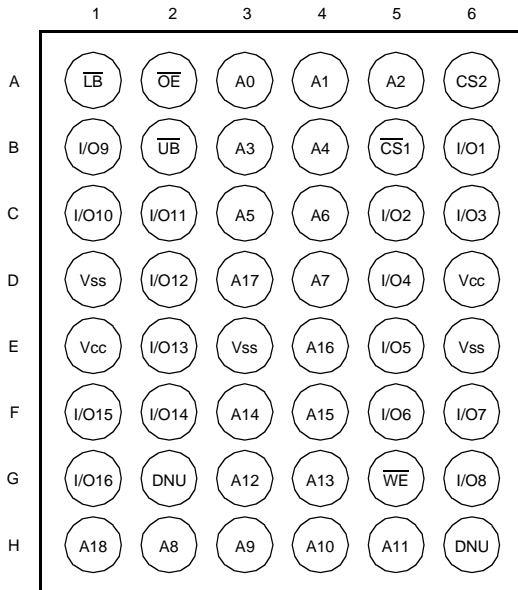
The K6F8016U6B families are fabricated by SAMSUNG's advanced full CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{SB1} , Typ.)	Operating (I _{CC1} , Max)	
K6F8016U6B-F	Industrial(-40~85°C)	2.7~3.3V	55 ¹⁾ /70ns	0.5μA ²⁾	2mA	48-TBGA-6.00x7.00

1. The parameter is measured with 30pF test load.
2. Typical values are measured at Vcc=3.0V, TA=25°C and not 100% tested

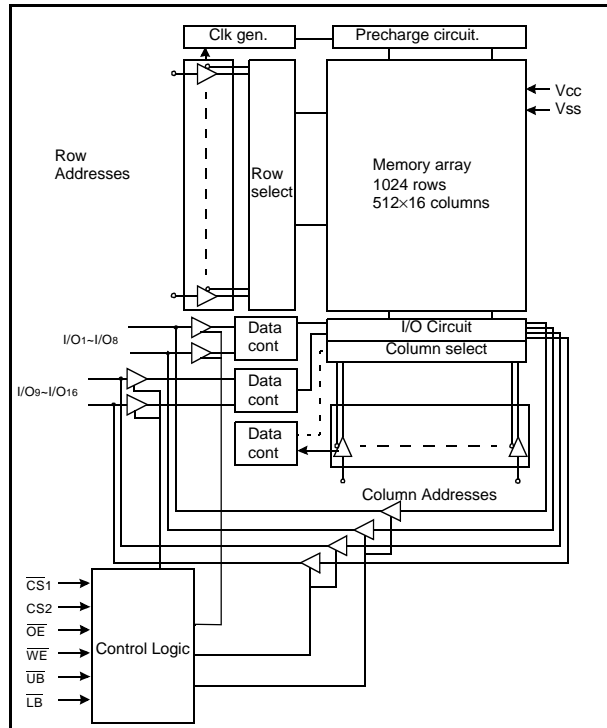
PIN DESCRIPTION



48 ball TBGA - Top View(Ball Down)

Name	Function	Name	Function
CS ₁ , CS ₂	Chip Select Inputs	Vcc	Power
OE	Output Enable Input	Vss	Ground
WE	Write Enable Input	UB	Upper Byte(I/O ₉₋₁₆)
A ₀ -A ₁₈	Address Inputs	LB	Lower Byte(I/O ₁₋₈)
I/O ₁ -I/O ₁₆	Data Inputs/Outputs	DNU	Do Not Use

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	Function
K6F8016U6B-EF55	48-TBGA, 55ns, 3.0V
K6F8016U6B-EF70	48-TBGA, 70ns, 3.0V

FUNCTIONAL DESCRIPTION

\overline{CS}_1	CS_2	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be low or high state)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.3V(Max. 3.6V)	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.3 to 3.6	V
Power Dissipation	P _d	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions over 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0	3.3	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	-0.3 ³⁾	-	0.6	V

Note:

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CC}+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTIC

Item	Symbol	Test Conditions	Min	Typ ¹⁾	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ or $\overline{LB}=\overline{UB}=V_{IH}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, $\overline{LB} \leq 0.2V$ or/and $\overline{UB} \leq 0.2V$, $CS_2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	2	mA
	I _{CC2}	Cycle time=Min, I _{IO} =0mA, 100% duty, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, $\overline{LB}=V_{IL}$ or/and $\overline{UB}=V_{IL}$, V _{IN} =V _{IL} or V _{IH}	70ns 55ns	- -	22 28	mA
Output low voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	-	-	V
Standby Current(CMOS)	I _{SB1}	Other input =0~V _{CC} 1) $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ (\overline{CS}_1 controlled) or 2) $0V \leq CS_2 \leq 0.2V$ (CS ₂ controlled)	-	0.5	15	μA

1. Typical values are measured at V_{CC}=3.0V, T_A=25°C and not 100% tested.

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

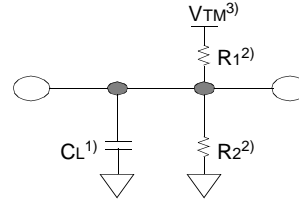
Input pulse level: 0.4 to 2.2V

Input rising and falling time: 5ns

Input and output reference voltage: 1.5V

Output load(see right): $C_L=100\text{pF}+1\text{TTL}$

$C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

2. $R_1=3070\Omega$, $R_2=3150\Omega$

3. $V_{TM}=2.8\text{V}$

AC CHARACTERISTICS ($V_{CC}=2.7\sim 3.3\text{V}$, Industrial product: $T_A=-40$ to 85°C)

Parameter List	Symbol	Speed Bins				Units	
		55ns		70ns			
		Min	Max	Min	Max		
Read	Read Cycle Time	tRC	55	-	70	-	ns
	Address Access Time	tAA	-	55	-	70	ns
	Chip Select to Output	tCO	-	55	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	35	ns
	\overline{UB} , \overline{LB} Access Time	tBA	-	55	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	\overline{UB} , \overline{LB} Enable to Low-Z Output	tBLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	20	0	25	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	tBHZ	0	20	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
	Output Hold from Address Change	tOH	10	-	10	-	ns
Write	Write Cycle Time	tWC	55	-	70	-	ns
	Chip Select to End of Write	tCW	45	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	45	-	60	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	tBW	45	-	60	-	ns
	Write Pulse Width	tWP	40	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	20	0	20	ns
	Data to Write Time Overlap	tDW	25	-	30	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
	End Write to Output Low-Z	tOW	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ ²⁾	Max	Unit
Vcc for data retention	VDR	$\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$	1.5	-	3.3	V
Data retention current	IDR	$V_{CC}=1.5\text{V}$, $\overline{CS}_1 \geq V_{CC}-0.2\text{V}^{1)}$	-	0.5	6	μA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	trDR		tRC	-	-	

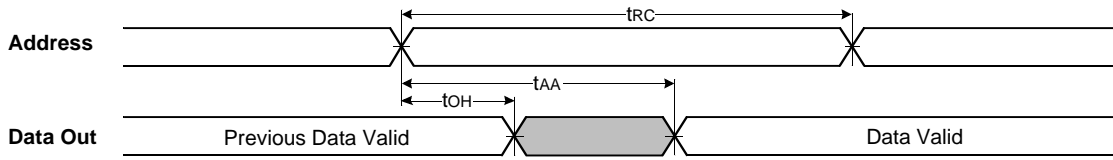
1. 1) $\overline{CS}_1 \geq V_{CC}-0.2\text{V}$, $\overline{CS}_2 \geq V_{CC}-0.2\text{V}$ (\overline{CS}_1 controlled) or

2) $0 \leq \overline{CS}_2 \leq 0.2\text{V}$ (\overline{CS}_2 controlled)

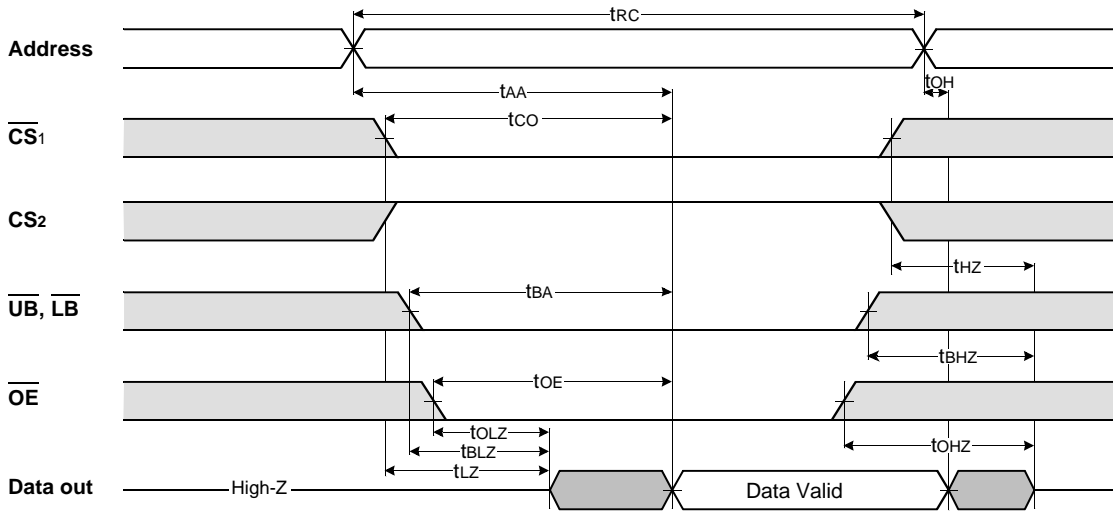
2. Typical value are measured at $T_A=25^\circ\text{C}$ and not 100% tested.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)



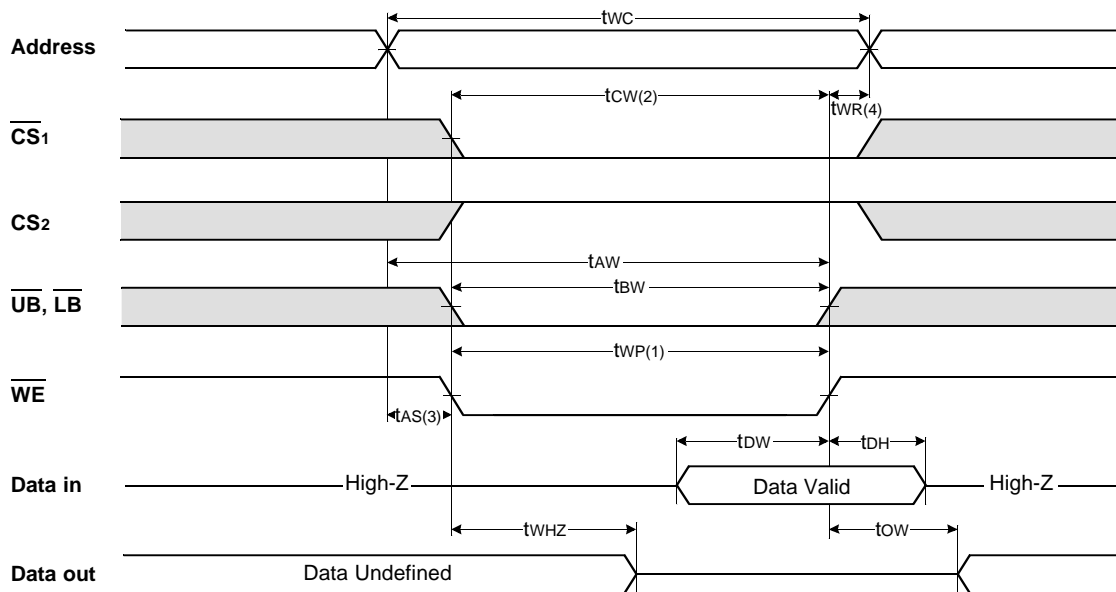
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



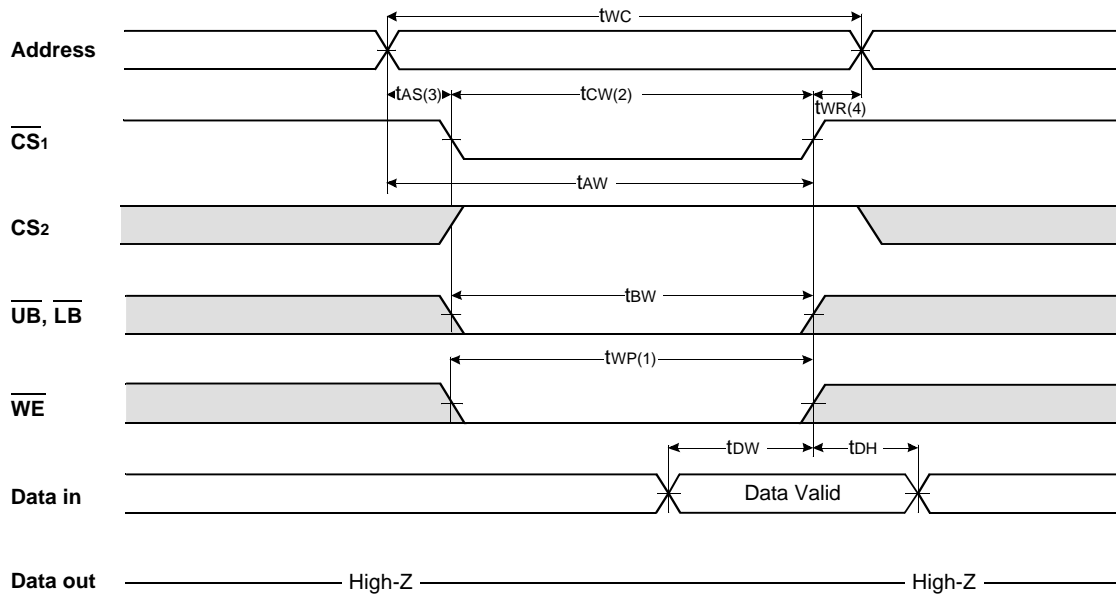
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

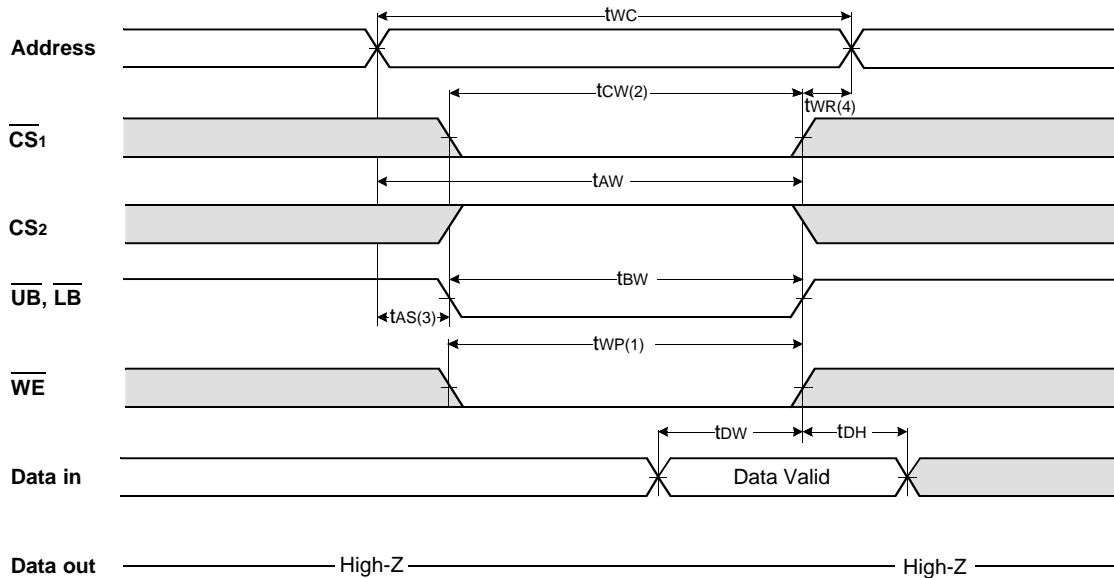
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{UB} , \overline{LB} Controlled)

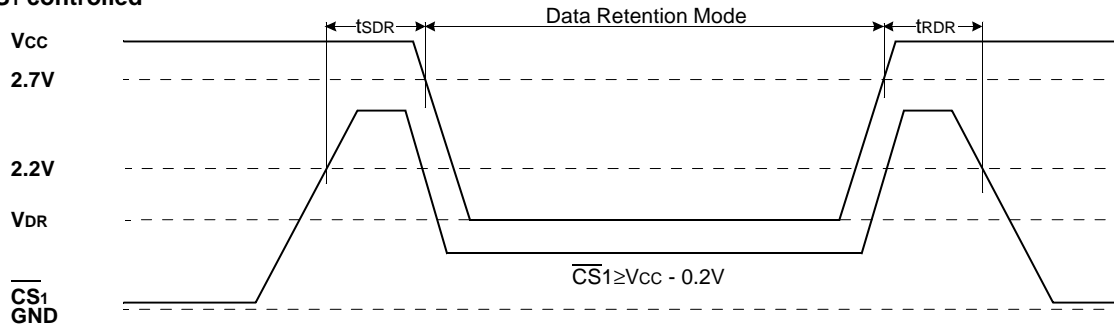


NOTES (WRITE CYCLE)

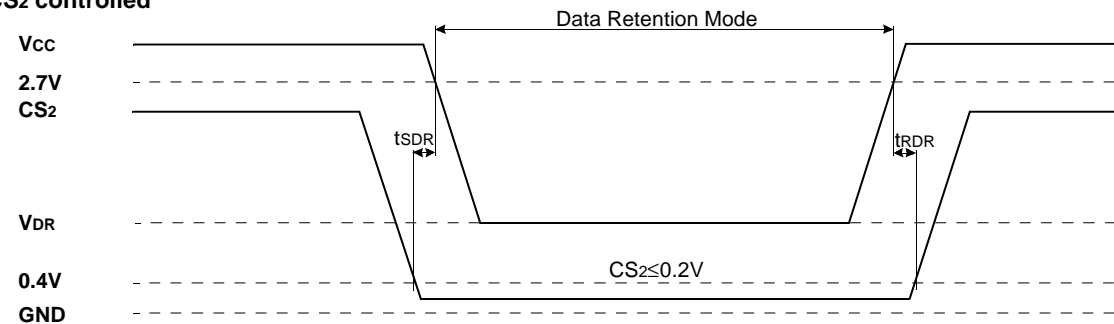
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS1}$ or \overline{WE} going high.

DATA RETENTION WAVE FORM

$\overline{CS1}$ controlled



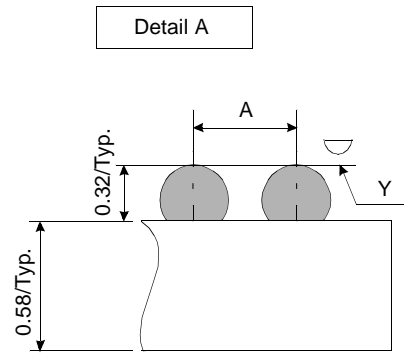
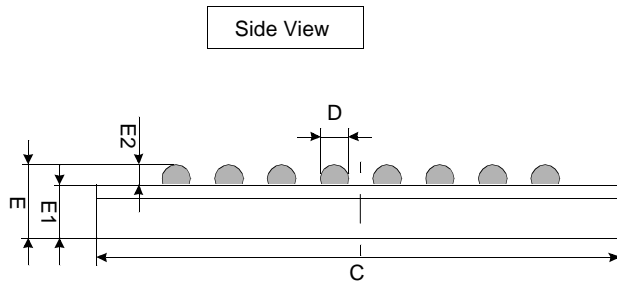
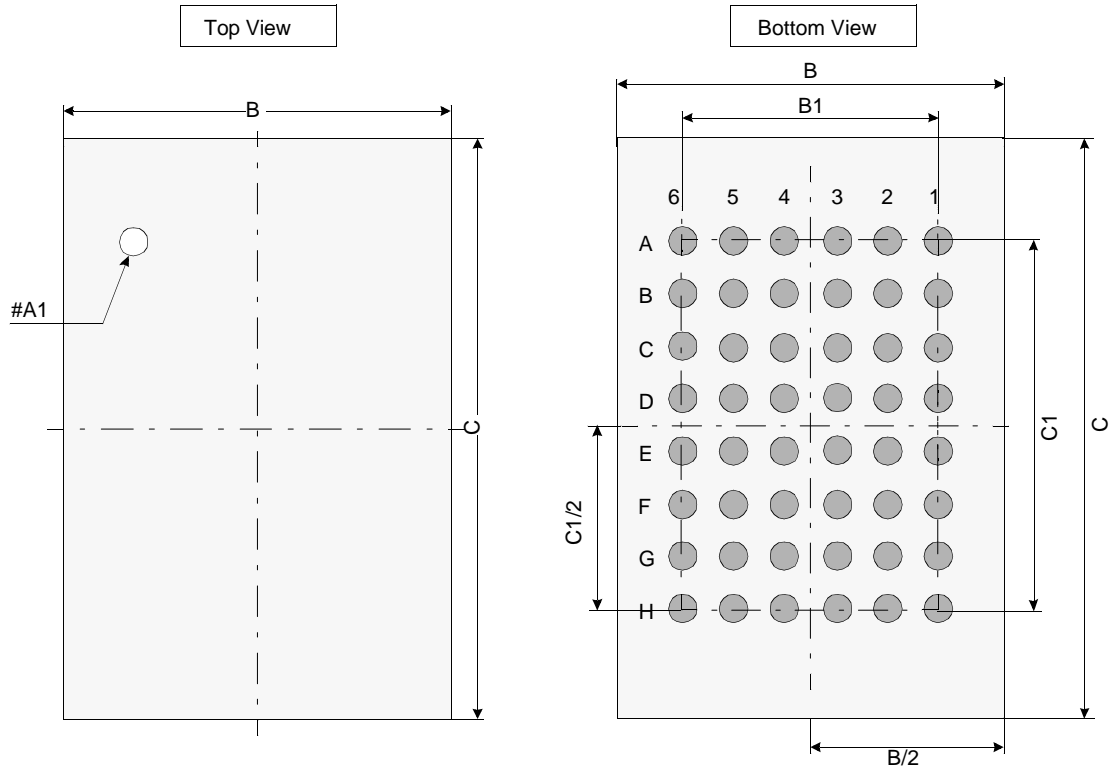
$CS2$ controlled



PACKAGE DIMENSION

Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	0.80	0.90	1.00
E1	-	0.58	-
E2	0.27	0.32	0.37
Y	-	-	0.08

Notes.

1. Ball counts: 48(8 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity: 0.08(Max)

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