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# HA17080 Series

## J-FET Input Operational Amplifiers

# HITACHI

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### Description

Since J-FET input operational amplifiers are formed from a pair of J-FET transistors, they provide superlative characteristics, including a high input impedance and a low input bias current. Thus they can be used in a wide range of applications, from general-purpose control equipment to medical applications. In particular, they are optimal for processing signals from high-impedance sensors.

Hitachi J-FET input operational amplifiers are available in single, dual, and quad versions. Other than the HA17080, all products are internal phase compensation types and include a built-in phase compensation capacitor. The HA17080 and the HA17083 allow offset adjustment. These products are also available in “A” grade versions with superlative electrical characteristics to allow the selection of an operational amplifier appropriate for the application.

### Features

- Wide operating power supply voltage range:  $\pm 5$  V to  $\pm 18$  V
- Low input bias current: 30 pA
- Low input offset current: 5 pA
- High input impedance:  $10^{12} \Omega$
- High slew rate: 13 V/ $\mu$ s
- Wide common mode input voltage range with operation possible near the power-supply voltage ( $V_{CC}$ ).
- High voltage gain: 106 dB
- The HA17080 and HA17083 support offset adjustment.
- Pin compatible with the Texas Instruments TL080 series.

Notes: 1. Since these products are high input impedance operational amplifiers, contamination may cause the input bias and input offset currents to increase if they are handled with bare hands.

Avoid contamination when handling these devices.

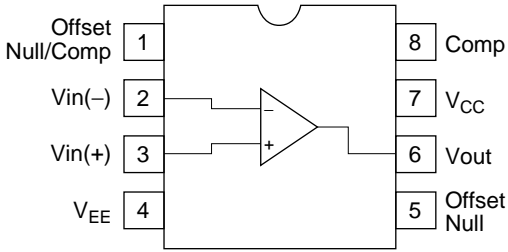
2. Since these products provide a high slew rate, oscillation may occur due to load capacitances.  
( $C_L < 100$  pF: voltage follower mode)

## Ordering Information

Item	Type No.			
	HA17080	HA17082	HA17083	HA17084
Number of operational amplifiers (number of channels)	Single	Dual	Dual	Quad
Offset adjustment pin	Yes	No	Yes	No
Phase compensation type	External	Internal	Internal	Internal

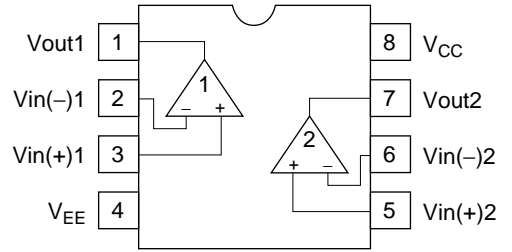
## Pin Arrangement

**HA17080**



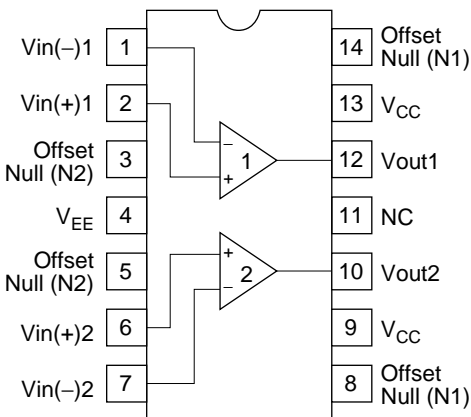
(Top view)

**HA17082**



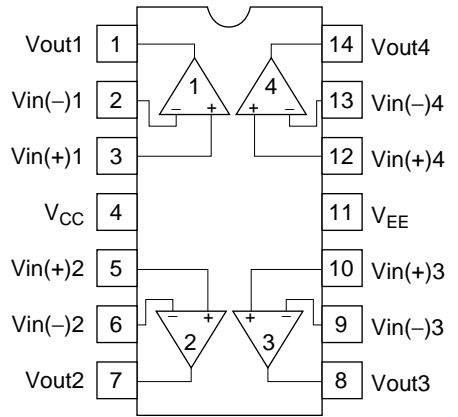
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**HA17083**



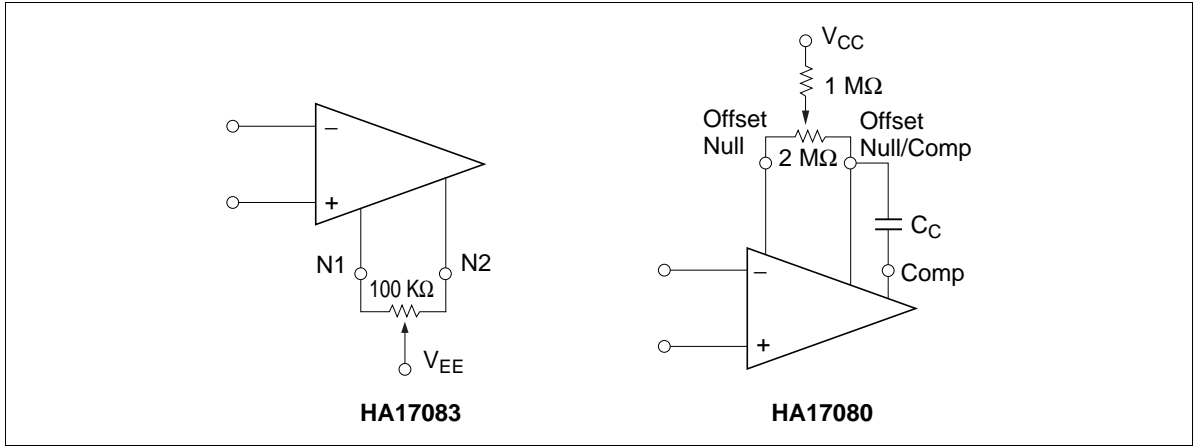
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**HA17084**

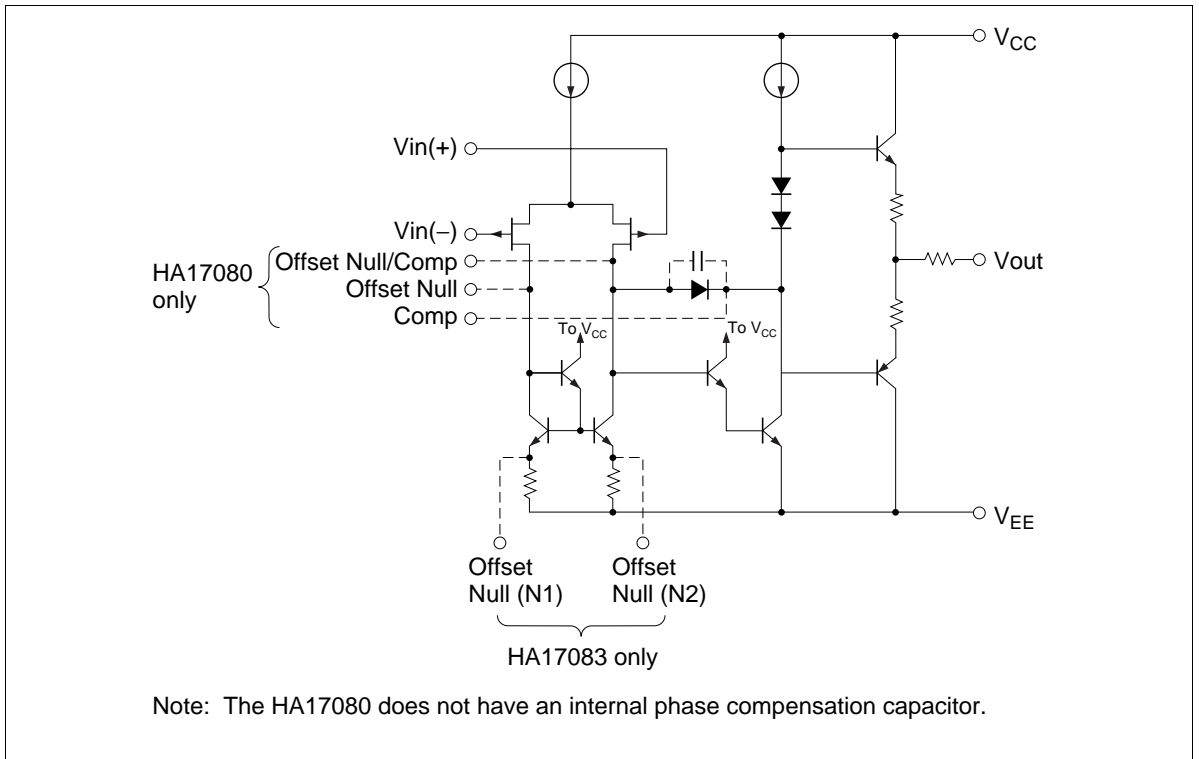


(Top view)

Voltage Offset Test Circuit



Circuit Structure



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings (P, PS Series)	Unit	Notes
Power-supply voltage	V <sub>CC</sub>	+18	V	
	V <sub>EE</sub>	-18	V	
Differential input voltage	V <sub>in(diff)</sub>	±30	V	
Input voltage	V <sub>in</sub>	±15	V	1
Allowable power dissipation	P <sub>T</sub>	625	mW	2
Operating temperature	T <sub>opr</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	

- Notes: 1. When the power-supply voltage is less than ±15 V, the input voltage must fall within the power-supply voltage range.
2. These are the allowable values up to Ta = 50°C for the P and PS series. Derate by 8.3 mW/°C above that temperature.

## Electrical Characteristics ( $V_{CC} = -V_{EE} = 15\text{ V}$ , $T_a = 25^\circ\text{C}$ )

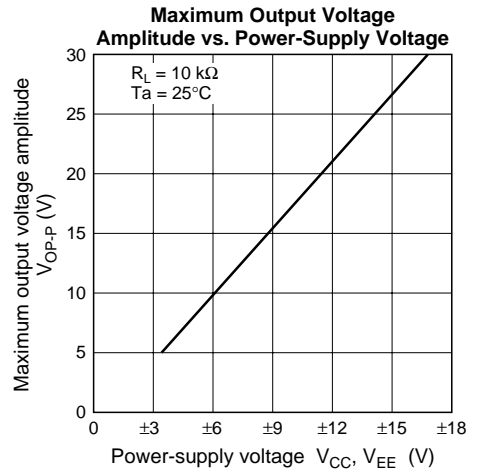
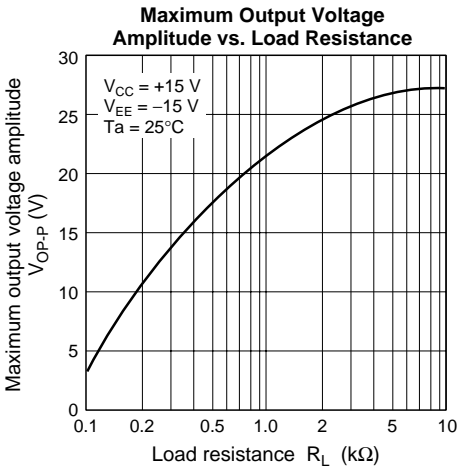
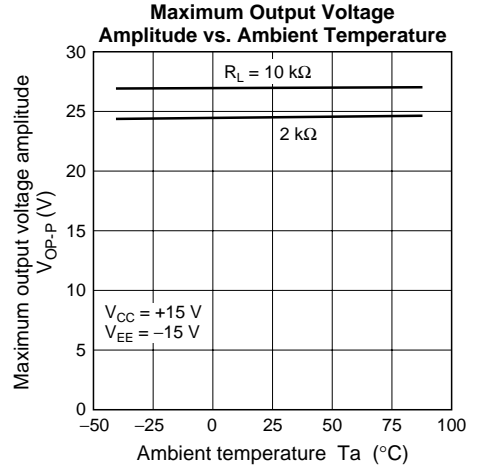
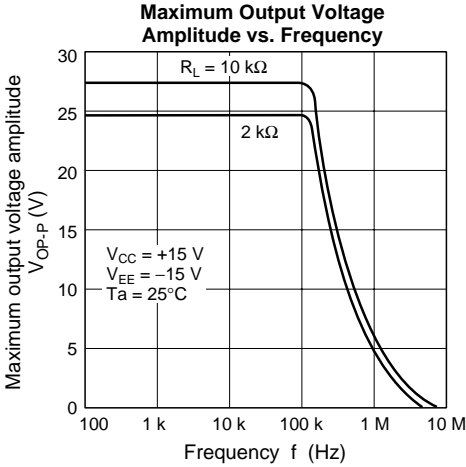
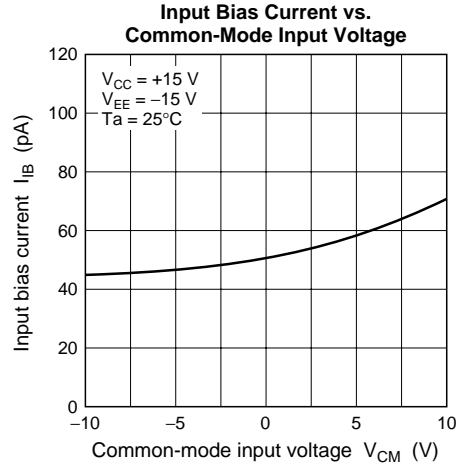
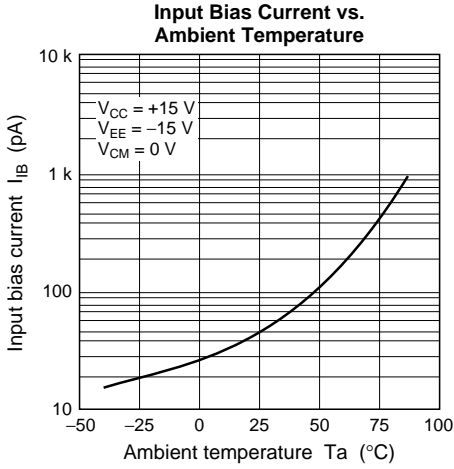
Item	Symbol	HA17080 Series			HA17080A Series			Unit	Test Conditions	Notes
		Min	Typ	Max	Min	Typ	Max			
Input offset voltage	$V_{IO}$	—	5	15	—	3	6	mV	$R_S = 50\ \Omega$	1
Input offset current	$I_{IO}$	—	5	200	—	5	100	pA	$I_{IO} =  I_{IB(+)} - I_{IB(-)} $	1
Input bias current	$I_{IB}$	—	30	400	—	30	200	pA		1, 2
Common-mode input voltage range	$V_{CM}$	$\pm 10$	—	—	$\pm 11$	—	—	V		1
Maximum output voltage amplitude	$V_{op-p}$	24	27	—	24	27	—	V	$R_L \geq 10\ \text{k}\Omega$	
		20	24	—	20	24	—		$R_L \geq 2\ \text{k}\Omega$	
Voltage Gain	$A_{VD}$	88	106	—	94	106	—	dB	$R_L \geq 2\ \text{k}\Omega$ , $V_O = \pm 10\ \text{V}$	1
Common-mode rejection ratio	CMR	70	86	—	80	86	—	dB	$R_S \leq 10\ \text{k}\Omega$	1
Power supply rejection ratio	PSRR	70	86	—	80	86	—	dB	$R_S \leq 10\ \text{k}\Omega$	1
Supply current	$I_{CC}$	—	1.4	2.8	—	1.4	2.8	mA		3
Bandwidth	BW	—	3	—	—	3	—	MHz	$A_{VD} = 1$	
Slew rate	SR	—	13	—	—	13	—	V/ $\mu\text{s}$	$V_{in} = 10\ \text{V}$ , $R_L = 2\ \text{k}\Omega$ , $C_L = 100\ \text{pF}$ , $A_{VD} = 1$	
Channel separation	CS	—	120	—	—	120	—	dB	$A_{VD} = 100$	
Rise time	$t_r$	—	0.1	—	—	0.1	—	$\mu\text{s}$	$V_{in} = 20\ \text{mV}$ , $R_L = 2\ \text{k}\Omega$	
Overshoot	$V_{over}$	—	10	—	—	10	—	%	$C_L = 100\ \text{pF}$ , $A_{VD} = 1$	
Input resistance	$R_{in}$	—	$10^{12}$	—	—	$10^{12}$	—	$\Omega$		
Input noise voltage	$V_n$	—	35	—	—	35	—	nV/ $\sqrt{\text{Hz}}$	$R_S = 100\ \Omega$ , $f = 1\ \text{kHz}$	

Notes: 1. The non-A ratings apply to the HA17080, HA17082, HA17083, and HA17084.

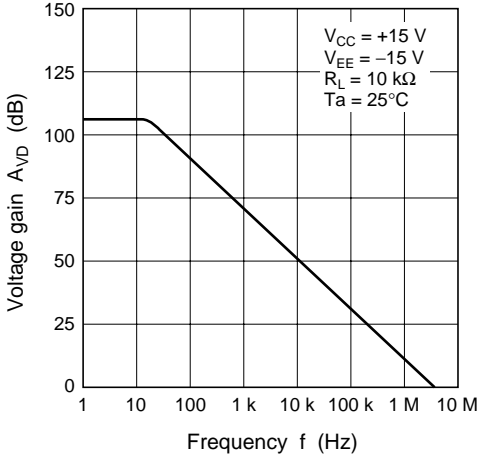
The A version ratings apply to the HA17080A, HA17082A, HA17083A, and HA17084A.

2. This is the J-FET gate leakage current, which is temperature dependent. The junction temperature must be held near room temperature when measuring this parameter.
3. This is the per-channel value.

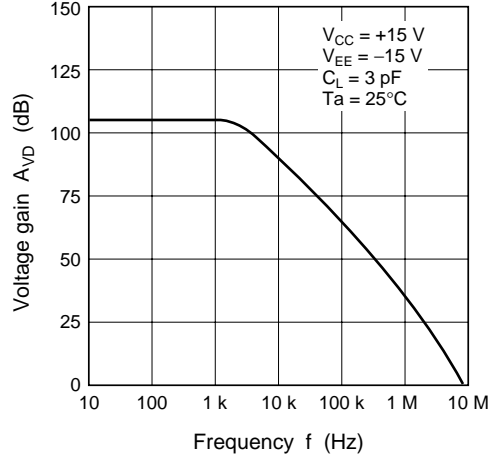
## Characteristic Curves



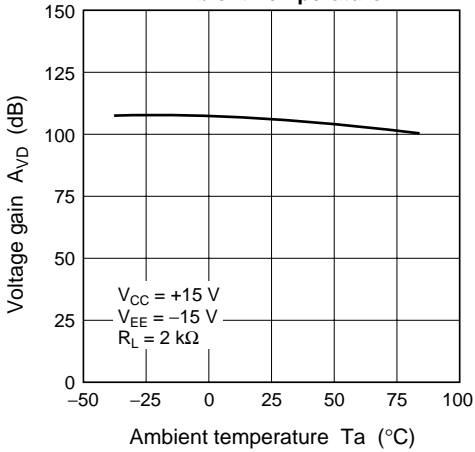
Voltage Gain vs. Frequency (1)



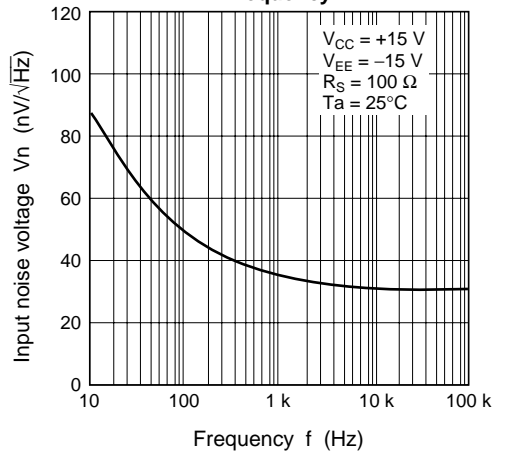
Voltage Gain vs. Frequency (2)



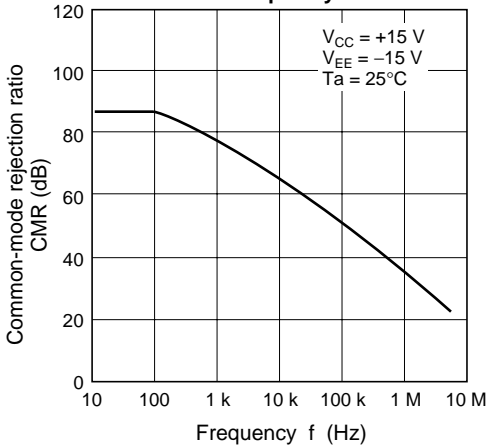
Voltage Gain vs. Ambient Temperature



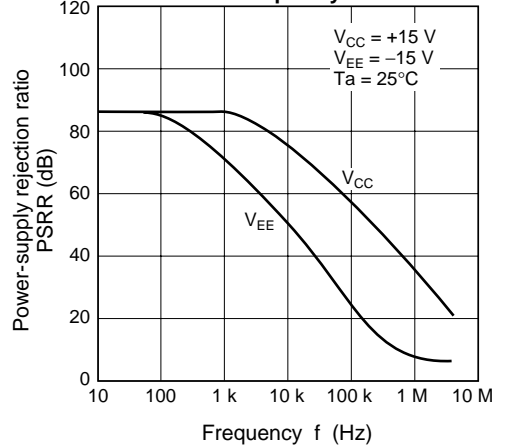
Input Noise Voltage vs. Frequency

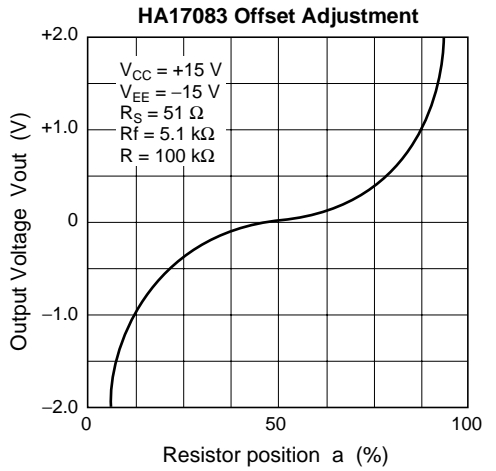
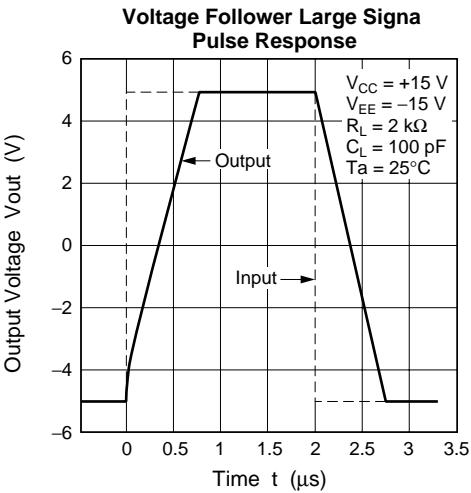
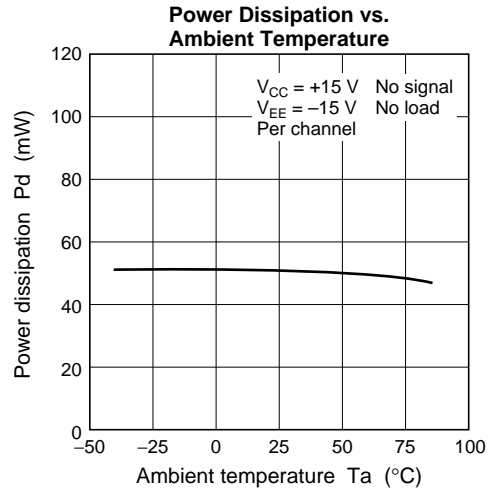
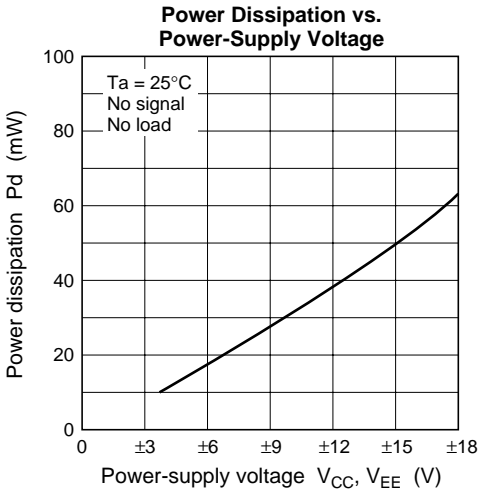
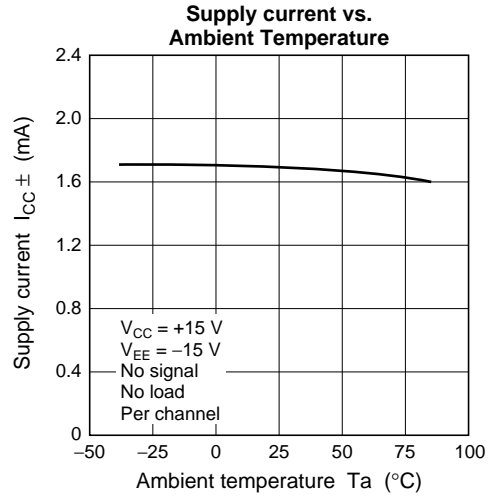
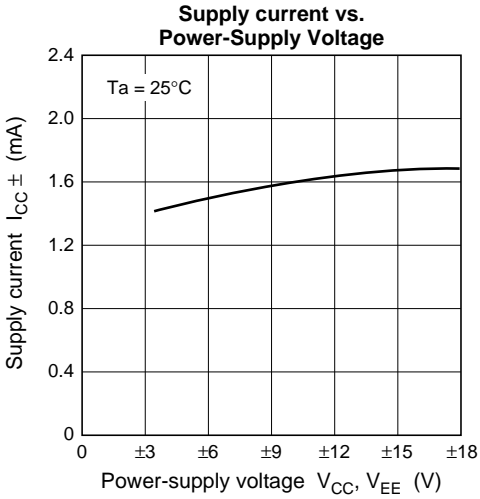


Common-Mode Rejection Ratio vs. Frequency



Power-Supply Rejection Ratio vs. Frequency

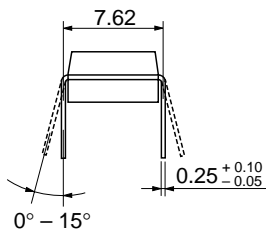
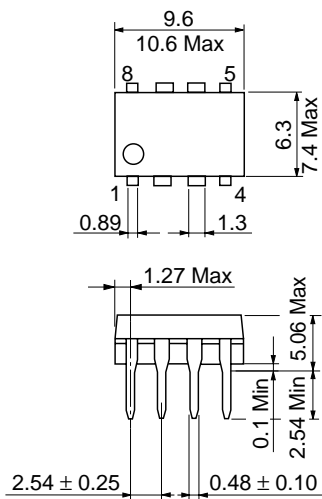






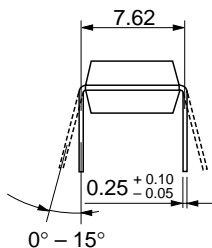
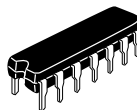
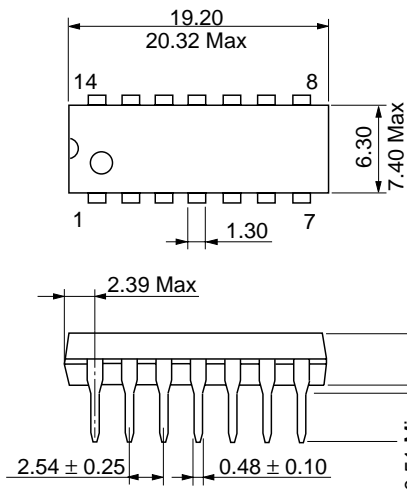
Package Dimensions

Unit: mm



Hitachi Code	DP-8
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.54 g

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

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