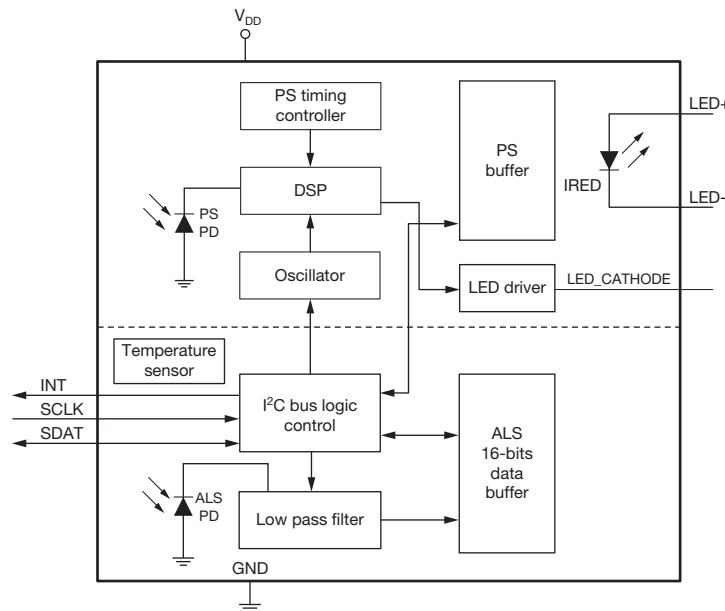


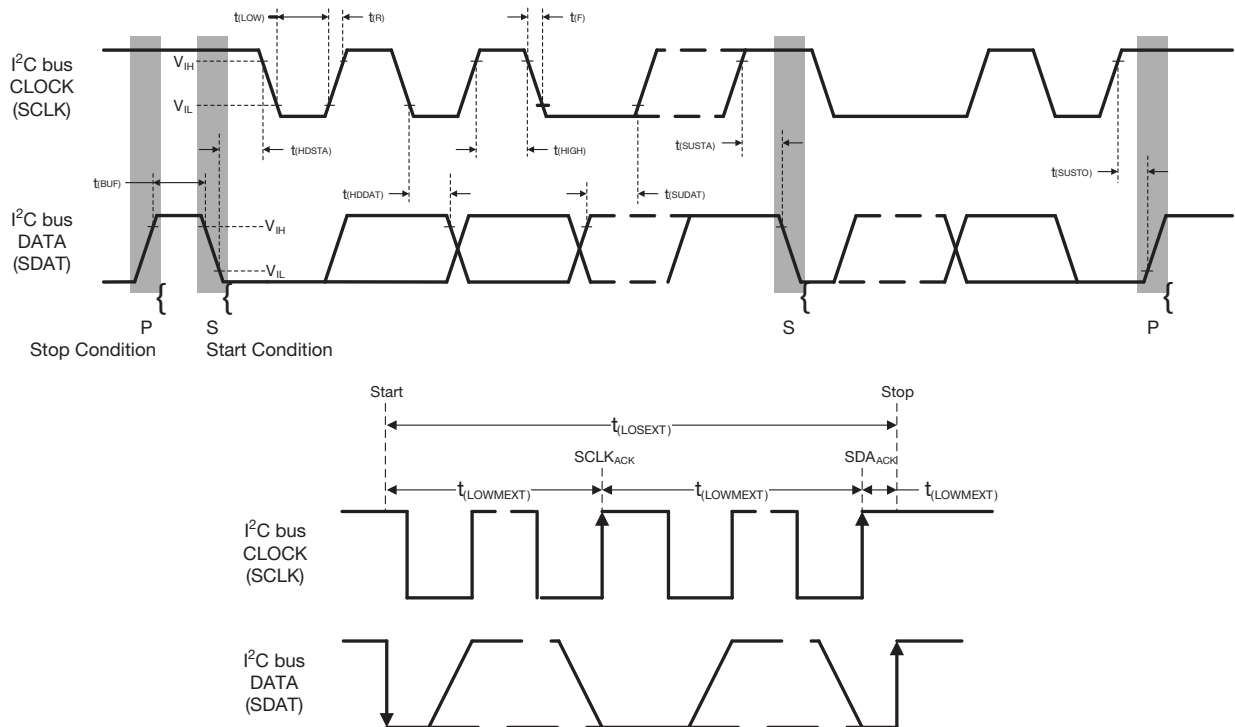
BLOCK DIAGRAM


BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)							
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Supply voltage		V_{DD}	2.5	-	3.6	V	
Supply voltage for IRED		V_{IRED}	3.8	-	5.0	V	
Supply current	Excluded LED driving	I_{DD}	-	195	-	μA	
Shutdown current	Light condition = dark, $V_{DD} = 3.3\text{ V}$	$I_{DD}(\text{SD})$	-	0.2	-	μA	
ALS shut down	ALS disable, PS enable	I_{ALSSD}	-	180	-	μA	
PS shut down	ALS enable, PS disable	I_{PSSD}	-	175	-	μA	
I²C signal input	Logic high	$V_{DD} = 3.3\text{ V}$	V_{IH}	1.5	-	-	V
	Logic low		V_{IL}	-	-	0.8	
	Logic high	$V_{DD} = 2.6\text{ V}$	V_{IH}	1.4	-	-	V
	Logic low		V_{IL}	-	-	0.6	
Peak sensitivity wavelength of ALS		λ_p	-	550	-	nm	
Peak sensitivity wavelength of PS		λ_{pps}	-	940	-	nm	
Full ALS counts	16-bit resolution		-	-	65 535	steps	
Full PS counts	8-bit resolution		-	-	255	steps	
Detectable intensity	Minimum	$IT = 640\text{ ms}$, $V_{DD} = 3.3\text{ V}$, 1 step ⁽¹⁾⁽²⁾		0.01	-	lx	
	Maximum	$IT = 80\text{ ms}$, $V_{DD} = 3.3\text{ V}$, 65 535 steps ⁽¹⁾⁽²⁾		5243	-		
ALS dark offset	$IT = 80\text{ ms}$, $V_{DD} = 3.3\text{ V}$, normal sensitivity ⁽¹⁾		0	-	3	steps	
Operating temperature range		T_{amb}	-40	-	+85	$^{\circ}\text{C}$	
IRED driving current	⁽³⁾		-	-	800	mA	

Notes

- (1) Light source: white LED
- (2) Maximum detection range to ambient light can be determined by ALS refresh time adjustment. Refer to table 17 "ALS Resolution and Maximum Detection Range"
- (3) Based on IRED on / off duty ratio = 1/5120, 1/640, 1/80, and 1/20. The circuitry should use an external MOSFET as shown with fig.10. Please see also the Application Note "Designing the VCNL4100 into an Application" (www.vishay.com/doc?84361).

I²C BUS TIMING CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)						
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	μs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	μs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	μs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	μs
Data hold time	$t_{(HDDAT)}$		3450	-	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I ² C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	μs
I ² C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	μs
Detect clock / data low timeout	$t_{(TIMEOUT)}$	25	35	-	-	ms
Clock / data fall time	$t_{(F)}$	-	300	-	300	ns
Clock / data rise time	$t_{(R)}$	-	1000	-	300	ns


 Fig. 1 - I²C Bus Timing Diagram