Bulletin I27125 rev. A 04/99

International
IOR Rectifier

P100 SERIES

PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

25A

Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}, V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved

Description

The P100 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.
Applications include power supplies, control circuits and battery chargers.

Major Ratings and Characteristics

Parameters		P100	Units
I_D		25	A
	@ T_C	85	°C
I_{FSM}	@50Hz	357	A
	@ 60Hz	375	A
I^2t	@50Hz	637	A^2s
	@ 60Hz	580	A^2s
$I^2\sqrt{t}$		6365	$A^2\sqrt{s}$
V_{RRM}		400 to 1200	V
V_{INS}		2500	V
T_J		- 40 to 125	°C

This datasheet has been downloaded from http://www.digchip.com at this page

ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	V_{RRM} maximum repetitive peak reverse voltage V	V_{RSM} maximum non-repetitive peak reverse voltage V	V_{DRM} maximum repetitive peak off-state voltage V	I_{RRM} max. @ T_J max. mA
P101, P121, P131	400	500	400	10
P102, P122, P132	600	700	600	
P103, P123, P133	800	900	800	
P104, P124, P134	1000	1100	1000	
P105, P125, P135	1200	1300	1200	

On-state Conduction

	Parameter	P100	Units	Conditions		
I_D	Maximum DC output current	25	A	@ T_C = 85°C, full bridge		
I_{TSM}	Max. peak one-cycle	357	A	t = 10ms	No voltage	Sinusoidal half wave, Initial $T_J = T_J$ max.
I_{FSM}	non-repetitive on-state	375		t = 8.3ms	reapplied	
	or forward current	300		t = 10ms	100% V_{RRM}	
		315		t = 8.3ms	reapplied	
I^2t	Maximum I^2t for fusing	637	A^2s	t = 10ms	No voltage	
		580		t = 8.3ms	reapplied	
		450		t = 10ms	100% V_{RRM}	
		410		t = 8.3ms	reapplied	
$I^2\sqrt{t}$	Maximum $I^2\sqrt{t}$ for fusing	6365	$A^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reapplied I^2t for time tx = $I^2\sqrt{t} \cdot \sqrt{tx}$		
$V_{T(TO)}$	Max. value of threshold voltage	0.82	V	T_J = 125°C		
r_{t1}	Max. level value of on-state slope resistance	12	mΩ	T_J = 125°C, Av. power = $V_{T(TO)} * I_{T(AV)} + r_t + (I_{T(RMS)})^2$		
V_{TM}	Max. peak on-state or	1.35	V	T_J = 25°C, $I_{TM} = \pi \times I_{T(AV)}$		
V_{FM}	forward voltage drop					
di/dt	Maximum non repetitive rate of rise of turned on current	200	A/µs	T_J = 125°C from 0.67 V_{DRM} $I_{TM} = \pi \times I_{T(AV)}$, I_g = 500mA, tr < 0.5µs, tp > 6µs		
I_H	Maximum holding current	130	mA	T_J = 25°C anode supply = 6V, resistive load, gate open		
I_L	Maximum latching current	250	mA	T_J = 25°C anode supply = 6V, resistive load		

Blocking

	Parameter	P100	Units	Conditions
dv/dt	Maximum critical rate of rise of off-state voltage	200	V/µs	T_J = 125°C, exponential to 0.67 V_{DRM} gate open
I_{RRM} I_{DRM}	Max. peak reverse and off-state leakage current at V_{RRM}, V_{DRM}	10	mA	T_J = 125°C, gate open circuit
I_{RRM}	Max peak reverse leakage current	100	µA	T_J = 25°C
V_{INS}	RMS isolation voltage	2500	V	50Hz, circuit to base, all terminal shorted, T_J = 25°C, t = 1s

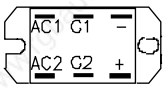
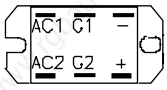
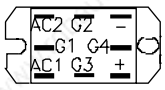
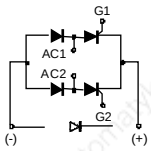
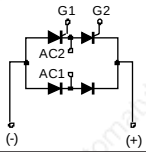
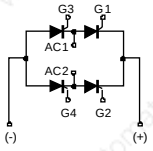
Triggering

	Parameter	P100	Units	Conditions	
P_{GM}	Maximum peak gate power	8	W		
$P_{G(AV)}$	Maximum average gate power	2			
I_{GM}	Maximum peak gate current	2	A		
$-V_{GM}$	Maximum peak negative gate voltage	10	V		
V_{GT}	Maximum gate voltage required to trigger	3 2 1		T_J = - 40°C T_J = 25°C T_J = 125°C	Anode Supply = 6V resistive load
I_{GD}	Maximum gate current required to trigger	90 60 35	mA	T_J = - 40°C T_J = 25°C T_J = 125°C	Anode Supply = 6V resistive load
V_{GD}	Maximum gate voltage that will not trigger	0.2	V	T_J = 125°C, rated V_{DRM} applied	
I_{GD}	Maximum gate current that will not trigger	2	mA	T_J = 125°C, rated V_{DRM} applied	

Thermal and Mechanical Specification

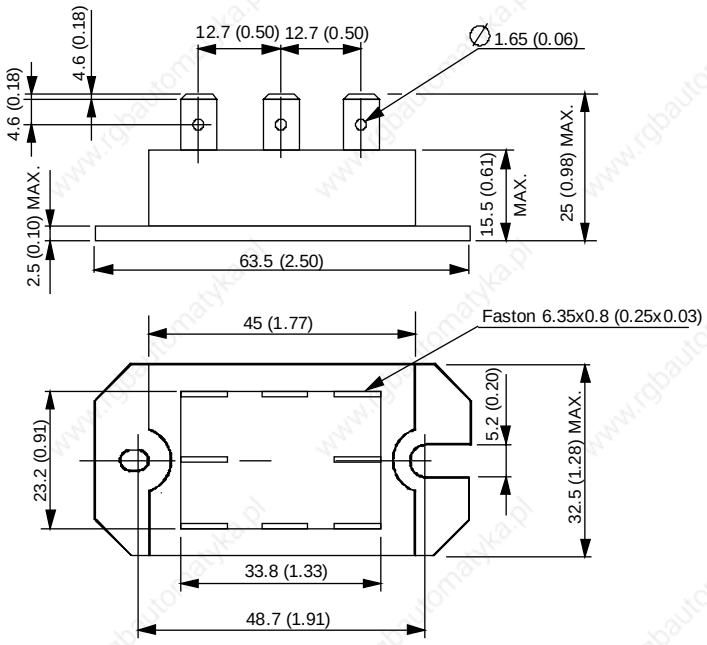
	Parameter	P100	Units	Conditions
T_J	Max. operating temperature range	-40 to 125	°C	
T_{stg}	Max. storage temperature range	-40 to 125		
R_{thJC}	Max. thermal resistance, junction to case	2.24	K/W	DC operation per junction
R_{thCS}	Max. thermal resistance, case to heatsink	0.10	K/W	Mounting surface, smooth and greased
T	Mounting torque, base to heatsink	4	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound
wt	Approximate weight	58 (2.0)	g (oz)	

Circuit Type and Coding *

	Circuit"0"	Circuit"2"	Circuit"3"
Terminal Positions			
Schematic diagram diagram			
	Single Phase Hybrid Bridge Common Cathode	Single Phase Hybrid Bridge Doubler	Single Phase All SCR Bridge
Basic series	P10.	P12.	P13.
With voltage suppression	P10.K	P12.K	P13.K
With free-wheeling diode	P10.W	-	-
With both voltage suppression and free-wheeling diode	P10.KW	-	-

* To complete code refer to voltage ratings table, i.e.: for 600V P10.W complete code is P102W

Outline Table



All dimensions in millimeters (inches)

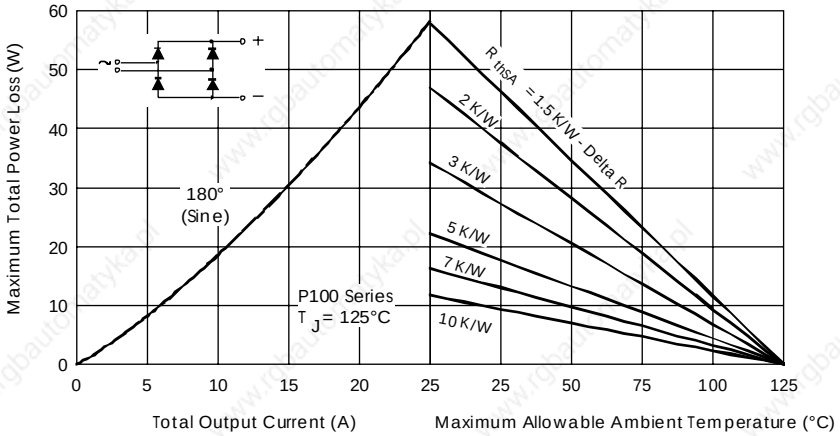


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

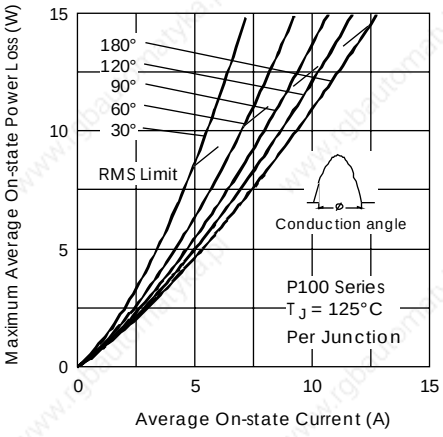


Fig. 2 - On-state Power Loss Characteristics

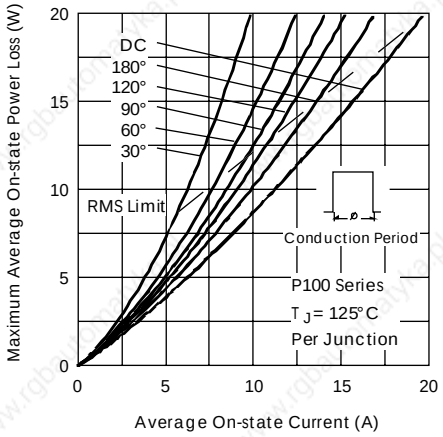


Fig. 3 - On-state Power Loss Characteristics

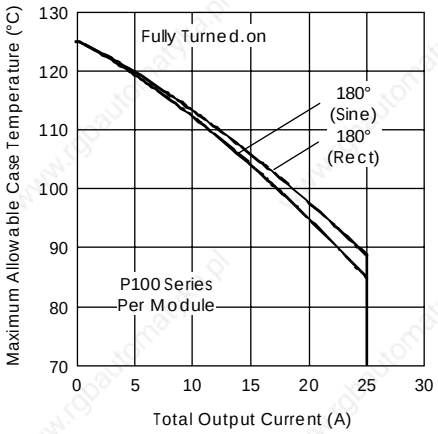


Fig. 4 - Current Ratings Characteristics

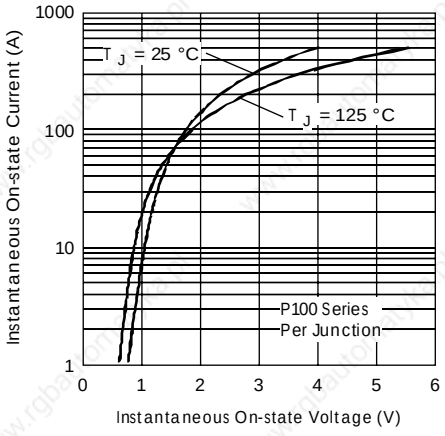


Fig. 5 - On-state Voltage Drop Characteristics

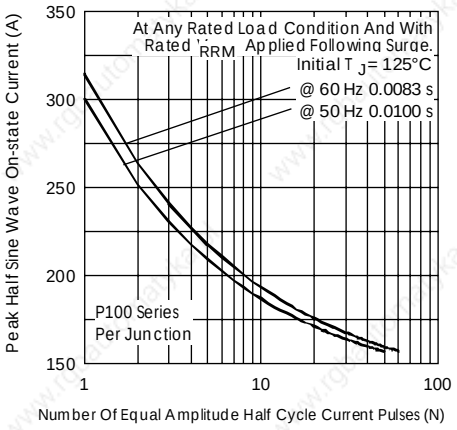


Fig. 6 - Maximum Non-Repetitive Surge Current

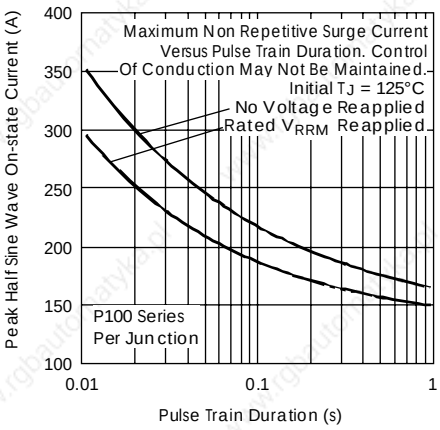


Fig. 7 - Maximum Non-Repetitive Surge Current

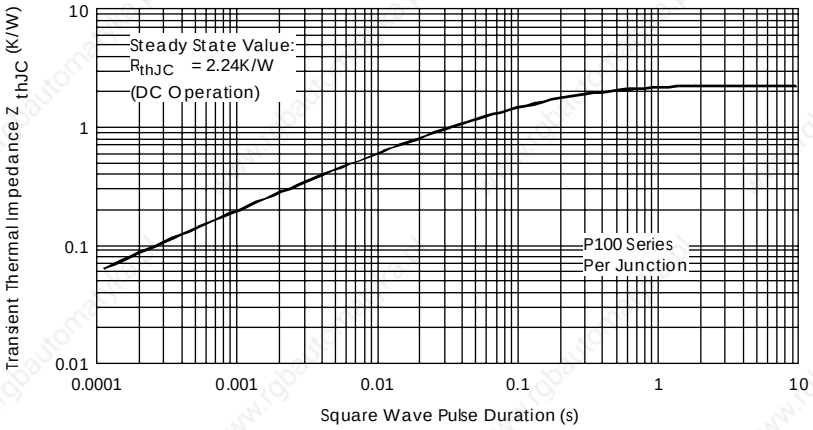


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

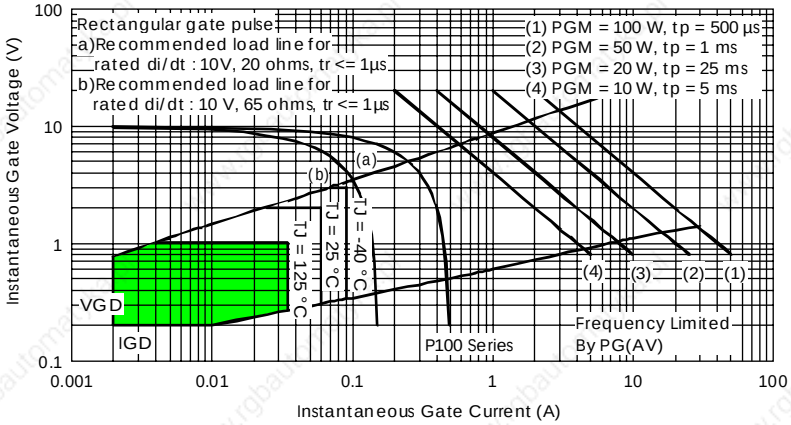


Fig. 9 - Gate Characteristics

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