

### 3. OUTPUT SPECIFICATIONS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
V1 Output Voltages	±0.5% set point accuracy RS+ closed on +V1, RS- closed on V1 RTN, at 6% load.	-	24 48	-	V
	85 – 137 V <sub>AC</sub> (120-163 V <sub>DC</sub> ), 800 LFM			600	W
V1 Output Power Rating	180 – 305 V <sub>AC</sub> (163-300 V <sub>DC</sub> ), 800 LFM			750	
	Peak, <10 s, after P_Ok asserted high			900	
V1 Output Current	85 – 137 V <sub>AC</sub> (120-163 V <sub>DC</sub> )	V1: 24 V <sub>DC</sub> V1: 48 V <sub>DC</sub>		25.7 12.5	A
	180 – 305 V <sub>AC</sub> (163-300 V <sub>DC</sub> )	V1: 24 V <sub>DC</sub> V1: 48 V <sub>DC</sub>		31.2 15.6	
V1 Voltage Adjustment Range	Manually by push up and down buttons	-	±5	-	%V1
V1 Line Regulation	V <sub>AC</sub> : 85 – 305 V <sub>RMS</sub>	-	-	±0.1	%V1
V1 Load-Line-Cross Regulation	V <sub>AC</sub> : 85 – 305 V <sub>RMS</sub> ; I <sub>1</sub> : 0 – 100%	-	-	±2	%V1
V1 Ripple and Noise	Rated load, Peak-to-peak, 20 MHz BW. (100 nF ceramic, 10 µF tantalum at load)	-	-	1	%V1
Transient Response: V1, 12V <sub>SB</sub> , 5V <sub>SB</sub>	25% load changes at 1 A/µs 24 V at 1000 µF load / I <sub>OUT</sub> > 2.5 A 48 V at 560 µF load / I <sub>OUT</sub> > 1.25 A	-	-	±5	%V1
Voltage Deviation	12 V <sub>SB</sub> , 5 V <sub>SB</sub> at 0-2200 µF load				%V <sub>SB</sub>
V1 Start-up Rise Time	85 < V <sub>IN</sub> < 305, any load conditions.	10	-	150	ms
	At nominal V <sub>IN</sub> , full load SEMI F47-0706 compliant at ≥208 V <sub>AC</sub>	10	-	-	
V1 Hold-up Time		50% sag (104 V)	200	-	ms
		30% sag (145 V)	500	-	
		20% sag (166 V)	1000	-	
V1 Current Sharing Accuracy	Parallel operation up to four units. Two units in parallel at I <sub>1</sub> rated load. I-Share signals connected together. RS+, RS- signals connected together and to the load. Max load at start up 750 W, operating 1250 W, 180÷305 V <sub>AC</sub> Max load at start up 600 W, operating 1000 W, 85÷137 V <sub>AC</sub>	40	-	60	%I <sub>1</sub>
V1 Remote Sense	RS+ and RS- power path voltage loss compensation	-	-	0.36	V
Start-up Delay	V1 in regulation after de-asserting PS_Inhibit	-	-	1700	
	V1 in regulation after AC is applied (worst case: 85 V <sub>AC</sub> )	-	-	2200	ms
	5V <sub>SB</sub> in regulation after AC is applied (worst case: 85 V <sub>AC</sub> )	-	-	500	
Turn-on Overshoot		-	-	10	%V1
		-	-	10	%V <sub>SB</sub>
Minimum Load	V1, 12V <sub>SB</sub> , 5V <sub>SB</sub>	0	-	-	A
Maximum Load Capacitance		V1: 24 V <sub>DC</sub>	-	16000	µF
		V1: 48 V <sub>DC</sub>	-	8000	
V1 Over Current Protection		V1: 24 V <sub>DC</sub>		46.8	A
		V1: 48 V <sub>DC</sub>		23.4	
12 V <sub>SB</sub> Output Voltage	V <sub>SB</sub> output voltage is referred to the same V1 output voltage return	-	12	-	V
12 V <sub>SB</sub> Output Current	Up to 70 °C	-	-	0.3	A
12 V <sub>SB</sub> Ripple & Noise	Peak-to-peak			120	mV
12 V <sub>SB</sub> Line Cross Regulation	V <sub>AC</sub> : 85 – 305 V <sub>RMS</sub> ; I <sub>SB</sub> : 0 – 100%	-	-	±5	%V <sub>SB</sub>
5 V <sub>SB</sub> Output Voltage	V <sub>SB</sub> output voltage is referred to the same V1 output voltage return	-	5	-	V
5 V <sub>SB</sub> Output Current	Up to 70 °C	-	-	0.72	A
5 V <sub>SB</sub> Ripple & Noise	Peak-to-peak			50	mV
5 V <sub>SB</sub> Load, line cross Regulation	V <sub>AC</sub> : 85 – 305 V <sub>RMS</sub> ; I <sub>SB</sub> : 0 – 100%	-	-	±5	%V <sub>SB</sub>

### 3.1 OUTPUT POWER DE-RATING CURVES

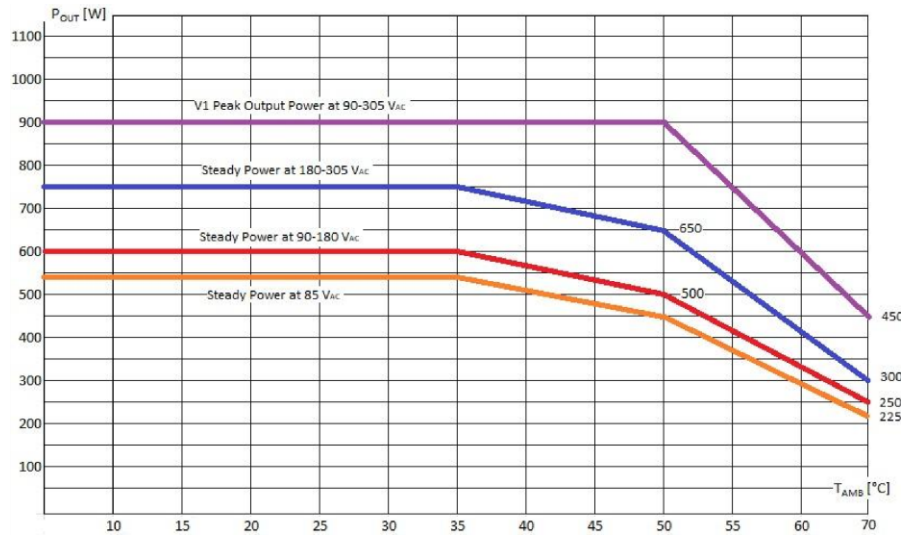


Figure 1 Derating Curves of MCC750 Series V1  $P_{OUT}$  to  $T_{AMB}$

## 4. POWER MANAGEMENT BUS

The MCC750 Series does support communication according to the Power Management Bus 1.2 protocol via SDA, SCL and #SMBALERT signals as defined in the SMBus Specification version 2.0.

The power supply shall not load the SMBus if it has no input power (SCL & SDA lines should go to High-Z).

The pull-up resistors (2.2 k $\Omega$ ) for these signals shall be external to the power supply and referenced to an external +3.3 V bus voltage.

The DSP circuits inside the power supply are powered by the standby output.

The Power Management Bus is active whatever input power is applied to the power supply or a parallel redundant power supply in the system, provided that their 12V<sub>SB</sub> are connected in parallel.

Maximum speed of SMBus is 100 kHz.

The ADDR0 and ADDR1 signals, are inputs to the power supply that control the Power Management Bus address assigned to the power supply.

On the system side, the ADDR0 and ADDR1 signals will either be connected to return through a 1 k $\Omega$  pull-down resistor or connected to +3.3 V external bus voltage through a 1 k $\Omega$  pull-up resistor.

The address shall be derived from the logic of this pin as indicated on Outline Drawing and Connections section.

The power supply is a slave only on SMBus device.

For a comprehensive description of MCC750 Series Power Management Bus management, do refer to the application note, "MCC750 Series Power Management Bus Mgt". The MCC750 Series parameters available through communication bus are:

- Input voltage status
- Output voltages +V1 measured value
- Output current on +V1 measured value
- Current sharing status
- Thermal health measured value
- Fan health status
- Power-On / Working hours
- Product information
- Status information

Failures shall be reported by Power Management Bus for all failure types:

- Protections failure (OV, OC, OT)
- Voltages out of specification