MC-421000A9
1,048,576 x 9-Bit
Dynamic CMOS RAM Module

Description

The MC-421000A9 is a fast-page 1,048,576-word by 9-bit dynamic RAM module designed to operate from a single +5-volt power supply.

The module is functionally equivalent to nine standard 1M DRAMs plus a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles

The MC-421000A9 consists of nine 1M x 1 DRAMs (μPD421000) or two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000). Packaging is in a variety of 30-pin Single Inline Memory Modules (SIMM ™).

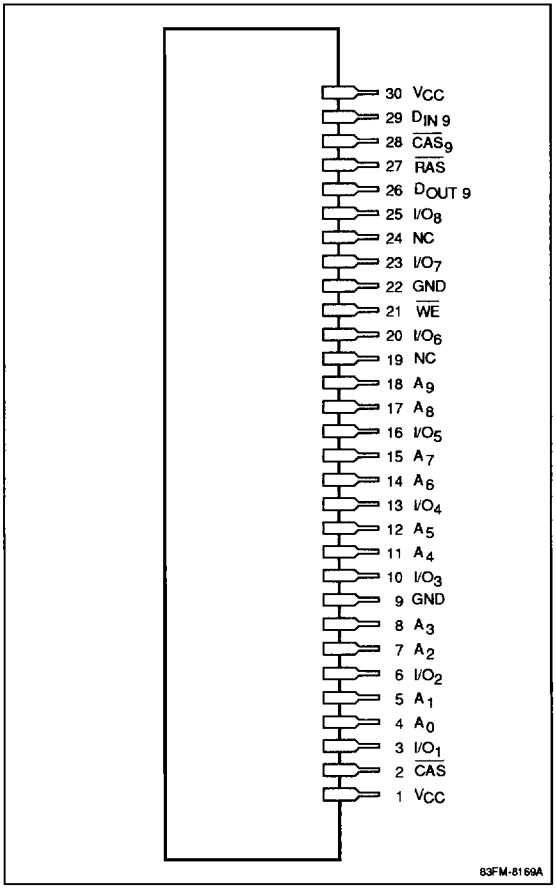
Features

- 1,048,576-word by 9-bit organization
- Single +5-volt power supply
- Standard 30-pin Single Inline Memory Module (SIMM) packaging
- Version 1: nine 1M x 1 DRAMs
- Version 2: two 1M x 4 DRAMs and one 1M x 1 DRAM
- Includes power supply decoupling capacitors
- Low power dissipation
- TTL-compatible inputs and outputs
- Fast-page capability

SIMM is a trademark of Wang Laboratories.

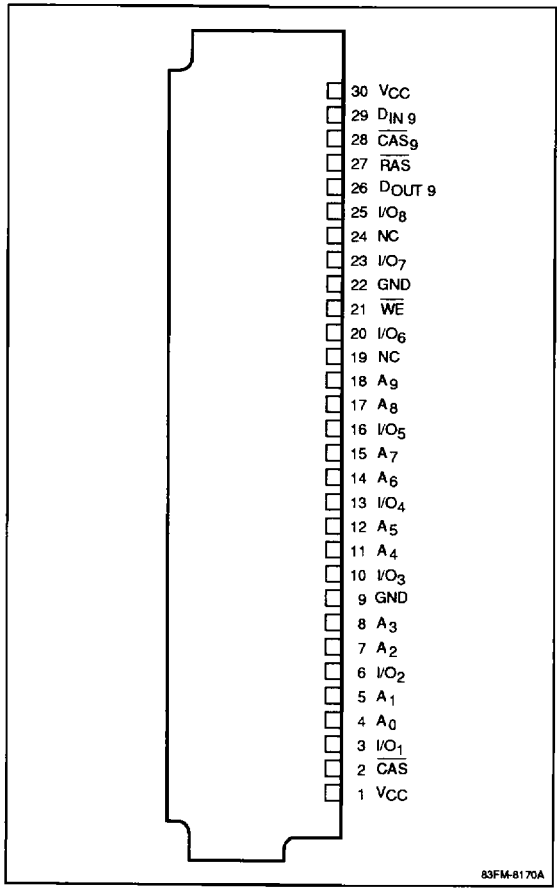
Pin Configurations

30-Pin Leaded SIMM (MC-421000A9A/AA/AB)



Pin Configurations (cont)

30-Pin Socket-Mountable SIMM (MC-421000A9B/BA/BB/F/FA/FB)



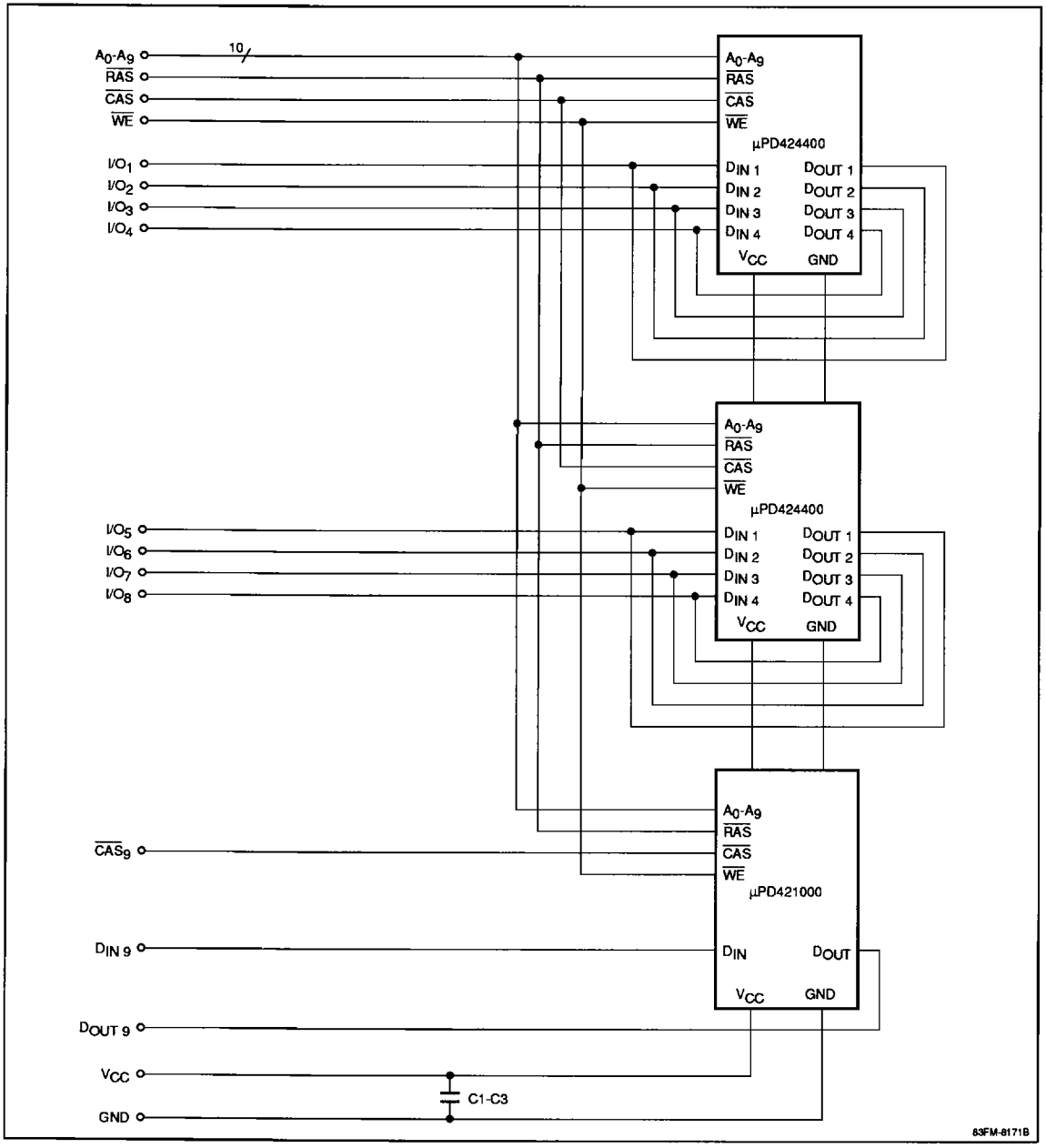
Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

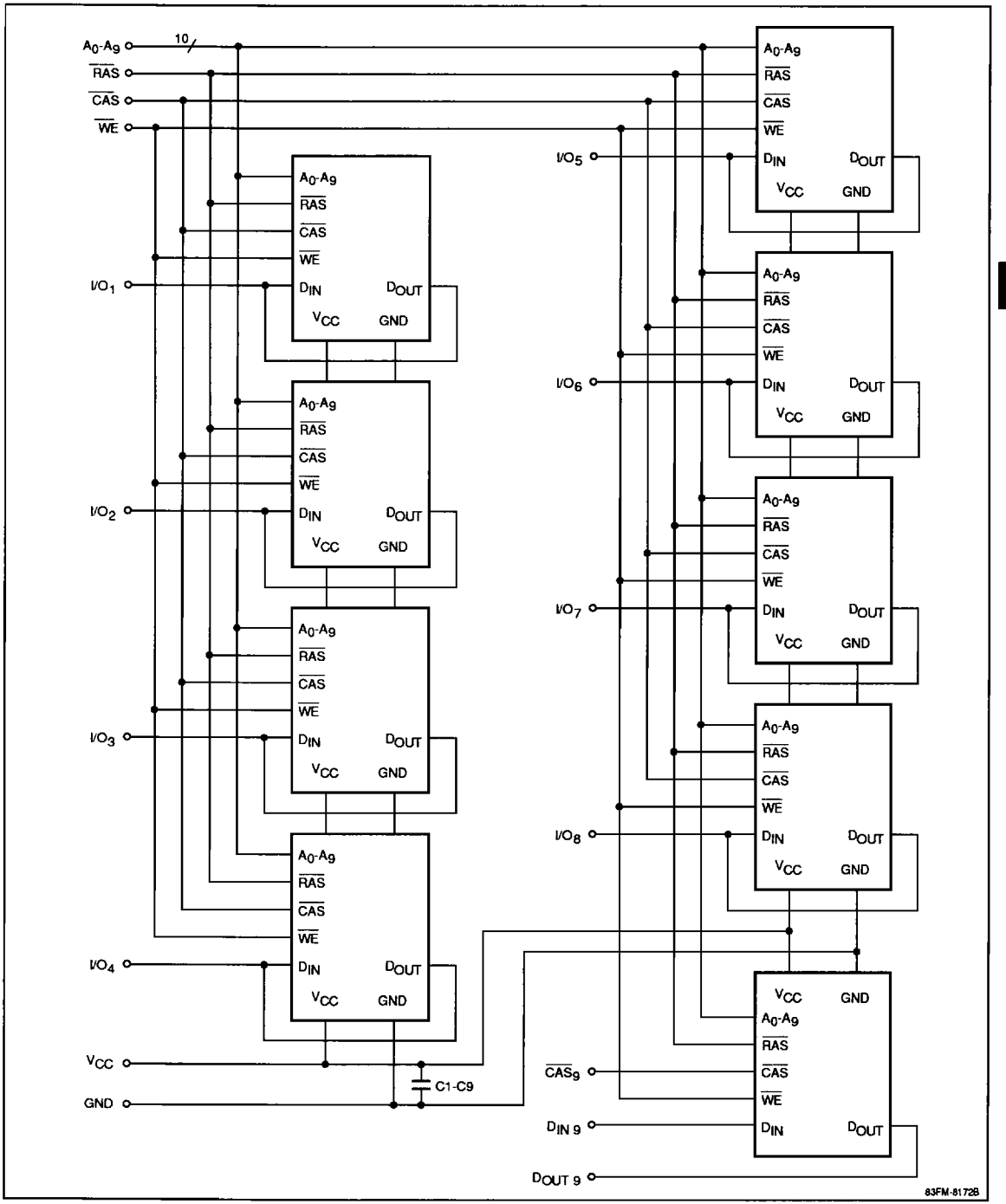
Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-421000A9A-60	60 ns	30-pin leaded SIMM (solder plating)	20.0 mm (0.787 inch)	5.28 mm (0.208 inch)	Nine μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9B-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9F-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9AA-60	60 ns	30-pin leaded SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424400LA One μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9AB-60	60 ns	30-pin leaded SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424400LB One μPD421000LA
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9BB-60	60 ns	30-pin socket-mountable SIMM (solder plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				
MC-421000A9FB-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
-70	70 ns				
-80	80 ns				
-10	100 ns				

Connection Diagram, MC-421000A9AA/BA/FA/AB/BB/FB



Connection Diagram, MC-421000A9A/B/F



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D MC-421000A9A/B/F	9.0 W
Power dissipation, P_D MC-421000A9AA/BA/FA/AB/BB/FB	3.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	MC-421000A9A/B/F	MC-421000A9AA/BA/FA/AB/BB/FB	Unit	Pins Under Test
Input capacitance, max	C_{I1}	70	31	pF	A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	17	pF	$\overline{CAS}_9$, $D_{IN\ 9}$
Input/output capacitance, max	C_D	15	12	pF	I/O_1 - I/O_8
Output capacitance, max	C_O	10	17	pF	$D_{OUT\ 9}$

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current (Note 1)	I_{CC2}			18	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				9	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Standby current (Note 2)	I_{CC2}			6	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				3	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current (Note 1)	I_{IL}	−90		90	μA	For A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$ and $D_{IN\ 9}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current (Note 2)	I_{IL}	−30		30	μA	For A_0 - A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$ and $D_{IN\ 9}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8 and $D_{OUT\ 9}$: D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

Notes:

(1) Applicable to MC-421000A9A/B/F, which consists of nine 1M x 1 DRAMs (μPD421000).

(2) Applicable to MC-421000A9AA/BA/FA/AB/BB/FB, which consists of two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000).

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-60		-70		-80		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1} (Note 21)		810		720		630		540	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
	I_{CC1} (Note 22)		330		280		250		220	mA	
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3} (Note 21)		810		720		630		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
	I_{CC3} (Note 22)		330		280		250		220	mA	
Operating current, fast-page cycle, average	I_{CC4} (Note 21)		720		630		540		450	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
	I_{CC4} (Note 22)		260		230		200		170	mA	
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5} (Note 21)		810		720		630		540	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
	I_{CC5} (Note 22)		330		280		250		220	mA	
Access time from column address	t_{AA}		30		35		40		50	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0		0		ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		40		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}		0		0		0		0	ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10		10		ns	(Note 11)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		15		20		ns	(Note 17)

AC Characteristics (cont)

Parameter	Symbol	-60		-70		-80		-10		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 11)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		140		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		8		8		8		8	ms	Addresses A_0 - A_9 (Note 21)
Refresh period	t_{REF}		16		16		16		16	ms	Addresses A_0 - A_9 (Note 22)
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		165		185		200		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	
Write command	t_{WHR}	15		15		15		20			

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)
Write command	t_{WSR}	10		10		10		10			

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For D_{OUT9}, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS_9}$ returns to V_{IH}) is indeterminate.

(19) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

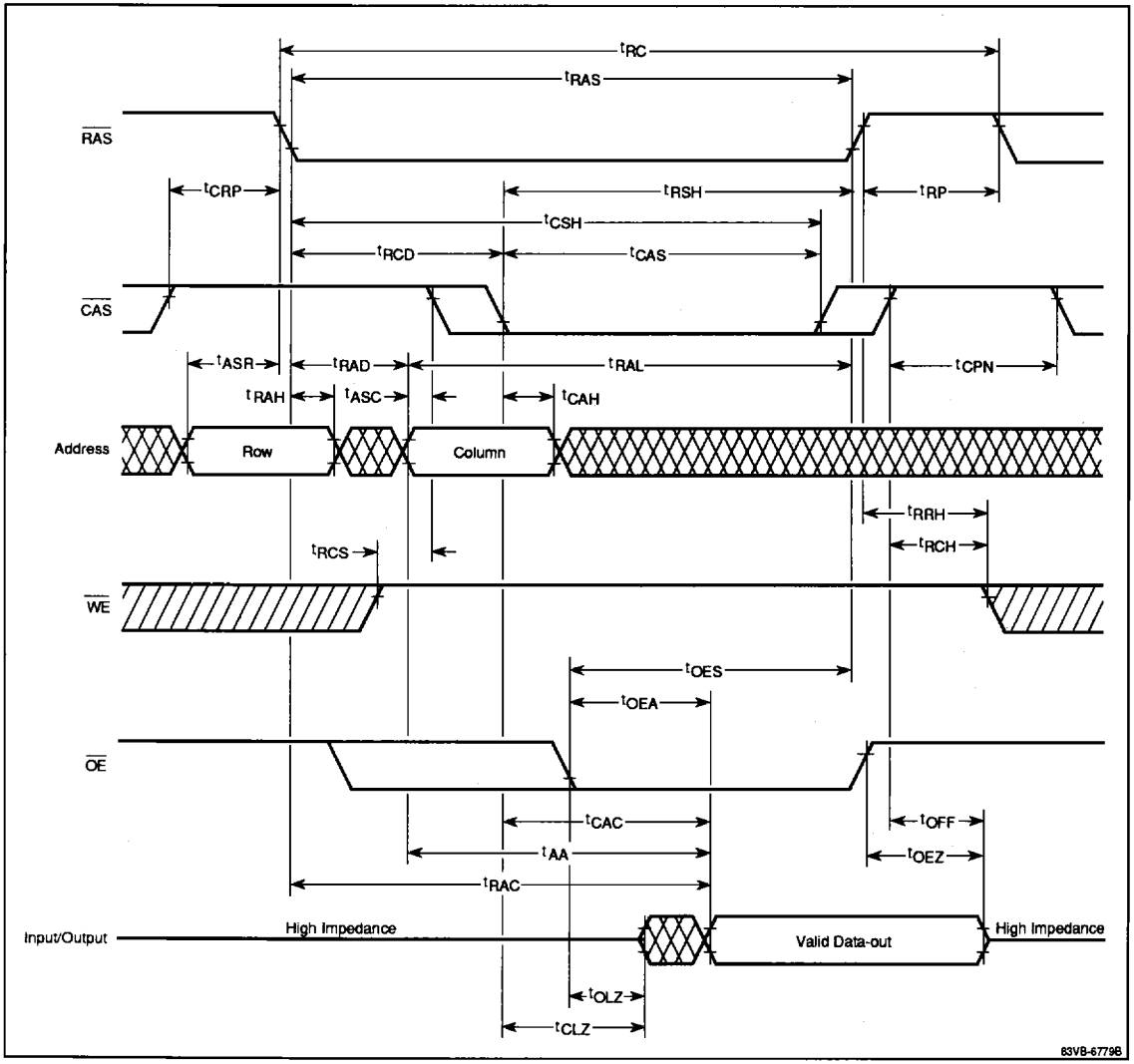
(20) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS_9}$ because of its separate data input and output pins.

(21) Applicable to MC-421000A9A/B/F, which consists of nine 1M x 1 DRAMs (μPD421000).

(22) Applicable to MC-421000A9AA/BA/FA/AB/BB/FB, which consists of two 1M x 4 DRAMs (μPD424400) and one 1M x 1 DRAM (μPD421000).

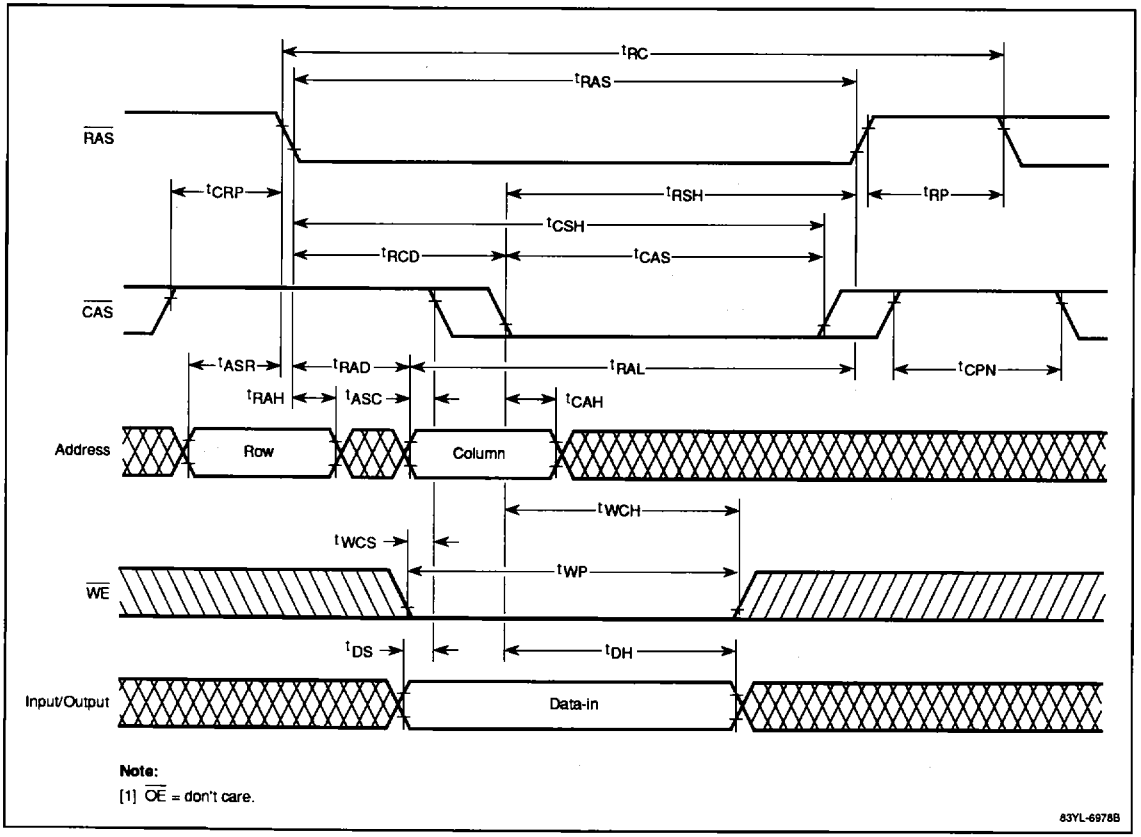
Timing Waveforms

Read Cycle



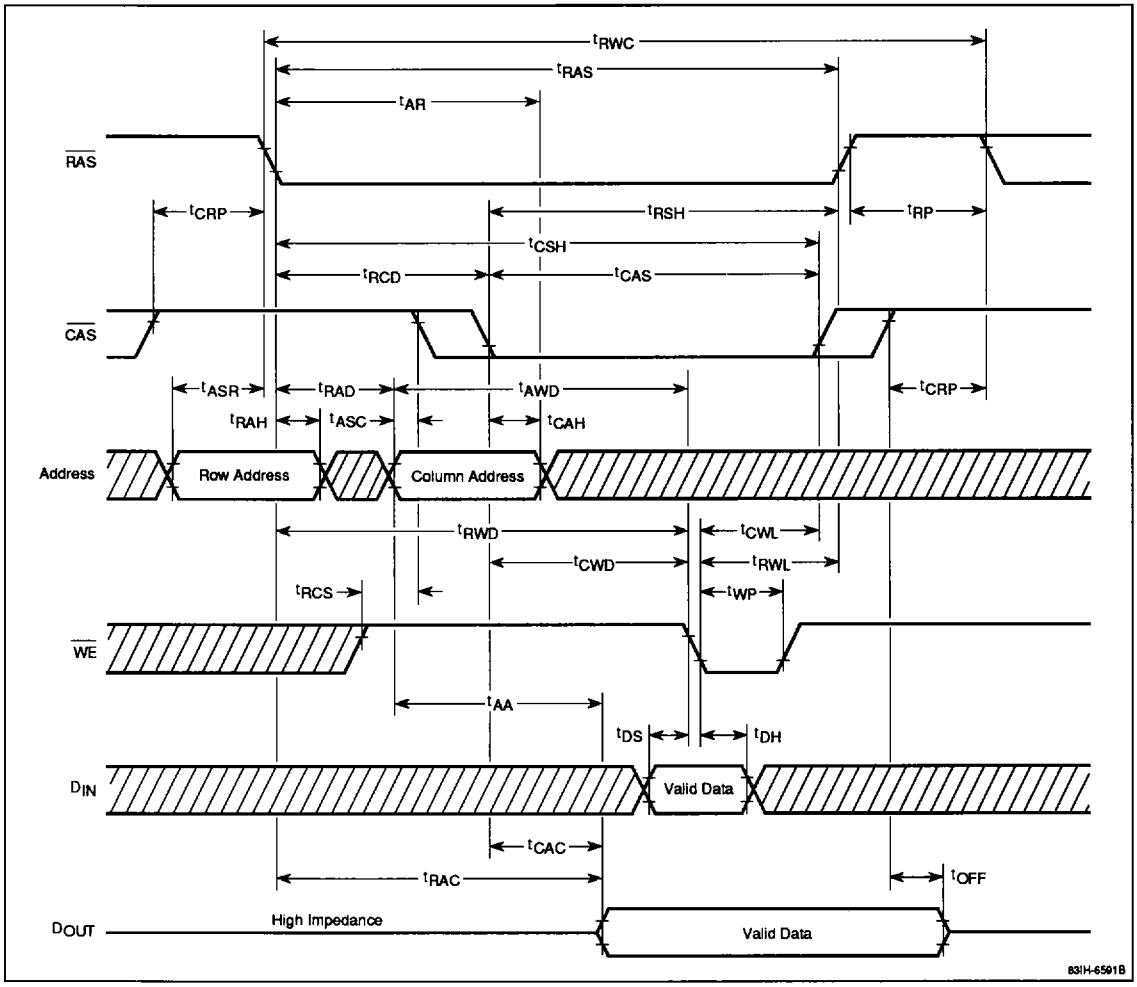
Timing Waveforms (cont)

Early Write Cycle



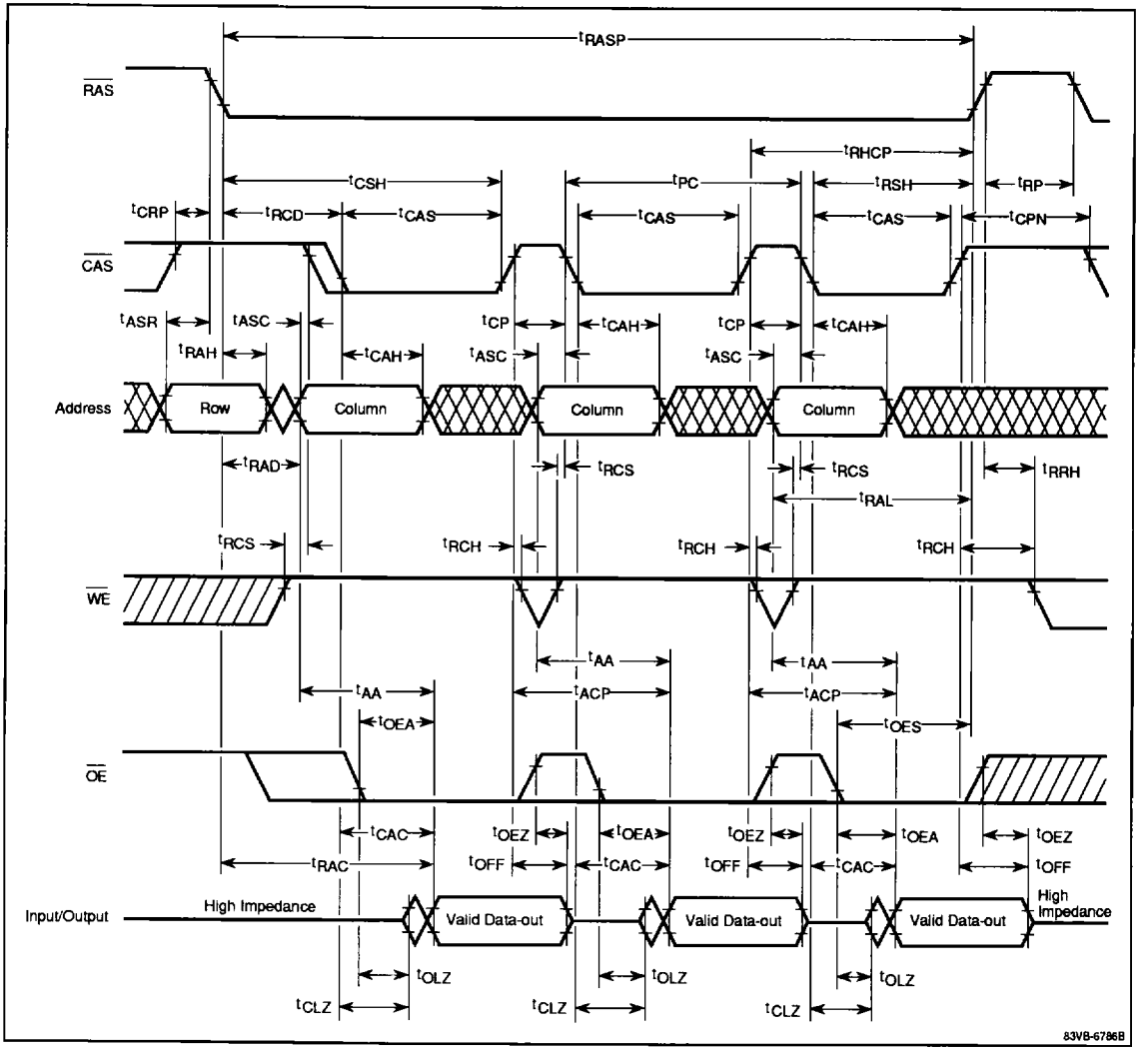
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



Timing Waveforms (cont)

Fast-Page Read Cycle



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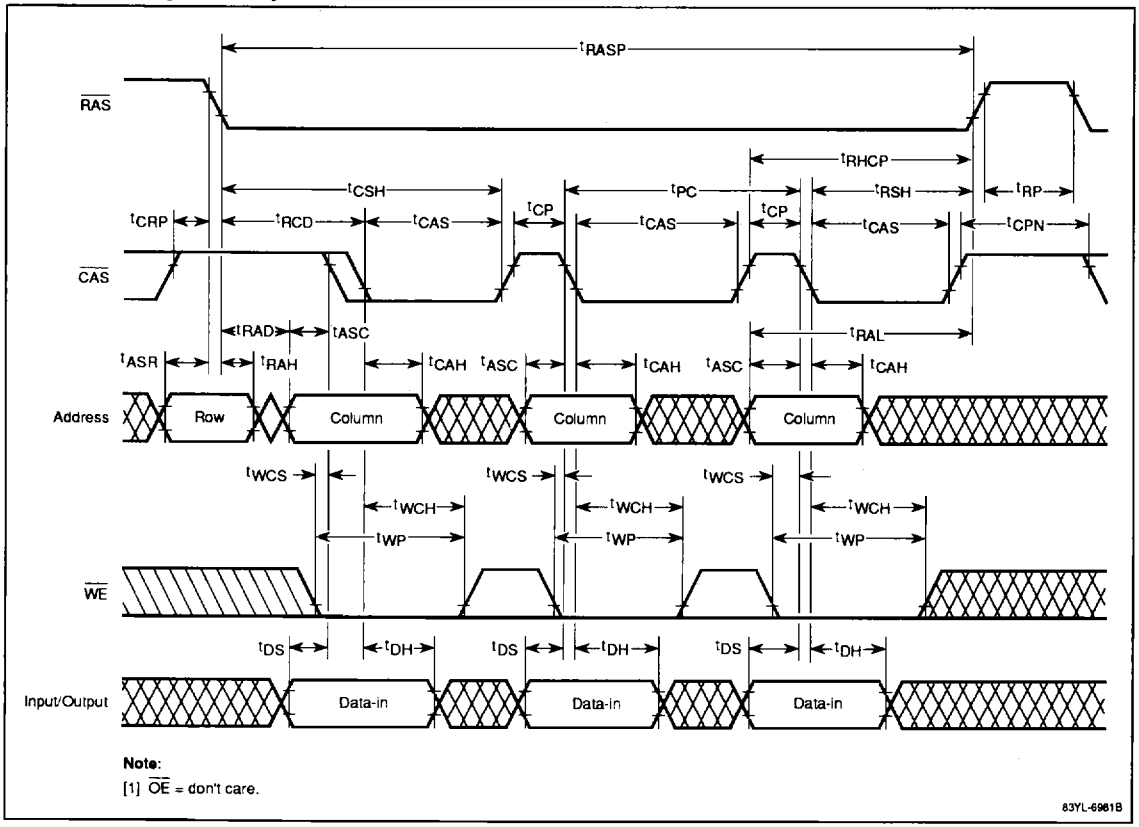
Timing Waveforms (cont)

Fast-Page Early Write Cycle



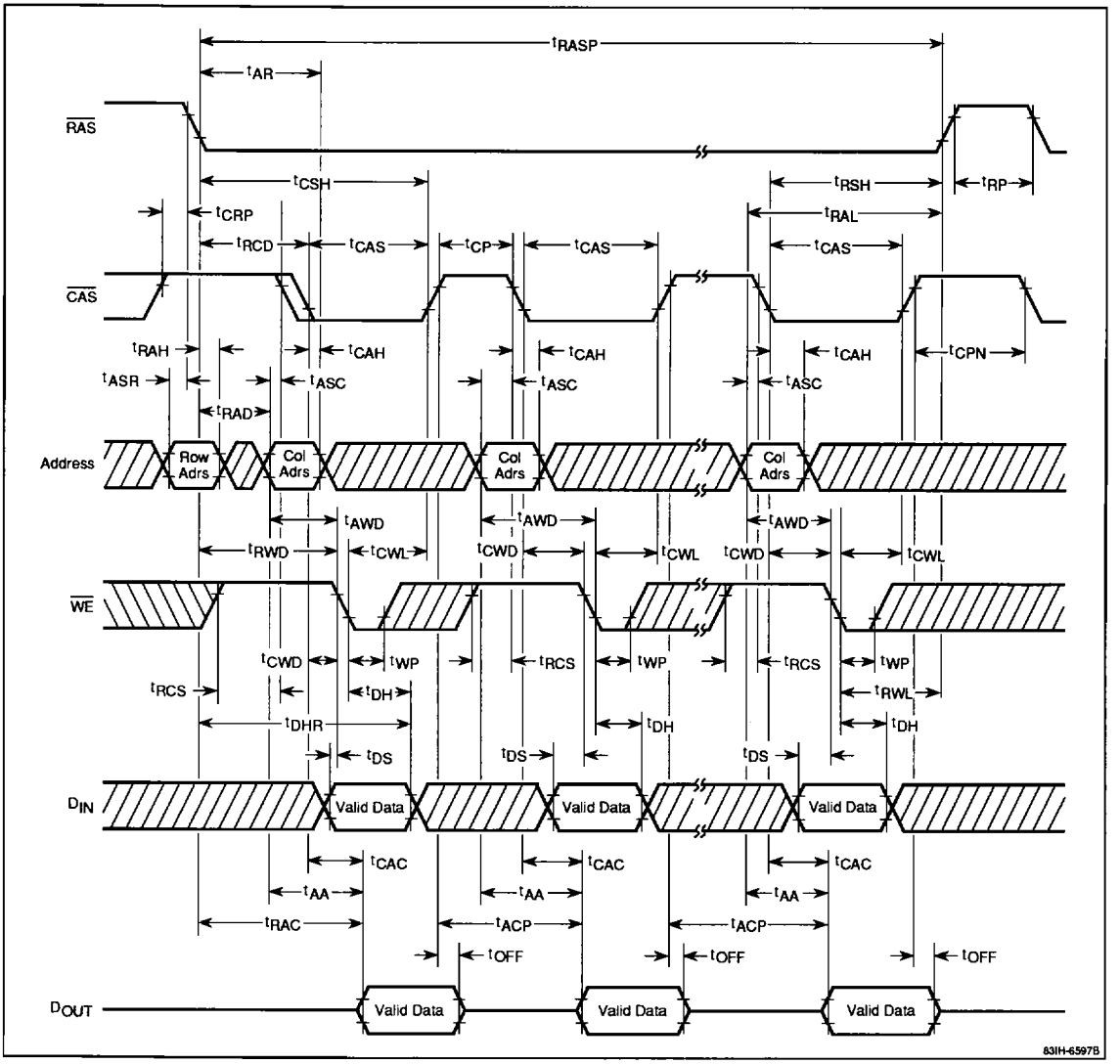
Note:

[1] $\overline{OE}$ = don't care.

83YL-6981B

Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



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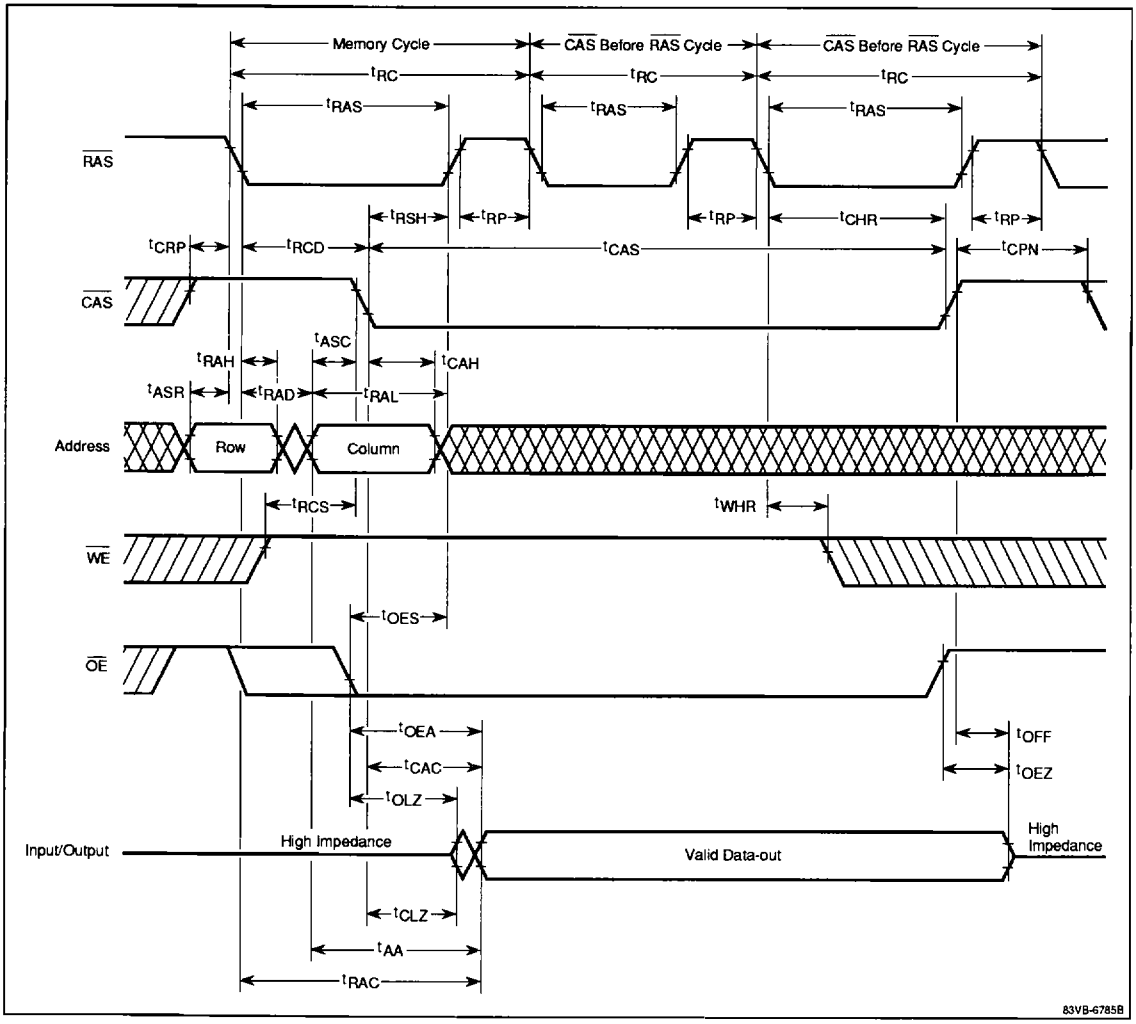
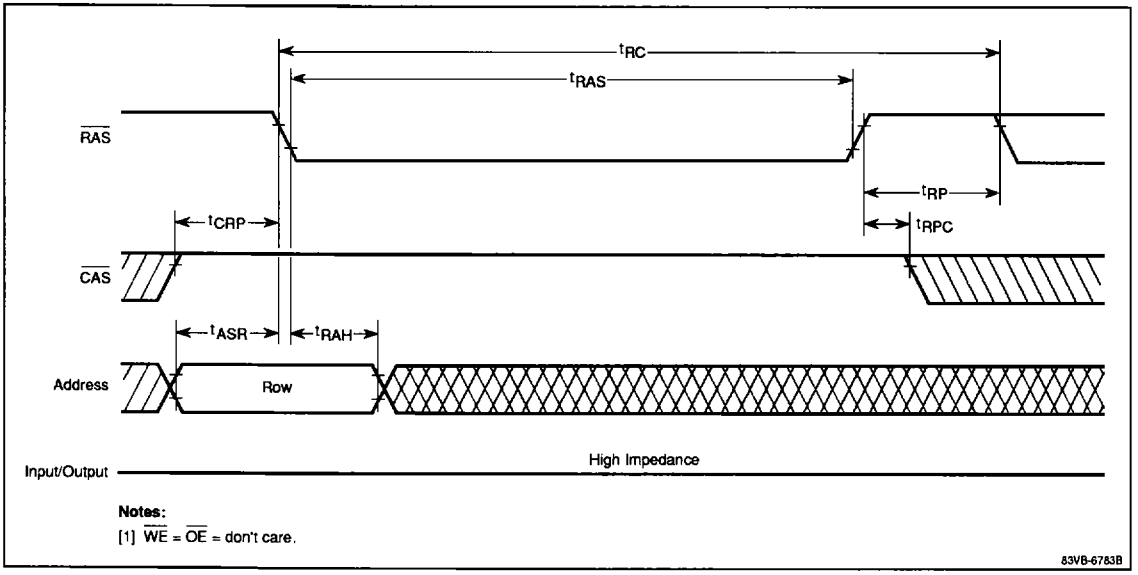
Timing Waveforms (cont)

Hidden Refresh Cycle

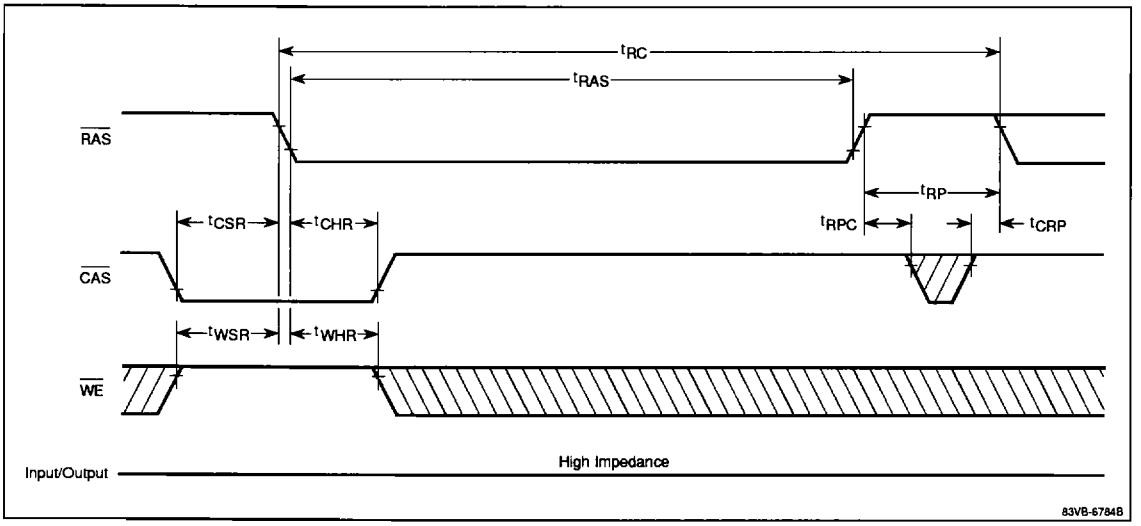


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



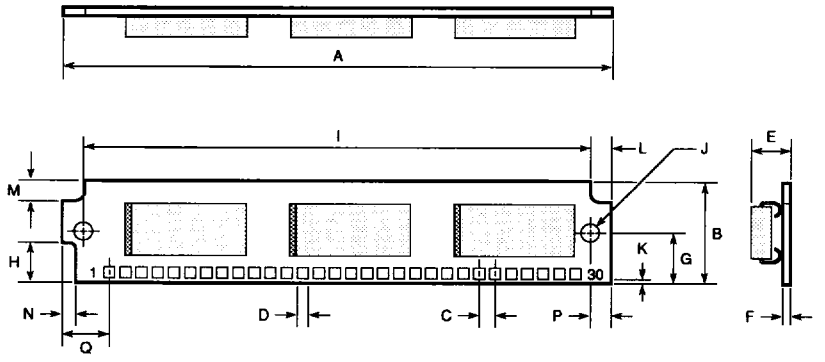
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawings

30-Pin Socket-Mountable SIMM (MC-421000A9BA/FA/BB/FB)

Item	Millimeters	Inches
A	88.9 ±0.5	3.5 ±.020
B	16.67	.656
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ±0.15	.050 ±.006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300

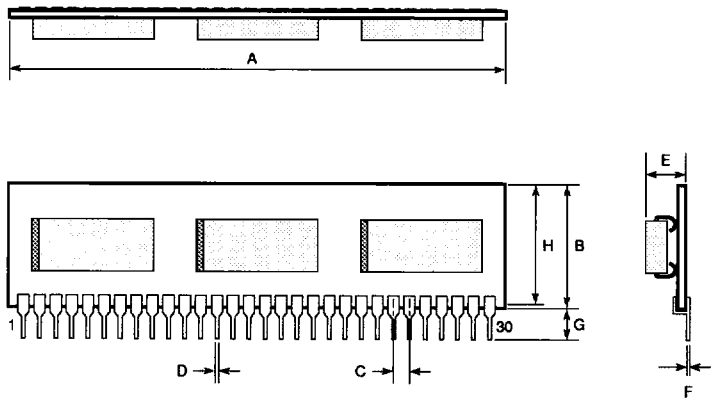


MC-421000A9/BA/FA/BB/FB

83FM-8173B (10/91)

30-Pin Leaded SIMM (MC-421000A9AA/AB)

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	18.27 max	.719 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.208 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	16.67	.656



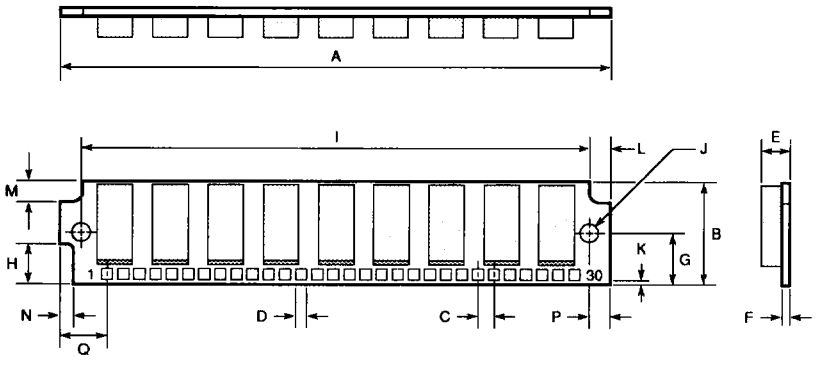
MC-421000A9AA/A9AB

83FM-8175B (10/91)

Package Drawings (cont)

30-Pin Socket-Mountable SIMM (MC-421000A9B/F)

Item	Millimeters	Inches
A	88.9 ±0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ±0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300

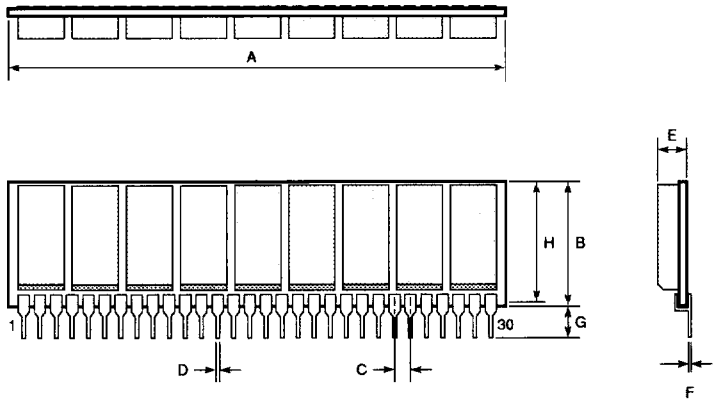


MC-421000A9B

83FM-8174B (10/91)

30-Pin Leaded SIMM (MC-421000A9A)

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 $^{+.021}_{-.020}$
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787



MC-421000A9A

83FM-8176B (10/91)