DATASHEET

HONEYWELL

620-1631

OTHER SYMBOLS:

6201631, 620 1631, 620-1631

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Honeywell

620 Logic Controller System
Model 620-11, 620-14, and 620-16

User Manual

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LIST OF TABLES

USER MANUAL CROSS REFERENCE FOR THE 620-11/14/16 LOGIC CONTROLLER SYSTEMS	
MANUAL:	MATERIAL COVERED:
620-11/14/16 Logic Controller System User Manual Form No. 620-8976	Detailed hardware description; modes of operation; Logic Controller diagnostics; remote serial operation; system configuration; communications detailing ABC and RTU protocol functions; instruction set and opcodes.
620-06 Processor User Manual Form No. 620-8975 620-10 and 620-15 Processor User Manual Form No. 620-8999 620-25 and 620-35 Processor User Manual Form No. 620-8984	Detailed hardware description; specific system configurations (processor and I/O); theory of operation; modes of operation; processor diagnostics; DIP switch settings; instruction sets and opcodes.
623-60 MS-DOS Loader User Manual Form No. 623-8986	Product description and requirements; installation and configuration; system startup and menus; 620 instruction set; edit and display functions; program editing directions; documentation; utility functions.
623-6000 Loader/Terminal User Manual Form No. 623-8987 623-6100/6150 Loader/Terminal User Manual Form No. 623-8940	Hardware and software description; configuration and installation; basic operation (running and loading programs); MS-DOS documentation.
620 Installation User Manual Form No. 620-8996	620 system overview; system configuration for all LCS models; parallel and serial I/O; addressing; rack assembly mounting; module settings (jumpers and DIP switches); module installation; cable and conduit routing; wiring; reference information on superseded model numbers.
620 Control Network User Manual Form No. 620-8994	Control Network overview; hardware description; modes of operation; CNM communications; diagnostics; configuration; DIP switch settings; addressing; installation.
621 I/O Specifications User Manual Form No. 620-8995	I/O system overview; detailed module descriptions (digital input, digital output, special function); serial I/O system; fuse and battery requirements.
620-0048/0052 Data Collection Modules User Manual Form No. 620-8980	Hardware description; theory of operation; instruction set, opcodes and description; installation; wiring; ABC protocol; DIP switch settings.
620-0043 Communications Interface Module User Manual Form No. 620-8986	Hardware description; theory of operation; instruction set; configuration; installation; wiring; DIP switch settings.

INTRODUCTION

The 620 Logic Controller System (LCS) fulfills three important factory automation requirements:

- Control
- Communication
- Monitoring

The 620 Logic Controller System consists of a choice of seven Control Processor Modules, a Universal I/O system, two programming devices, an industrial microcomputer with related software products, motion control products, monitoring products, and communication systems.

This manual covers the use of the 620-11, 620-14, and 620-16 LCSs.

Other 620 LCS products such as the 623-6100/6150 Loader/Terminal, 623-60 MS-DOS Loader, 627-10 microcomputers, motion control products, 620 Control Network, software products, and the other 620 Logic Controller Systems are supported by their own literature.

The User Manual Cross Reference Table at the front summarizes the material covered in other 620 user manuals, which are referenced in this manual.
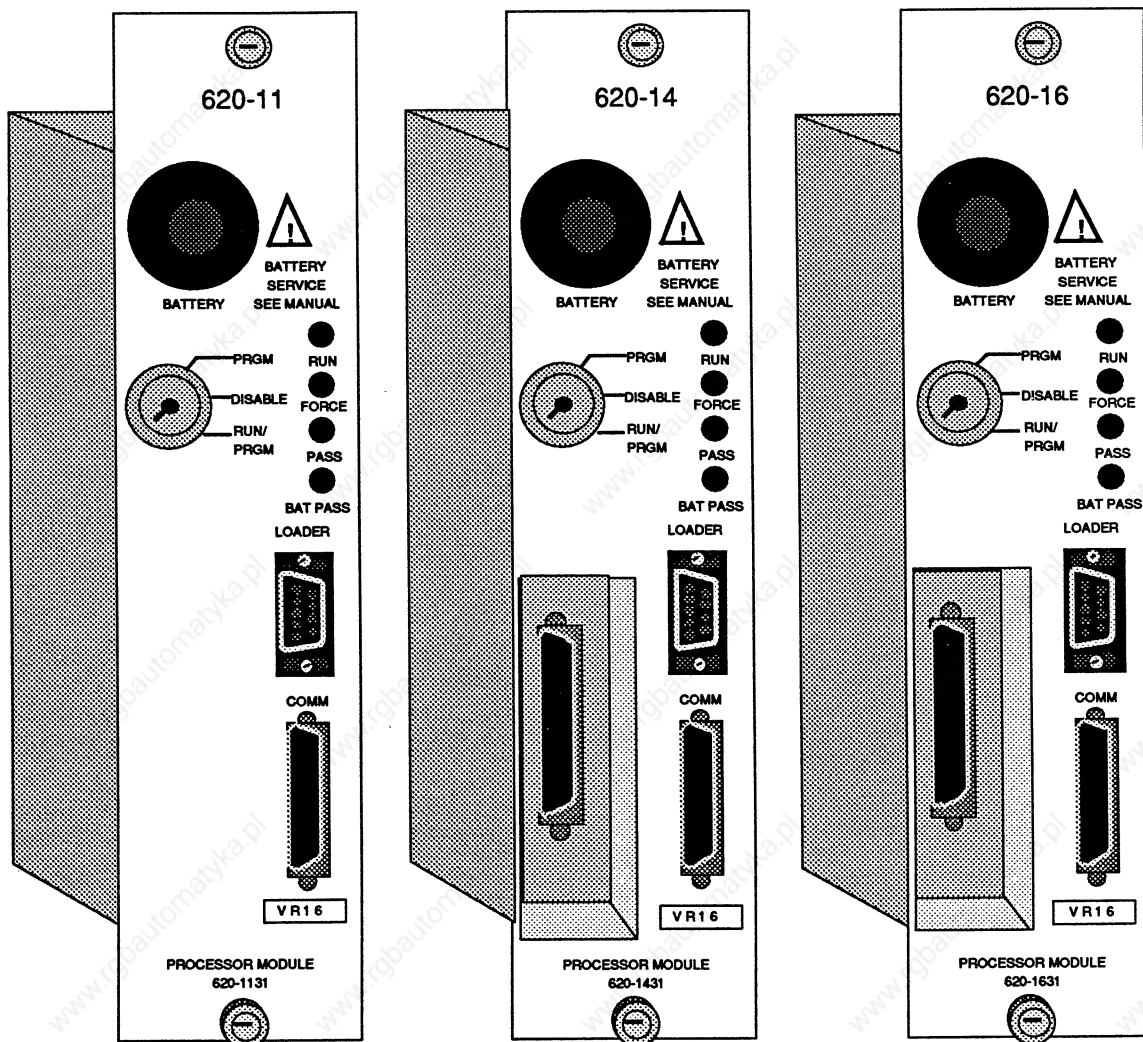
FIGURE 1 - 620-11, 620-14 AND 620-16 CONTROL PROCESSOR MODULES

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HARDWARE DESCRIPTION

SYSTEM SPECIFICATIONS

AC VOLTAGE *.................................115/230± 15% **

FREQUENCY *.................................47 to 63 Hz

DC VOLTAGE *.................................20 to 28VDC

NORMAL LOAD *.................................115 Watts

SURGE CURRENT *.................................15A 1 cycle from cold start

POWER FAIL
LEVEL *.................................115VAC - 85VAC
230VAC - 190VAC
24VDC - 19VDC

POWER FAIL
DELAY *.................................11.5ms (115VAC)
7.0ms (24VDC)

OPERATING
TEMPERATURE *.................................0 to 60°C Ambient

STORAGE
TEMPERATURE *.................................-40 to 85°C
(-40 to 70°C with battery)

RELATIVE
HUMIDITY *.................................5 to 95%
(non-condensing)

HEIGHT *.................................10.7in (27.2cm)

WIDTH *.................................19in (48.3cm)
[I/O half rack 11in (25.4cm)]

DEPTH *.................................7.5in (19.1cm)

REAL I/O CAPACITY
620-1131.................................256 max.
620-1431.................................640 max.
620-1631.................................2040 max.

CONTROL RELAY
CAPACITY
620-1131.................................3840
620-1431.................................3456
620-1631.................................2048

DATA REGISTERS.................................4096

REGISTER SIZE.................................16-Bit

MEMORY SIZES.................................8K words standard

MEMORY TYPE.................................Read/Write CMOS
plus 8K EPROM backup

BATTERY BACKUP.................................1 year minimum

BATTERY.................................Size C Lithium (629-3000)

MEMORY USAGE.................................One word per ladder
diagram element
(Floating Point Constants, JSR, TON and TOF require
two words)

SCAN RATE.................................4.39ms per K (Relay only)
7.05ms per K (Nominal mix)
10.50ms per K (Math intensive)

SYSTEM POWER SUPPLY LOAD
620-1131/1431/1631.................................+5VDC @ 3.0 amps

INDUSTRIAL RATINGS:
NEMA-ICS2-203
IEC 2KV/5KV Isolation Test 255-4
ANSI C37.902a-1974
IEEE 518-1977 (Surge Withstand Test)
UL 508 ***
FM Class No. 3820 ***
CSA C22.2-142-M1983 ****

* Also applies to the 621 I/O system.
** 250VAC maximum (fuse rating).
*** Pending Agency Approval
**** Process Control Equipment rated at 25°C

NOTE
To meet the requirements of Factory
Mutual Research Inc., these Logic
Controller Systems must be installed
in an enclosure that requires a tool for
access. Make sure the area is non-
hazardous and power is removed from
the LCS before changing fuses, removing
or installing modules, or making any
other connections or disconnections.

620-11, 620-14 AND 620-16 LOGIC CONTROLLER SYSTEM COMPONENTS

The 620-11, 620-14 or 620-16 Logic Controller Systems may be ordered as individual components or as a system package. A basic LCS is assembled from the components listed in Table 1. Figures 2 through 5 show processor rack configurations.

The 620-11/14/16 CPMs are double-board, double-width modules that reside in a 620 Processor Rack. The 620-11/14/16 LCSs can also include two option modules in the standard 19-inch processor rack. The 11-inch processor half rack does not accommodate option modules.

The 620-11/14/16 LCSs accommodate eight I/O modules in the standard 19-inch rack and four I/O modules in the 11-inch half rack. A 620-0041, 620-0083 or 620-0046 Power Supply Module is required with each 620-11/14/16 LCS.

Both the 620-14 and 620-16 can support a 621 Slave Rack assembly that will connect 12 additional local I/O modules without the use of a power supply in the I/O rack. This is accomplished by using a special Slave I/O Extender Module and Slave Power Supply Extender Module in the slave I/O rack. The slave I/O rack can be any 621 Universal I/O Rack.

The 620-16 LCS will support processor rack serial I/O through a Serial Link Module that resides in I/O slot H in the 19-inch processor rack. Serial I/O is not supported in the 620-11 and 620-14 LCSs.

TABLE 1 - BASIC 620-11/14/16 LOGIC CONTROLLER SYSTEM COMPONENTS

COMPONENT	MODEL NO.
620-11 Control Processor Module, 8K	620-1131
620-14 Control Processor Module, 8K	620-1431
620-16 Control Processor Module, 8K	620-1631
19-inch Processor Rack	620-1690
19-inch Augmented Processor Rack	620-1693
11-inch Processor Half Rack	620-1692
11-inch Augmented Processor Half Rack	620-1695
Processor Power Supply Module	620-0041/0083/0046
Standard I/O Rack (Slave)	621-9990
Augmented I/O Rack (Slave)	621-9992
I/O Half Rack (Slave)	621-9991
Slave I/O Extender Module	621-9000
Slave Power Supply Extender Module	621-9001
Serial Link Module	621-9939
620-16 Slave Power Supply Cable	628-1600
Parallel I/O Cable	628-2000

620 PROCESSOR RACK

A-H	I/O Module Slots
I-J	Power Supply Slot
K-L	Option Module Slots
M	620-11 Control Processor Module Slot
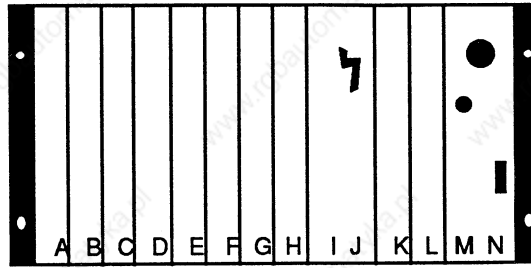
FIGURE 2 - 620-11 RACK CONFIGURATION

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620 PROCESSOR RACK

A-H	I/O Module Slots
I-J	Power Supply Slot
K-L	Option Module Slots
M-N	620-14 Control Processor Module Slot
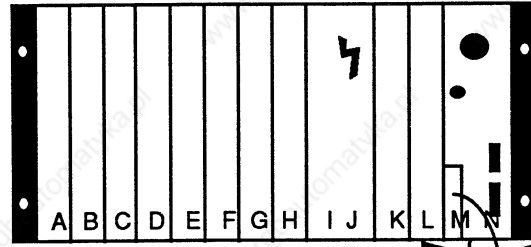
I/O RACK

A-L	I/O Module Slots
M	Slave Power Supply Extender or I/O Power Supply Slot
N	Slave I/O Extender Slot
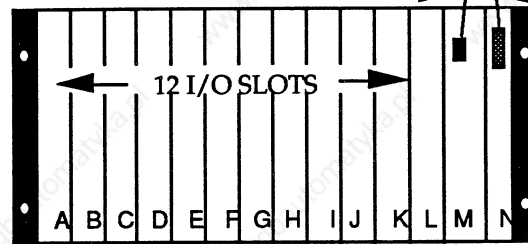
FIGURE 3 - 620-14 RACK CONFIGURATIONS

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620 PROCESSOR RACK

A-G	I/O Module Slots
H	SLM or I/O Slot
I-J	Power Supply Slot
K-L	Option Module Slots
M-N	620-16 Control Processor Module Slot
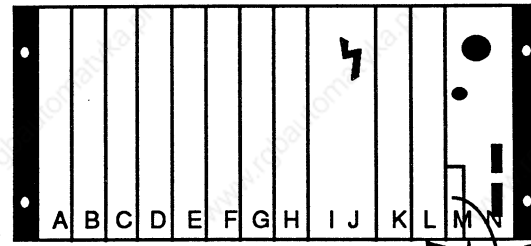
I/O RACK

A-L	I/O Module Slots
M	Slave Power Supply Extender or I/O Power Supply Slot
N	Slave I/O Extender Slot
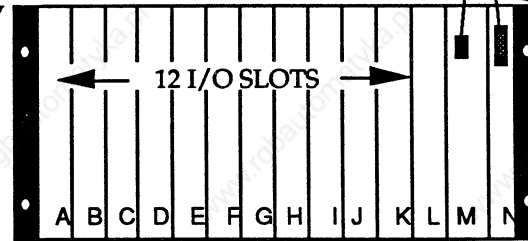
FIGURE 4 - 620-16 RACK CONFIGURATIONS

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620 PROCESSOR RACK

A-D	I/O Module Slots
E-F	Power Supply Slot
G-H	620-11/14/16 Control Processor Module Slot
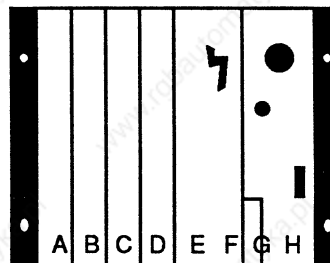
FIGURE 5 - 620-11/14/16 HALF RACK CONFIGURATION

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PROCESSOR RACKS
Model No. 620-1690/1693 - 19-inch
620-1695 - 11-inch

The processor racks include the chassis, backplane, and frontplates for option module slots. The processor rack modules are vertically positioned in the racks with the component side toward the left. Backplane connectors are offset in order to prevent incorrect insertion of a CPM (i.e., upside down or in wrong slots). Card slots (labeled A-M) and the modules that they accommodate are shown in Figures 2–5 and Table 2.

The 620-1093 Augmented Rack includes an additional upper local bus that can be segmented into three separate regions by removing jumpers located on the backplane. An augmented rack is required for the 622 Motion Control System.

The racks fit into an 8-inch NEMA 12 enclosure, or a 19-inch instrumentation rack. The rack fits the European "HE" standard. Reversible mounting brackets allow the rack to be panel mounted. When the brackets are attached to the rack front, it mounts in a standard 19-inch rack. When the brackets are rotated 180° and mounted to the rear, the rack can be panel mounted.

On 620-14 and 620-16 LCSs, the 620-1690 Processor Rack will support processor bus connection to the 621-9990 I/O Slave Rack through a 628-2000 (9-inch) Parallel I/O Cable and a 621-9000 Slave I/O Extender Module.

Also on 620-14 and 620-16 LCSs, the 620-1690 Processor Rack is capable of supplying power to the I/O Slave Rack through a 628-1600 (14-inch) Slave Power Cable and the 621-9001 Slave Power Supply Extender Module.

NOTE
The standard 9-inch 628-2000 I/O cable and 14-inch 628-1600 slave power supply cable are used only when the slave rack is located directly below the processor rack (approximately 5.5 in.).

If the slave rack will be located as much as 50 feet (max.) from the processor rack, a separate I/O Power Supply Module must be installed in the slave rack instead of the Slave Power Supply Extender Module. In this configuration, the 9-inch 628-2000 cable must be replaced by a longer 628-2000 series cable.

The 620-1695 Augmented Half Rack can be used with any 620-11/14/16 Logic Controller. This half rack will accommodate a Control Processor Module (CPM), a 620-0041/0046/0083 Power Supply Module and four standard I/O modules. The 620-1695 Half Racks do not allow option modules, nor do they support power supply connections to an I/O slave rack. Also, the 620-16 CPM cannot support serial I/O when installed in a 620-1695 Half Rack.

TABLE 2 - MODULE CAPACITY, RACK SLOT ASSIGNMENTS

MODULES	SYSTEM QUANTITY (CAPACITY)	PROCESSOR RACK SLOT ASSIGNMENT	
		19-INCH	11-INCH
620-11/14/16 Control Processor Module (CPM)	1	M-N	G-H
Power Supply Module (620-0041, 620-0083 or 620-0046)	1	I-J	E-F
Control Network Module (620-0038)	2	K-L	–
Communication Interface Module (620-0043)	2	K-L	–
Data Collection Module (620-0048 or 620-0052)	2	K-L	–
Access 4000 Master Module (AHM-4000-1)	1	K-L	–
Hiway Interface Module (620-0081)	2	K-L	–
Serial Link Module (621-9939)	1	H*	–
621 I/O Modules	8	A-H	A-D

* 620-16 only

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CONTROL PROCESSOR MODULES
Model No. 620-1131 (620-11 Processor, 8K)
620-1431 (620-14 Processor, 8K)
620-1631 (620-16 Processor, 8K)

The Control Processor Module executes the program stored in the processor's memory and handles all arithmetic and data movement instructions.

The CPM is a double-width, double-board module that is installed in slots M and N of the 620 Processor Rack or slots G-H of the 620 Processor Half Rack. Figure 6 shows the frontplate components of each CPM.

These CPMs are self-contained processors consisting of the logic processor, user program memory, 16-bit user register area and I/O status tables. Incorporated within the module are an integral I/O connector port and communication port.

KEYSWITCH

The 620-11/14/16 CPM frontplate contains a 3-position mode control keyswitch with PROGRAM, DISABLE and RUN/PROGRAM selections.

LED DISPLAYS

There are four LED status displays on the right side of each 620-11/14/16 CPM frontplate. The RUN, PASS and BAT PASS LEDs are green and the FORCE LED is red.

The RUN LED is illuminated and remains lit when the CPM keyswitch is placed in the DISABLE or RUN mode while the CPM is scanning.

The PASS LED is lit when the CPM has successfully completed its self-test. This LED should stay on during normal operation. It is turned off while the CPM is executing diagnostics during a PROGRAM-to-RUN transition.

The BAT PASS LED remains energized as long as the CPM's battery is in good condition and power is applied. The CPM is shipped with the battery installed.

The red FORCE LED is lit when one or more forced contacts within the program is being scanned.

LOADER PORT

Each 620-11/14/16 CPM includes a 9-pin loader port on the right side of its frontplate. This port connects to the 623-6000, and 623-6100/6150 Loader/Terminal or the 623-60 MS-DOS Loader (with software Level of 3.0 or greater) installed on an IBM-compatible personal computer.

COMMUNICATION PORT

Each 620-11/14/16 CPM includes a 25-pin communication port for serial communication with host computers. Through this port, the CPM accepts commands, carries out the data exchange requests, and returns a response to the host computer.

This communication port communicates through RS422/485 interface and supports currently implemented Honeywell ABC and MODBUS RTU protocols. The port provides on-board functions of the 620-0043 Communication Interface Module or the 620-0048 Data Collection Module.

NOTES
This port does not allow the CPM to perform data collection and storage functions associated with Machine Diagnostics.

RS232 communication connections are not supported by the 620-11/14/16 CPMs.

Consult the Communication Port section of this manual for more information.

I/O CONNECTOR PORT

The 620-14 and 620-16 CPMs contain a 50-pin I/O Connector Port located along the lower left-hand side of the frontplate. This port links the CPM with the optional I/O Slave Rack through a 628-2000 I/O cable and a 621-9000 I/O Extender Module that reside in the slave rack. This port extends the processor rack I/O bus to the slave rack.
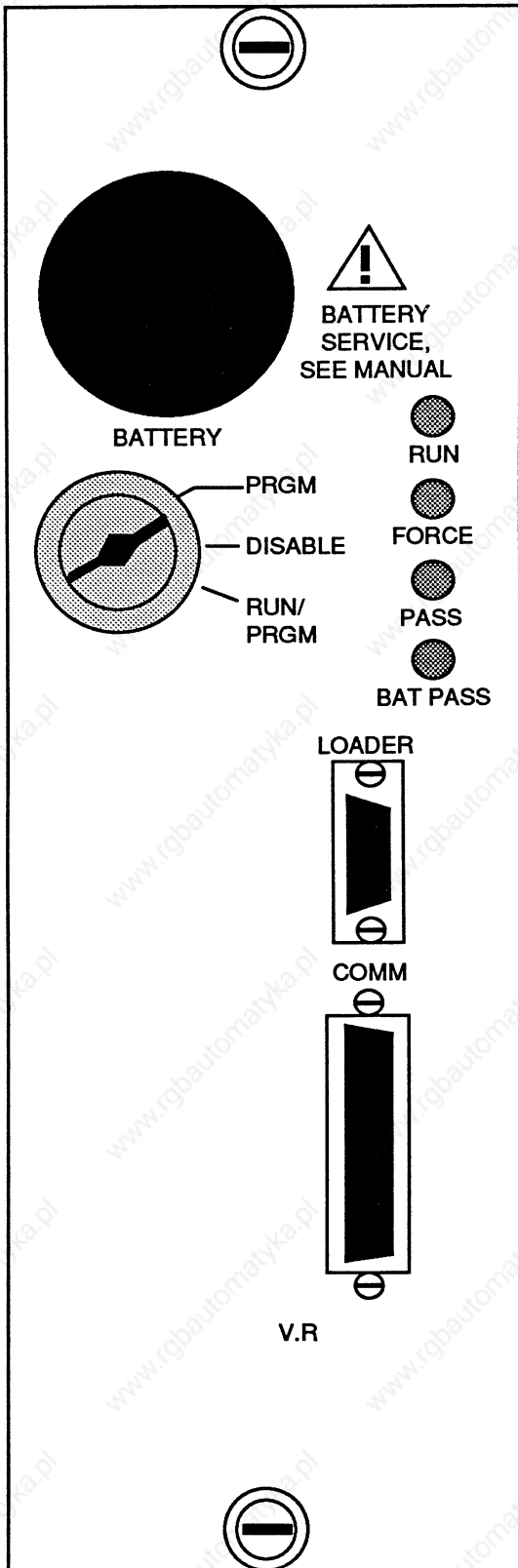
**620-11 CONTROL PROCESSOR
MODULE FRONTPLATE**
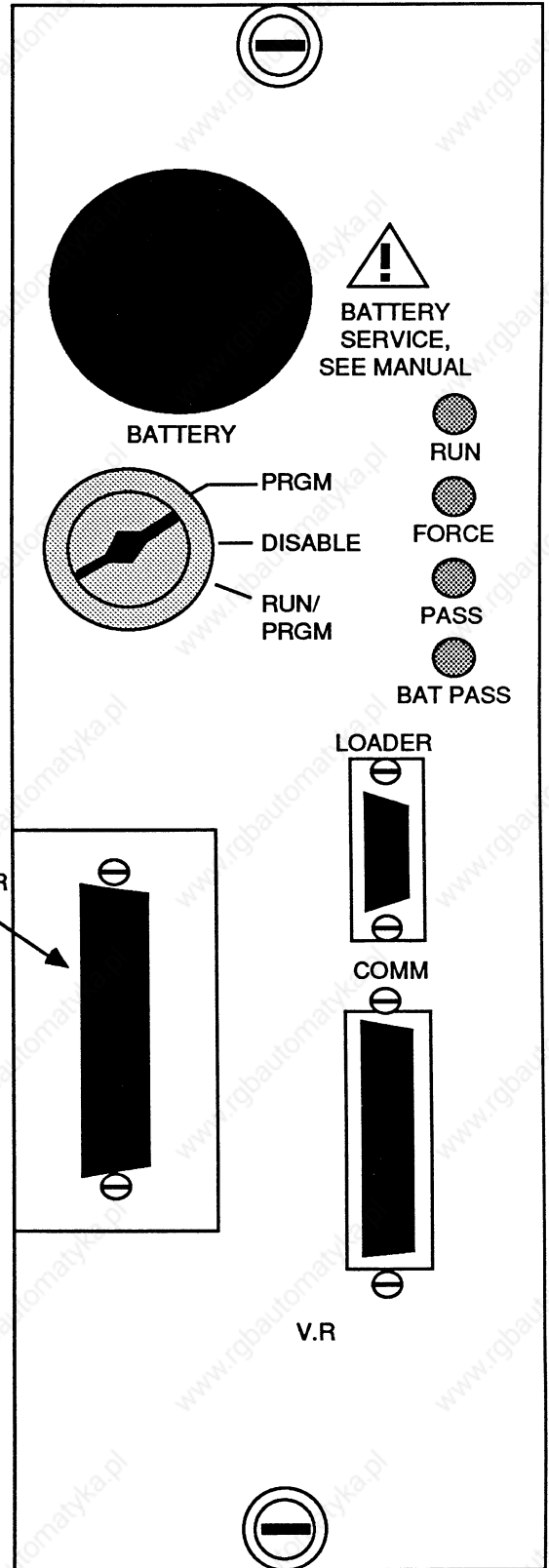
**620-14/16 CONTROL PROCESSOR
MODULE FRONTPLATE**

**FIGURE 6 - FRONTPLATE COMPONENTS OF THE 620-1131, 620-1431 AND 620-1631
CONTROL PROCESSOR MODULES**

BATTERY

The battery compartment in the CPM contains a Size C Lithium battery that provides backup power for internal processor RAM memory and user registers for a minimum of one year. The battery is accessible through a screw-on cover on the upper left-hand side of the CPM frontplate.

NOTE
An insulating wafer prevents battery discharge during shipment and storage and must be removed before the system is operated. See the 620 Installation Manual (Form No. 620-8996) for a figure that shows how to remove the wafer.

The battery compartment is identified on the frontplate of the Control Processor Module with this symbol:

**Battery
Service
See Manual**

Let only qualified personnel service the battery.

CAUTION
Lithium batteries are prohibited from passenger aircraft.

The following conditions are potentially hazardous and should be avoided:

- Recharge
- Incineration
- Short circuit
- Forced overcharge (reversal)
- Use or storage outside of the specified temperature range.
- Puncturing, crushing or disassembling

CAUTION
RAM memory retention is not guaranteed when the Control Processor Module is removed from the rack. Even if the battery remains installed, stray static voltages may occur, resulting in memory changes. In these cases, a checksum fault is detected.

620-1131 - 8K USER MEMORY

The 620-11 Control Processor Module has 8K of user memory words. Each word is 24 bits wide and each ladder element of a logic line uses one word (see Note below). Timer and counter preset and accumulated values are assigned to registers and do not use main memory.

The 620-11 Processor's Output Status Table is contained on the processor board and accommodates the status of 4096 single-bit output elements. The output status of real I/O is contained in locations 0-255. Control relays (internal I/O) statuses are posted at addresses 256-4095, for a total of 256 real I/O and 3840 internal I/O.

Timer and counter presets, accumulated values, and other user data is contained in the Register Table at addresses 4096-8191. These addresses represent 4096 16-bit registers available to the user. Each timer or counter uses two registers for a maximum of 2048 timers and counters combined. Refer to I/O bit and register capacities in Table 3 and the memory map in Figure 7.

620-1431 - 8K USER MEMORY

The 620-14 Control Processor Module has 8K of user memory words. Each word is 24 bits wide and each ladder element of a logic line uses one word (see Note below). Timer and counter preset and accumulated values are assigned to registers and do not use main memory.

The 620-14 Logic Controller System's Output Status Table is contained on the processor board and accommodates the status of 4096 single-bit output elements. The output status of real I/O is contained in locations 0-639. Control relays (internal I/O) statuses are posted at addresses 640-4095, for a total of 640 real I/O and 3456 internal I/O.

Timer and counter presets, accumulated values, and other user data is contained in the Register Table at addresses 4096-8191. These addresses represent 4096 16-bit registers available to the user. Each timer or counter uses two registers for a maximum of 2048 timers and counters combined. Refer to I/O bit and register capacities in Table 3 and the memory map in Figure 7.

NOTE
Floating Point Constants, JSR, TON and TOF instructions use two words of user memory. Floating Point Bring-Ins and Send Outs use two registers.

620-1631 (8K USER MEMORY)

The 620-16 Control Processor Module has 8K of user memory words. Each word is 24 bits wide and each ladder element of a logic line uses one word (see Note below). Timer and counter preset and accumulated values are assigned to registers and do not use main memory.

The 620-16 Processor's Output Status Data Table is contained on the processor board and accommodates the status of 4096 single-bit output elements. The output status of real I/O is contained in locations 0-2039. Control relays (internal I/O) statuses are posted at addresses 2048-4095, for a total of 2040 real I/O and 2048 internal I/O.

Timer and counter presets, accumulated values, and other user data is contained in the Register Table at addresses 4096-8191. These addresses represent 4096 16-bit registers available to the user. Each timer or counter uses two registers for a maximum of 2048 timers and counters combined. Refer to I/O bit and register capacities in Table 3 and the memory map in Figure 7.

NOTE
Floating Point Constants, JSR, TON and TOF instructions use two words of user memory. Floating Point Bring-Ins and Send Outs each use two registers.

TABLE 3 - SYSTEM I/O BIT AND REGISTER CAPACITIES

SYSTEM MODEL & MEMORY SIZE	SINGLE-BIT I/O CAPACITY		16-BIT REGISTERS
	MAXIMUM REAL I/O	MAXIMUM NO. OF INTERNAL CONTROL RELAYS (in addition to real I/O)	
620-1131 (8K)	256*	3840	4096
620-1431 (8K)	640*	3456	4096
620-1631 (8K)	2040*	2048	4096

* Any unused real I/O address may be used as an internal control I/O address.
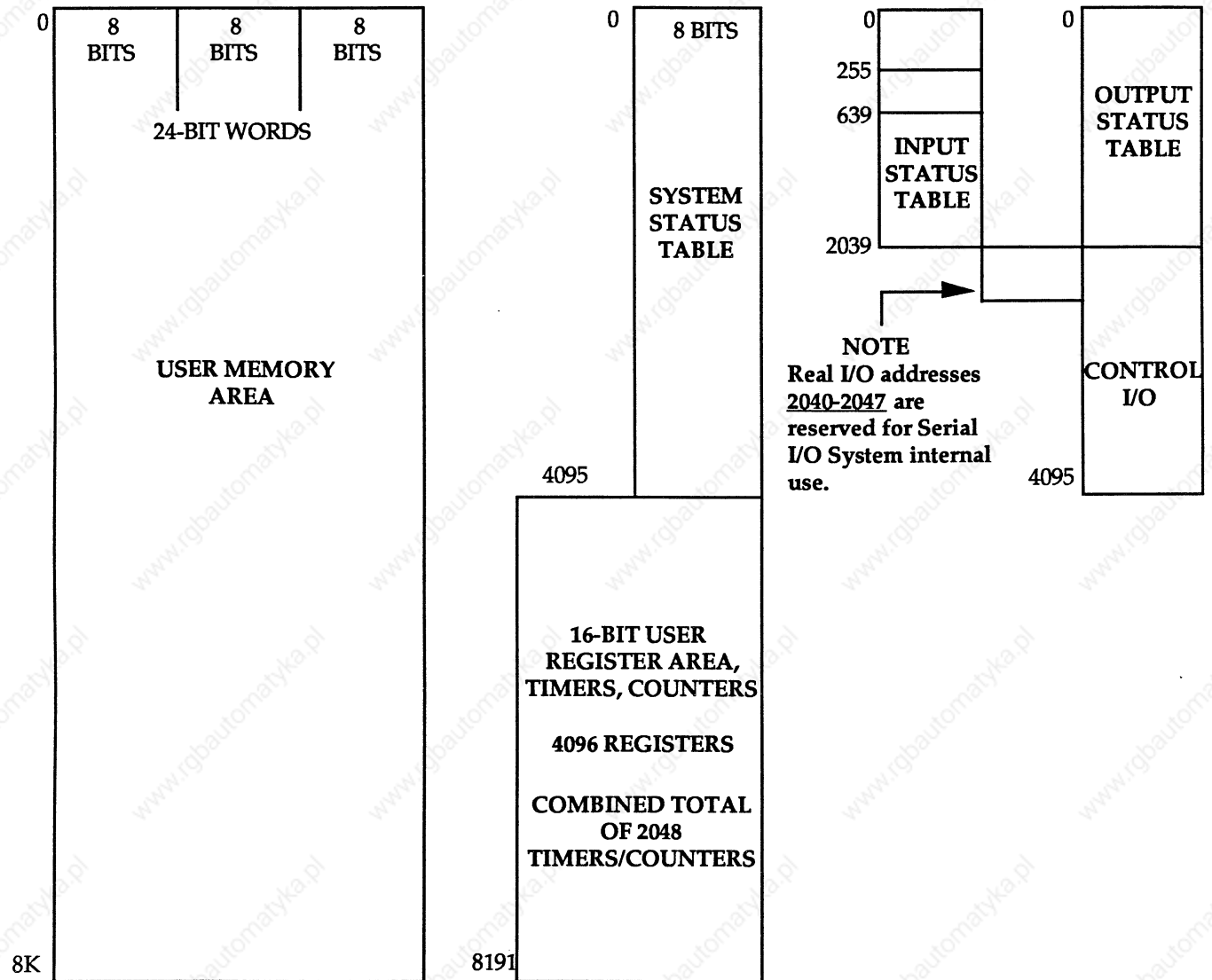
REAL I/O SUPPORTED BY
620-11/14/16 LOGIC
CONTROLLERS

620-1131 = 256 (0-255)
620-1431 = 640 (0-639)
620-1631 = 2040 (0-2039)

FIGURE 7 - 620-11/14/16 LOGIC CONTROLLER SYSTEM
8K SYSTEM MEMORY MAP

POWER SUPPLY MODULES
Model No. 620-0041 (115/230VAC)
620-0083 (115/230VAC)
620-0046 (24VDC)

The Power Supply Module provides power to operate the 620-11/14/16 Logic Controller. It is a double-width module that occupies slots I-J in the standard 19-inch rack and slots E-F in the standard half rack.

Model No. 620-0041

The 620-0041 Power Supply Module provides a maximum of 8 amps of +5VDC power for use by the processor rack modules. It also supplies 600mA of ±15VDC for analog I/O operations. The maximum normal power consumption of the 620-0041 Power Supply Module is 95VA. A power-up will require a maximum of 15 amps for one cycle.

The power supply is selectable for 115 or 230 VAC input by the position of a shorting board located under the module's component cover. The 620-0041 is factory set at 115VAC. The 115VAC selection will allow a voltage range of 85 to 132VAC. The 230VAC selection allows a 170 to 250VAC range of operation. The frequency of both ranges is 47 to 63 Hz.

The 620-0041 offers a front-accessible fuse holder. It is shipped with a 2A Slo-Blo fuse installed for 115VAC operation. The 230VAC 1A Slo-Blo fuse is also shipped with the module. A green LED indicates that 5VDC power is present.

Model No. 620-0083

The input power for this module is selectable for either 85-132VAC or 170-250VAC. The 620-0083 Power Supply Module provides up to 15 amps at +5VDC and up to 1.6 amps at ±15VDC for modules in the processor rack (see Figure 8).

The maximum total output power cannot exceed 90 watts. The maximum normal power consumption of the 620-0083 is 110VA. A power-up will require a maximum of 20 amps for one cycle.

This power supply is selectable for 115 or 230 VAC input by the position of a toggle switch located under the module's component cover. The 620-0083 is factory set for 115VAC. The fuse holder is accessible from the front of the module. It is shipped with a 4A Slo-Blo fuse installed for 115VAC and a 2A Slo-Blo fuse for 230VAC. The green LED indicates that 5VDC is present.

NOTE
Be sure to match the 115/230VAC toggle switch with the module fuse on the 620-0041 or 620-0083 Power Supply Modules.

Model No. 620-0046

The 620-0046 Power Supply Module provides 8 amps of +5VDC for modules in the processor rack. It also supplies 600mA of ±15VDC power. The maximum power consumption of the 620-0046 Power Supply Module is 96VA. A power-up will require a maximum of 40 amps for 1 cycle.

The required input is 20-28VDC with a 24VDC nominal input. This power supply module offers a front-accessible fuse holder and is shipped with an 8A Slo-Blo fuse. A green LED labeled 5VDC is energized when the 5VDC power is present.

620-1690/1693 Slave Power Limitation with the 620-0083 Power Supply Module

Because of a new backplane design in the 620-1690/1693 Processor Racks, a voltage drop can occur when using the 620-0083 Power Supply with the 628-1600 slave power cable and 621-9001 Slave Power Extender in the 620-14/16 CPMs. When the current in the slave power cable exceeds 7 amps, an excessive voltage drop will occur. *This drop will not be detected by the power supply and will result in erratic operation.*

CAUTION
Never use the 620-0083 Power Supply Module in save power configurations with the 628-1600 Slave Power Cable and 621-9001 Slave Power Extender in 620-1690/1693 Processor Racks, an undetected voltage drop can occur.

620-0041/0046 Power Supplies may be used in 620-14/16 slave power configurations.

Available power supply configuration for these Logic Controllers vary. The 620-0041, 0083, or 0046 power supplies are available in the processor rack when a slave rack is not present. The 620-0041 or 0046 power supplies are available in the processor rack with a 628-1600 slave power cable and 621-9001 Slave Power Supply Extender when the power requirements of both the processor rack and slave rack is 8 amps or less. The 620-0041, 0083, and 0046 power supplies are available in the processor rack and any of the 621 I/O power supplies in the slave I/O rack as required, without the 628-1600 Slave Power Cable or the 621-9001 Slave Power Supply Extender.

621 I/O SYSTEM

The I/O system consists of I/O Full or Half Processor Racks, Power Supply Modules, Slave I/O Extender or Serial I/O Modules, and various digital, analog and special function I/O modules.

NOTE
The 620-11/14/16 Logic Controller Systems do not support 621 parallel I/O. Refer to the Slave I/O Extender Module and Slave Power Supply Extender Module descriptions in this section of the manual.

621 I/O FULL RACK
Model No. 621-9990

The 621 I/O Full Rack is identical in size to the 19-inch 620 Processor Racks. It is designed for instal-lation in 8-inch NEMA 12 enclosures or 19-inch instrumentation racks. It holds a maximum of 12 I/O modules; a Slave I/O Extender Module (620-14/16) or Serial I/O Module (620-16 only); and a Power Supply Extender Module or I/O Power Supply Module.

Model No. 621-9992

The 621-9992 Augmented I/O Full Rack is identi-cal to the 621-9990 I/O rack in size and function. It contains an additional upper bus on the backplane to facilitate communication between modules within the I/O rack. This rack is used with modules that require dual bus communication (i.e., Servo Modules).

621 I/O HALF RACK
Model No. 621-9991

The 11-inch Half Rack is approximately one half the width of a full rack. It accommodates a maximum of six I/O modules, a Serial I/O Module or Slave I/O Extender, and a Power Supply Module. The half rack is useful for installation in narrow enclosures such as motor control centers.

I/O RACK POWER SUPPLY MODULES (PSM)
Model No. 621-9932 (8A, 24VDC)

The 621-9932 I/O Rack Power Supply provides 8 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 600mA of $\pm$15VDC power. Refer to the 620 Installation Manual (Form No. 620-8996) for individual module power requirements.

The maximum power consumption of the 621-9932 Power Supply is 96VA. A power-up surge of this power supply requires a maximum of 40 amps.

The required input is 20-28VDC with a 24VDC nominal input. The module offers a front-accessible fuse holder and is shipped with an 8A Fast-blo fuse. A green LED labeled 5V PASS is energized when the 5VDC power is present.

Model No. 621-9933 (15A, 115/230VAC)

The 621-9933 I/O Rack Power Supply is a double-width module that provides 10 to 15 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 1.3 to 2 amps of $\pm$15VDC. The graph in Figure 8 shows the relationship of current loads between the $\pm$15VDC source and the +5VDC source. If, for ex-ample, the $\pm$15VDC source requires 2 amps, the 5VDC can draw a maximum of 10 amps. If the $\pm$15VDC requires 1.3 amps, the +5VDC can draw a maximum of 15 amps. Refer to the 620 Installation Manual (Form No. 620-8996) or individual module specifica-tions for module power requirements.

The maximum power consumption of the 621-9933 Power Supply is 110VA. A power-up surge re-quires a maximum of 20 amps for one cycle.

The input is selectable for 115 or 230VAC by the position of a toggle switch located under the compo-nent cover of the power supply. The 115VAC selec-tion allows a voltage range of 85 to 132VAC. The 230VAC allows a 170 to 250VAC operation. The frequency for both ranges is 47 to 63 Hz. The power supply module offers a front-accessible fuse holder. It is shipped with a 4A Slo-Blo fuse installed for 115VAC operation. The 230VAC 2A Slo-Blo fuse also is shipped with the module. One green LED, labeled 5VDC, is energized when the 5VDC power is present.

NOTE
Be sure to match the 115/230 VAC toggle switch with the fuse of the 621-9932 or 621-9933 I/O Processor Rack power supply modules.

Model No. 621-9934 (8A, 115/230VAC)

The 621-9934 I/O Power Supply provides 8 amps of +5VDC power. This module also provides 600mA of $\pm$ 15VDC power for the operation of some special function I/O and analog I/O modules. It is selectable for 115/230VAC operation, 47- 63Hz.

A terminal block at the top of the module front coverplate is labeled with an A (Line or L1), a B (Common or L2), and a ground symbol for AC input wiring termination. A front-accessible fuse holder houses a 2A Slo-Blo fuse for 115VAC operation. A 1A Slo-Blo fuse for 230VAC operation is also shipped.
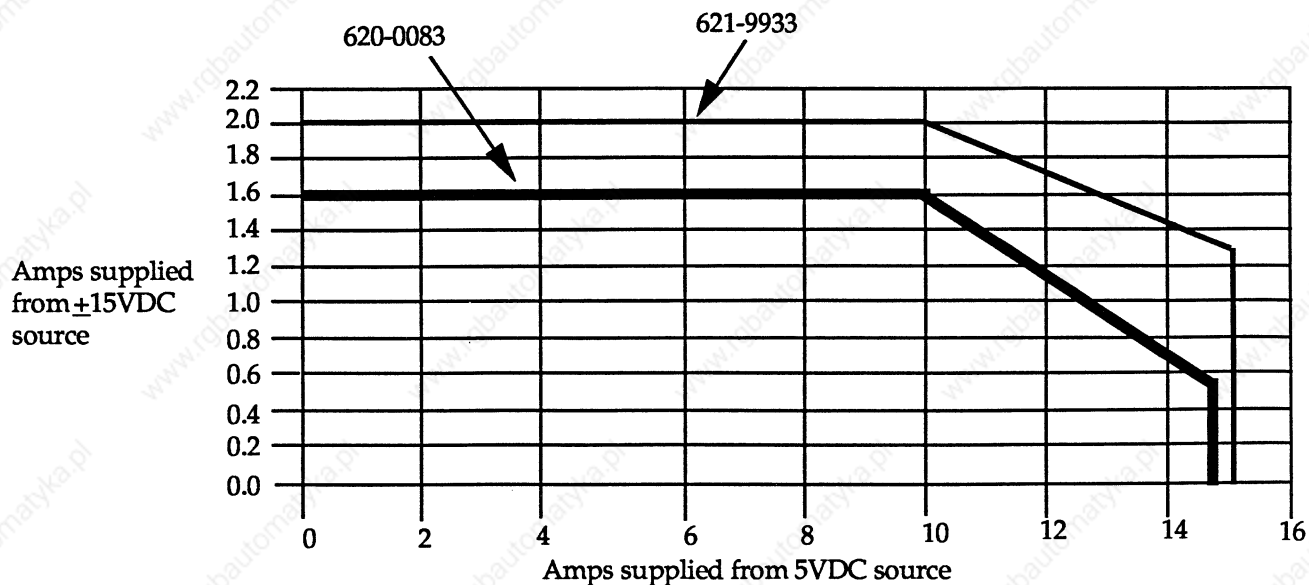
FIGURE 8 - RELATIONSHIP BETWEEN ±15 VDC, +5 VDC SOURCE CURRENT LOADS

SLAVE POWER SUPPLY EXTENDER MODULE
Model No. — 621-9001

The 621-9001 Slave Power Supply Module extends processor rack power to the slave I/O rack. This module can be used only if the slave rack is located directly below the processor rack.

The 621-9001 is located directly beside the I/O Slave Extender Module in the slave rack and is connected to the processor rack backplane through a 14-inch 628-1600 bus power cable. The cable is linked through a 25-pin D-shell connector on the 621-9001 frontplate and a 12-pin connector on the bottom backplane of the processor rack.

NOTE
Because the 628-1600 Slave Power Supply cable is only 14 in. long, the 621-9001 Slave Power Supply Extender Module can be used only when the slave rack is located directly (5.5 in. maximum) beneath the processor rack.

For slave racks located as much as 50 feet (maximum) from the processor rack, an I/O rack power supply module must be installed in the designated 621-9001 slot. Common power supply modules in this type of configuration are the 621-9934 (8 amp AC), 621-9933 (15 amp AC) and the 621-9932 (2VDC).

CAUTION
Never use the 620-0083 Power Supply Module in slave power configurations with the 628-1600 Slave Power Cable and 621-9001 Slave Power Extender in 620-1690/1693 processor racks, an undetected voltage drop can occur.

SLAVE I/O EXTENDER MODULE
Model No. — 621-9000

The 621-9000 Slave I/O Extender Module is a single-width module. It extends I/O a maximum of 50 feet to a slave rack in a 620-14 or 620-16 configuration. The module resides in the right-most slot of the slave rack.

The 621-9000 is linked to the host Control Processor Module through a parallel cable not to exceed 50 feet. The cable (Model No. 628-2000 to 628-2018, depending on length) is attached to the CPM frontplate and the I/O Extender Module frontplate by 50-pin connectors.

INPUT/OUTPUT MODULES

The 621 Universal I/O System has a variety of 8-, 16- and 32- point digital modules, analog, and special function module types. Table 4 provides a complete list of 621 I/O modules.

Double swing terminal blocks that attach to the rack chassis fit over 8- and 16- point modules, splitting the field wiring into two small bundles. One terminal block swings down, closing from the top of the rack, the other swings up, closing from the bottom, both fitting over the installed I/O module. The terminal blocks lock open for easy installation or removal of the module without disconnecting the field wiring.

The 8-point terminal blocks are factory jumpered at T1 and T2 and B1 and B2. The 16-point terminal blocks are factory jumpered at T1, T2, and T3 and B1, B2, and B3. These terminals are field power and return connections and the jumpers select the number of points per common (see Figure 9).

The 32-point I/O modules use two removable connectors that attach to the front of the module. The field wiring is installed in the front of the module using set screws that can be accessed without removing the connector from the module. If a connector must be removed, metal connector bars eject the connectors from the module (see Figure 10).

TABLE 4 - INPUT/OUTPUT AND SPECIAL FUNCTION MODULES

	MODEL NUMBER	MODULE DESCRIPTION
INPUT MODULES	621-0009	Simulator Input Module
	621-0014	Thermocouple/mV Input Module
	621-0020	Universal Analog Input Module
	621-0022-A	Isolated Analog Input, 8 pt. (4-20mA)
	621-0022-V	Isolated Analog Input, 8 pt. (0-10V)
	621-1100	115VAC/DC, 8-pt.
	621-1101	115VAC/DC Isolated, 6-pt.
	621-1160	115VAC, 16-pt.
	621-1180	115VAC, 32-pt.
	621-1200	230VAC/DC, 8-pt.
	621-1201	230VAC/DC Isolated, 6-pt.
	621-1250	240VAC/DC, 16 pt.
	621-1251	240VAC/DC Isolated, 16 pt.
	621-1500	24VAC/DC, 8-pt.
	621-1550	24VAC/DC, 16-pt.
	621-3300	5VDC Sink, 8-pt.
	621-3450	12VDC Sink, 16-pt.
	621-3500	12-24VDC Sink, 8-pt.
	621-3502	12-24VDC Sink Fast Response, 8-pt.
	621-3552	24VDC Sink Fast Response,16-pt.
	621-3560	24VDC Sink, 16-pt.
	621-3580	24VDC Sink, 32-pt.
	621-3600	48VDC Sink, 8-pt.
	621-3650	48VDC Sink, 16-pt.
	621-4300	5VDC Source, 8-pt.
	621-4350	5V TTL, 16-pt.
	621-4500	12-24VDC Source, 8-pt.
	621-4502	12-24VDC Source Fast Response
	621-4550	24VDC Source, 16-pt.

TABLE 4 - INPUT/OUTPUT AND SPECIAL FUNCTION MODULES (Continued)

	MODEL NUMBER	MODULE DESCRIPTION
OUTPUT MODULES	621-0007	Reed Relay, 6-pt.
	621-0010-A	Analog Output, 4-pt. (4-20mA)
	621-0010-V	Analog Output, 4-pt. (0-10V)
	621-2100	115VAC, 8-pt.
	621-2101	115VAC Isolated, 6-pt.
	621-2102	115VAC Source Self-Protected, 8-pt.
	621-2150	115VAC, 16-pt.
	621-2175	115VAC, 32-pt.
	621-2200	230VAC, 8-pt.
	621-2201	230VAC Isolated, 6-pt.
	621-2500	24VAC, 8-pt.
	621-2550	24VAC, 16-pt.
	621-6300	5VDC Source, 8-pt.
	621-6350	5V TTL, 16-pt.
	621-6450	12VDC Source, 16-pt.
	621-6500	12-24VDC Source, 8-pt.
	621-6502	24VDC Source Self-Protected, 8-pt.
	621-6550	24VDC Source, 16-pt.
	621-6551	24VDC Low Power Source, 16-pt.
	621-6575	24VDC Source, 32-pt.
	621-6600	24VDC Source, 8-pt.
	621-6650	48VDC Source, 16-pt.
	621-6700	120VDC Source (0.5A), 8-pt
	621-6701	120VDC Source (2A), 8-pt.
SPECIAL FUNCTION MODULES	621-0006	BCD Converter*
	621-0008	Pulse Input Module
	621-0012	ASCII Communications Module
	621-0016	Controller Access Module
	621-0018	Absolute Encoder Module
	621-0019	Pulse /Quadrature Input Module
	621-0021	Enhanced Diagnostic Module
	621-0307	High Speed Counter
	621-0576	24VDC 24 Sink Inputs, 8 Source Output

*Not required in 620-11/14/16 Logic Controllers that perform BINARY/BCD conversions internally.
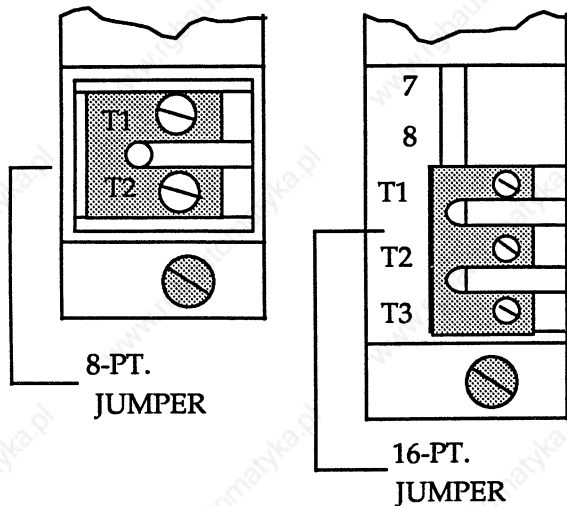
FIGURE 9 - 8- AND 16-POINT TERMINAL BLOCK JUMPERS
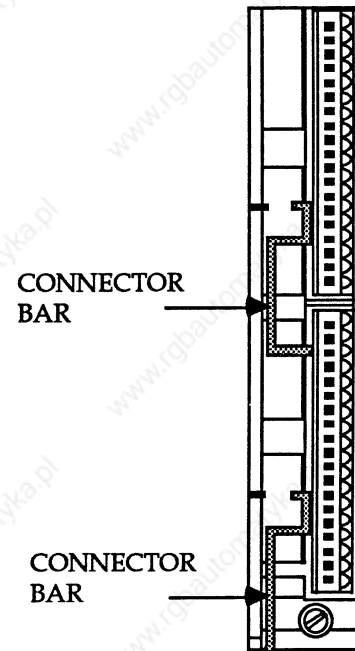
FIGURE 10 - 32-POINT I/O CONNECTORS

SERIAL LINK MODULE (SLM)
Model No. 621-9939

The SLM frontplate has five LED's indicating the status of the LCS. The status of the front panel LED's shows the operating states of the SLM.

The green active light shows that data is being properly transmitted. The light is normally ON during transmission. Each channel has one of these LED's.

Each channel has a yellow link fault LED, which shows that a rack fault or a communication fault has occurred on the channel. This LED is normally OFF. When a link fault occurs, it turns ON. It remains ON while the problem exists unless it is reset.

After the SLM has been reset by shorting the reset terminals at the SLM or had power cycled, the serial system re-initializes. This includes the drops taken off-line (except those that have been manually powered down because of the fault) and the link fault LED is turned OFF.

A DIP switch, SW1, located near the top edge of the circuit board configures the SLM. This module must be used with the 621-9940 SIOM. The SIOM must reside in each rack on the serial link.

SERIAL INPUT/OUTPUT MODULE (SIOM)
Model No. 621-9940

Serial I/O Modules are used in remote serial configurations that allow I/O racks to be mounted close to the machine or process being controlled, eliminating long wire runs. Serial I/O is independent of the Control Processor Module .

The 621-9940 frontplate has six LED's that show the module status. The green active LED shows that the associated port is transmitting and receiving data properly. The light is ON when data is transmitting.

The green pass LED shows the SIOM has successfully completed its self-test, which occurs on power-up and when the SIOM reset terminals are closed. The normal state is ON.

The yellow rack fault LED shows that an output module data fault has occurred. The LED is normally OFF. The statuses of the front panel LED's show the operating state of the SIOM.

Five banks of DIP switches, located near the top edge of the circuit board, set the rack configuration and output handling, and the number of I/O points used in each I/O rack slot.

NOTE
The 620-11/14/16 Logic Controller Systems do not support redundancy.

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COMPATIBLE OPTION MODULES

CONTROL NETWORK MODULE (CNM)
Model No. 620-0038

The 620 Control Network is an easy-to-use, high-speed, peer-to-peer communication network, providing communication between a maximum of eight 620 Logic Controllers. Installing a CNM in the 620-11/14/16 enables the Control Processor Module to communicate with as many as seven other 620 LCSs, transferring I/O status bits or register data between LCSs that are interconnected on a multi-drop, twisted-pair serial link.

Two CNM's may be installed in the 620-11/14/16 full rack configuration (none in the half rack configuration), thus allowing two separate control networks.

COMMUNICATION INTERFACE MODULES (CIM)
Model No.   620-0044 (Honeywell DMCS)
620-0043 (MODBUS RTU)

DATA COLLECTION MODULES (DCM)
Model No.   620-0048 (Honeywell ABC)
620-0052 (Dual-Port Honeywell ABC)

These Communication Interface Modules and Data Collection Modules are optional in the 620-11/14/16 Logic Controller Systems. They provide interface to the 627-10 MiniCOP and host computers supporting asynchronous communication.

For more information, refer to the User Manual Cross Reference Table at the front of this manual. It lists subjects in the CIM and DCM user manuals.

NOTE
The 620-11/14/16 Control Processor Modules feature a communication port that supports both Honeywell ABC and MODBUS RTU protocols. For more information, refer to the Communication Port section of this manual.

HIWAY INTERFACE MODULE (HIM)
Model No. 620-0081

The HIM acts as an interface between a 620 Logic Controller System (LCS) and Honeywell's TDC 3000 Data Hiway. The HIM provides a service facility for higher order devices in the system, such as computers and operator stations to interface with the 620 LCS.

The HIM is a single-slot option module that can be installed in any 620 Processor Rack. The module has the same functional capacity as a maximum of four Data Hiway Port (DHP) modules. It also implements the same point structure as the DHP from the Data Hiway. See the HIM User Manual (Form No. 620-8981) for more information.

ACCESS 4000™ OPERATOR INTERFACE SYSTEM
Model No. AHM 4000

The AHM 4000 Honeywell Master Module is the controlling device for each Operator Interface System. It is a single-width module that resides in an option module slot in a 620 Logic Controller. It conducts communication to peripheral devices through a high-speed coaxial cable link.

Up to 58 devices (Keypad Display Panels or Illuminated Pushbutton Panels) can be linked through the coaxial cable to the AHM 4000 module. This structure, in either a star or multidrop configuration, makes up the Access 4000.

623-60 MS-DOS LOADER

The 623-60 MS-DOS Loader is a software/hardware package that gives any MS-DOS compatible personal computer the capability to program and monitor all 620 Logic Controllers Systems. The Loader can interface with the 620 Logic Controller through a board or external converter, or through a personal computer to LCS adapter. A software Level of 3.0 or greater is required to support the 620-11/14/16 Logic Controller Systems.

623-6100/6150 LOADER/TERMINAL

The 623-6100/6150 Loader/Terminal is a portable hardware platform that has the 623-60 MS-DOS 3.0 Software loaded on the internal hard disk. When power is applied, the unit immediately responds as a 620 Loader/Terminal. A software Level of 3.0 or greater is required to support the 620-11/14/16 Logic Controller Systems.

627-10 MiniCOP

The 627-10 MiniCOP is a module that resides within two or three I/O slots. It interfaces with the Logic Controller System and can read and write inputs, outputs and program memory.

The BASIC09 programming language provides flexibility. It allows the 627-10 MiniCOP to use Logic Controller System (LCS) data. This feature allows communication with color graphic displays, printers, touch panels, card readers, etc; thus providing an efficient man-machine interface.

627 LOCAL OPERATOR STATION

The 627 Local Operator Station, an MS-DOS based, AT-compatible industrial monitor/workstation, gives more monitoring, programming, and control options for the 620 Logic Controller System. It is 19-inch rack-mountable with large memory capability for user programs and data collection. LOS components include: an EGA-compatible monitor; CPU with 1 Mbyte RAM and 20Mbyte hard drive; and choice of external disk drives and keyboards. It accommodates application programs such as Honeywell ScreenWare2, 623-60 MS-DOS Loader software, and PCOS (Process Data Collection and Manipulation). Parallel and serial interface ports and five option slots for interface boards allow more applications, for example RS485 communication.

NOTE
For information on system installation and wiring considerations, see the Communication Port Installation section of this manual.

620-11/14/16 LOGIC CONTROLLER SYSTEM THEORY OF OPERATION

LOGIC CONTROLLER MODES OF OPERATION

The three-position keyswitch on the front panel of the 620-11/14/16 Control Processor Module determines the mode of operation. The three operating modes featured in the 620-11/14/16 Logic Controller System are PROGRAM, DISABLE and RUN/PROGRAM. Refer to Figures 11 and 12 when using this section of the manual.

PROGRAM MODE

The Logic Controller System (LCS) may be placed in the PROGRAM mode using the front panel keyswitch, a Loader/Terminal (L/T), Communication Interface Module (CIM) or the CPM's built-in communication port. When the system is in the PROGRAM mode, the CPM receives commands from the Loader/Terminal, CIM or communication port and executes only those commands. The user program is not scanned, and I/O is not updated.

SOFTWARE PROGRAM MODE

During SOFTWARE PROGRAM mode the Loader/Terminal is used to remotely change the LCS to the SOFTWARE PROGRAM mode when the keyswitch is in the RUN/PROGRAM position.

NOTE
The LCS also may be placed in SOFTWARE PROGRAM mode by CIM's or the on-board communication port.

The system enters the SOFTWARE PROGRAM mode only after the scan being executed is completed. When the Loader/Terminal removes the SOFTWARE PROGRAM mode request, the LCS leaves the SOFTWARE PROGRAM mode and returns to the original mode.

NOTE
A return to RUN/PROGRAM mode is preceded by execution of self-diagnostics and a retentive scan.

SOFTWARE PROGRAM mode changes are made through the Loader/Terminal Mode Change menu. This function is particularly useful in the program debug stage. It allows a quick change from the PROGRAM mode to the RUN mode while operating from the Loader/Terminal keyboard.

PROGRAM MODE SYSTEM STATUS

The RUN LED on the LCS is OFF when the system is in the PROGRAM mode, and the scan loss timer is disabled.

Switching the LCS to the SOFTWARE PROGRAM/PROGRAM mode activates the Clear/Freeze switch setting (F6) on the processor configuration screen. When a mode transition is executed, all outputs will clear or freeze according to the selection option made on the configuration screen.

Switching the keyswitch to another processor mode removes the Control Processor Module from the PROGRAM mode unless the CPM was placed in the PROGRAM mode by the Loader/Terminal, CIM or communication port (SOFTWARE PROGRAM mode). If the system was placed in PROGRAM mode by the Loader/Terminal, CIM or communication port, the PROGRAM mode request must also be removed from the CPM by these devices. Then the LCS can return to the mode of operation specified by the position of the keyswitch.

During PROGRAM mode the 620-11/14/16 Logic Controller's RUN LED is de-energized and the scann loss timer is disabled; indicating no scan loss.

DISABLE MODE

The LCS may be placed in the DISABLE mode by the front panel keyswitch. The DISABLE mode is also the LCS's default mode.

In the DISABLE mode, the Control Processor Module scans through the program. Instruction execution is the same in the DISABLE mode and normal RUN mode operation. It involves collecting field input status, solving the ladder logic program, and posting the outputs in the Output Status Table. Field outputs are cleared or held in the DISABLE mode's last state depending on the selection made in the Processor Configuration Menu (F6).
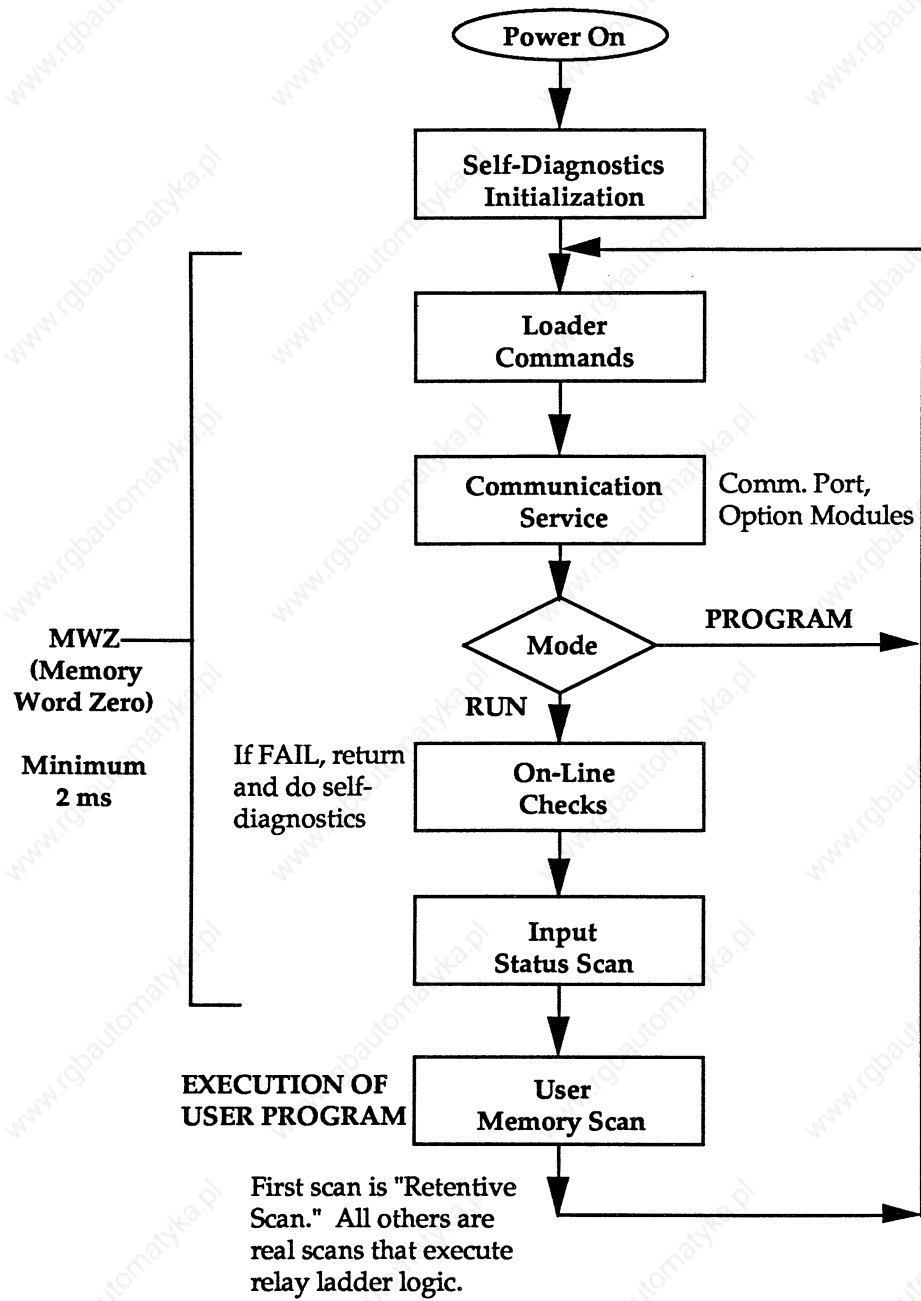
FIGURE 11 - 620-11/14/16 LOGIC CONTROLLER SYSTEM (LCS) EXECUTIVE FLOWCHART

- I/O power fail?
- Keyswitch in PROGRAM mode?
- Keyswitch in RUN mode?
- On-line programming enabled?
- Data change enabled?
- Force enabled?
- Mode request - RUN or PROGRAM?
- I/O configuration requested?

Update Logic Controller System status information

Change since last scan? NO

YES

Change in mode request NO

YES

PROGRAM to RUN Requested:

1) If Remote Power-fail...Do Not Run, Remain in PROGRAM

2) If RUN with low bat disabled and low battery...Do Not Run, Remain in PROGRAM

3) If I/O configuration requested... Do Not Run, Remain in PROGRAM. Otherwise proceed with change to RUN mode.

RUN to PROGRAM Requested

Enter PROGRAM Mode

PROGRAM Mode Request

Remain in PROGRAM Mode

RUN Mode Request:

1) If I/O Power-fail...Change to PROGRAM Mode

2) If I/O configuration requested... Change to PROGRAM mode

3) If I/O configuration complete and no I/O power-fail...RUN mode

4) If I/O power-fail removed and no I/O configuration request... RUN mode

What is Current Mode? PROGRAM

RUN

FIGURE 12 - 620-11/14/16 LOGIC CONTROLLER SYSTEM MODE DECISION BLOCK FROM EXECUTIVE FLOWCHART

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RUN/PROGRAM MODE

The Control Processor Module is in the RUN/PROGRAM mode when the front panel keyswitch is in the RUN/PROGRAM position and SOFTWARE PROGRAM mode is not selected. The RUN/PROGRAM mode is the main control mode for the LCS.

The CPM performs a self-test when it enters the RUN/PROGRAM mode. After the self-test, the system executes a retentive scan, and all non-retentive outputs are turned OFF, including all internal coils. Retentive outputs hold the state of the last scan before being taken out of RUN mode.

After the retentive scan is complete, and it is verified that Input Status Scan (ISS) and End of Memory (EOM) instructions reside in the user program, an ISS begins. The CPM reads from each input module to obtain the present data and examines output card faults simultaneously. If any output card faults are detected in the I/O system, the fault information is inserted in the System Status Table. The ISS operation takes approximately 2ms.

The Control Processor Module then reads and executes the second memory location and continues through the user program. Outputs are updated at the instant the associated output is solved. A Return to Beginning of Program or End of Memory (EOM) instruction causes the scanning sequence to repeat. In this instance, a Return to Beginning of Program is an optional instruction programmed by the user. The EOM instruction is automatically deposited into the user memory at the end of the user program. The ISS instruction is automatically deposited in the first memory location of the user memory.

PROGRAM EXECUTION SEQUENCE

Assume that the CPM has now completed the ISS and is ready for the actual program execution. (See Figure 13). Using the sample represented by the following logic lines, program execution would be as follows:

```
    101       67                    32
|--] [----] [----------------( )--------
|
    32       242                   384
|--] [----] [----------------( )--------
```
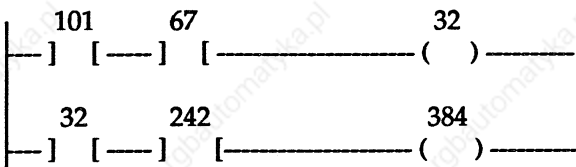
1. The first instruction (-] [- at address 101) is read from memory, which causes a logical OR to be performed on the binary digit stored at address 101 in the Output Status Table of the CPM and the binary digit read from the Input Status Table.

   Assuming that input contact 101 is closed, a binary 1 is read from the Input Status Table at address 101. All non-retentive Output Status Table bit addresses were cleared to zero during retentive scan, so the OR operation will result in a 1 (input contact 101 true).

2. The next instruction (-] [- at address 67) is brought from memory and a logical OR peformed on the Input Status Table and the Output Status Table at address 67. Assuming that input contact 67 is closed, a binary 1 is read from the I/O card at address 67.

3. The next instruction (-( )- at address 32) is brought from memory. The CPM recognizes that output 32 must be turned ON since both input contacts 101 and 67 are closed (OFF). The LCS transmits a signal through the field I/O bus to energize output 32 and also posts a binary 1 in bit address 32 of the Output Status Table.

4. The next instruction (-] [- at address 32) is brought from memory and a logical OR is performed on the Input Status Table and the Output Status Table at address 32. Bit address 32 in the Input Status Table is read as 0, but a binary 1 was posted at address 32 in the Output Status Table as a result of the previous instruction. The result of the logical OR is a binary 1 (contact 32 true).

5. The next instruction (-] [- at address 242) is brought from memory, and a logical OR performed on the Input Status Table and the Output Status Table at address 242. Assuming that input contact 242 is open, 0 is read from the Input Status Table at address 242.

6. The next instruction (-( )- at address 384) is brought from memory. The CPM recognizes that contact 32 is true, but contact 242 is false, therefore, output 384 must be de-energized. The CPM transmits the signal through the field I/O bus to de-energize output address 384 and posts a 0 in bit address 384 of the Output Status Table.

7. The remainder of the instructions are executed until the End of Memory instruction is reached. The EOM ends execution of the user program and causes a return to Memory Word Zero (MWZ). Overhead operations are performed until the next scan of the user program is finished.

RUN/PROGRAM MODE STATUS

The RUN LED located on the CPM is ON when the CPM is in the RUN/PROGRAM mode. A scan-loss timer is reset on each scan. It performs a diagnostic function by timing each scan. If the scan loss timer is enabled and the scan runs beyond the timer's limit, it has "timed out." When a scan-loss timer times out, the CPM stops executing the user program and may clear or freeze outputs in the I/O system. The clearing of outputs is performed according to selection (F6) made in the Processor Configuration Menu. A time-out causes the RUN LED to turn off. If the scan-loss timer has not reached its time-out setting before the end of the scan, the processor continues with the next scan thus resetting the timer.

Some valid ladder logic programming will cause the scan time to exceed the time-out setting. The user can enable or disable the scan loss timer with selection F5 on the Processor Configuration Menu.

NOTE
All system diagnostics are performed whether the scan loss timer is enabled. However, an enabled scan loss timer provides an additional level of system check.

The CPM can be removed from the RUN mode by moving the keyswitch to another position or by entering a SOFTWARE PROGRAM mode request command from the Loader/Terminal, Communication Interface Module or on-board communication port. Note, however, that the Loader/Terminal security code must be passed before the Loader/Terminal actually performs a processor mode change from RUN to PROGRAM. When the CPM receives a SOFTWARE PROGRAM mode request, it enters the SOFTWARE PROGRAM mode after the scan returns to the first location in the memory. The CPM stays in the SOFTWARE PROGRAM mode until the Loader/Terminal, CIM or communication port removes it.

In the RUN/PROGRAM mode, element status may be forced by the Loader/Terminal. This can happen if; a) the force functions are enabled by switch (F2) in the Processor Configuration Menu; b) preset and accumulated values of timers and counters are changed by the Loader/Terminal; c) and data change functions are enabled by switch F4 on the Processor Configuration Menu.
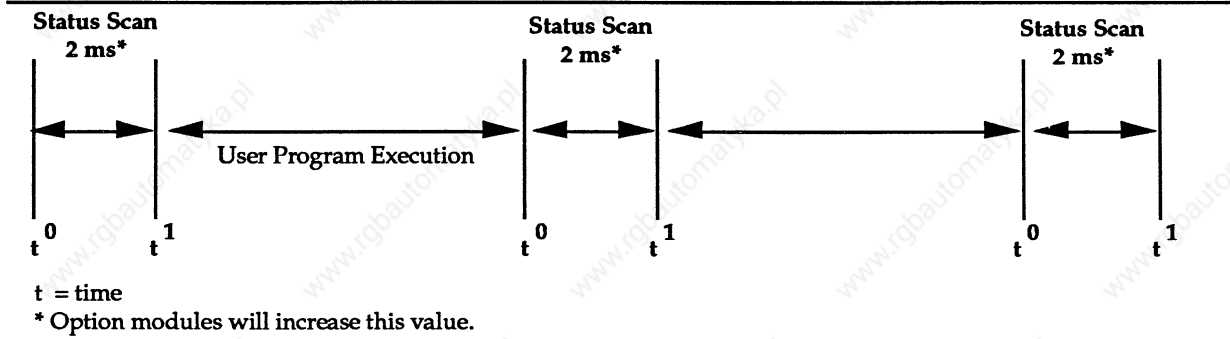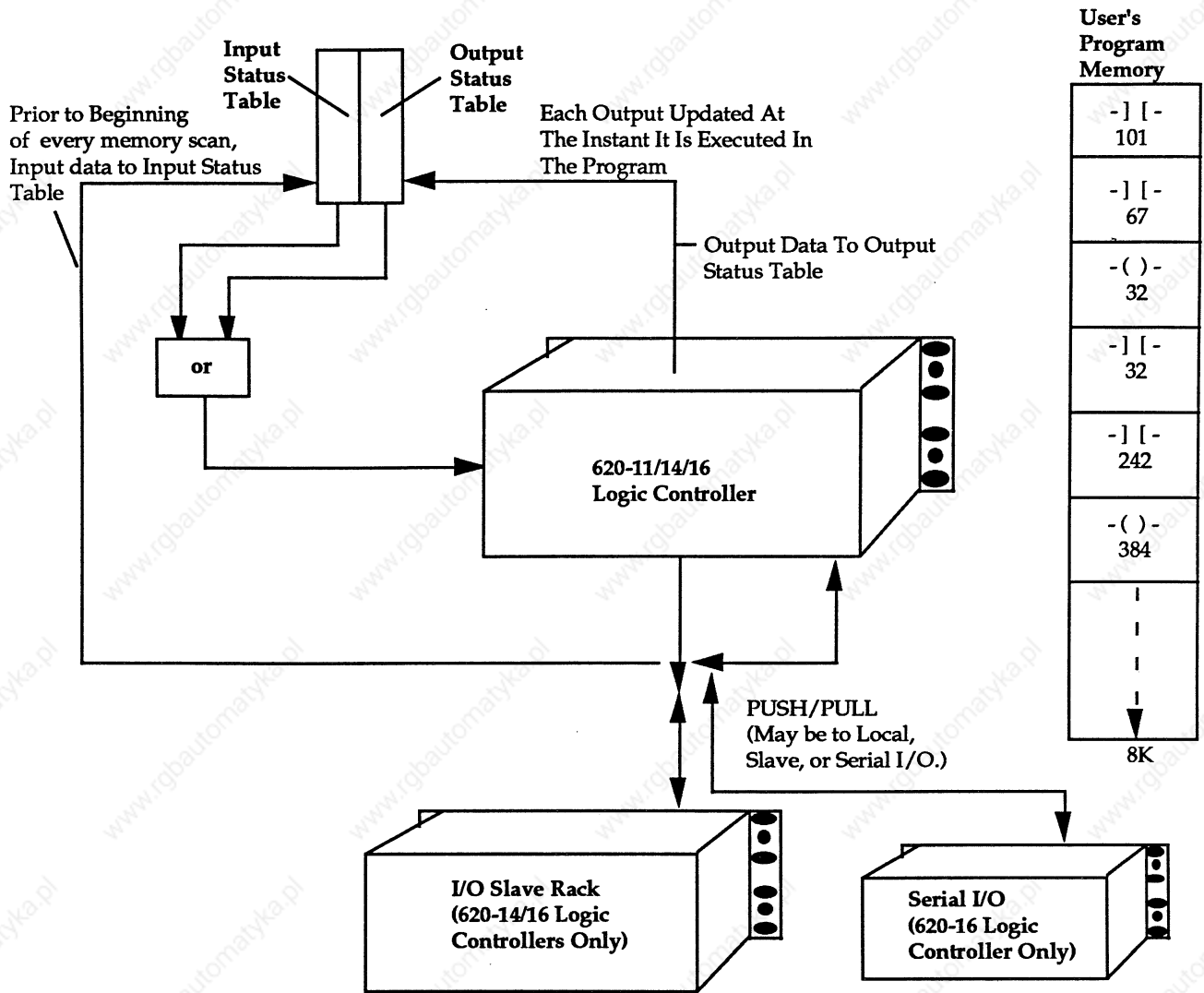
FIGURE 13 - 620-11/14/16 CONTROL PROCESSOR MODULE PROGRAM EXECUTION

RUN MODE PROGRAMMING

The 620-11/14/16 Control Processor Modules have the capability to make program changes while in the RUN mode.

Selecting F1 enables this function on the Processor Configuration Menu screen and allows users to make control program additions and deletions while in the RUN mode with no adverse effect on system operation, other than temporarily increasing scan time (20ms maximum).

The 623-60 MS-DOS Loader or 623-6100/6150 Loader/Terminal with software revision 3.0 or higher must be used to perform RUN Mode Programming.

RUN MODE PROGRAMMING CHANGES

RUN mode programming is possible only when the Loader/Terminal is in the PROGRAM mode, the processor keyswitch is in the RUN/PROGRAM position, and RUN mode programming has been enabled by selecting F1 of the Processor Configuration menu.

When the Loader/Terminal is placed in the PROGRAM mode by pressing F11 (or SHIFT and F1 simultaneously), the following message is displayed:

```
CAUTION
620 in RUN mode-RUN MODE PGM ENABLED
Output bit(s) will remain in last state
if DELETED or ADDRESS CHANGED
```

Editing A Line - An existing program line can be edited. When the changes are complete, press INSERT and ENTER. This message appears:

```
WARNING!
RUN mode programming enabled! ENTER to
Execute; Any key to cancel<<<
```

An additional message is displayed during a delete or line enter function:

```
WARNING!
Loader is not monitoring line status!
```

Press ENTER to complete the process. A "busy" message flashes when the line edit function is being executed. When this message disappears, line monitoring resumes.

INSERTING AND LOADING A LINE - A new logic line can be inserted between existing lines (INSERT, Pg Dn) or at the end of the program (ENTER). These operations are similar to the edit line process. The actual operation is started by pressing ENTER.

DELETING A LINE - The currently displayed line can be deleted from the program by pressing DEL, Pg Dn. Caution and warning messages are displayed. If the line terminator is a coil, make sure it is OFF prior to the delete operation. A Send Out, likewise, should be set to zero. The delete is started by pressing ENTER.

SEQUENCERS - Sequencers of 80 steps or fewer can be inserted, loaded, or deleted using normal RUN mode methods. To delete sequencers with more than 80 steps individual steps must be deleted until 80 steps or fewer are left. At that point, the entire sequencer can be deleted. Do not use multiple step editing on sequencers with more than 80 steps.

ON-LINE PROGRAMMING RULES

When making RUN mode changes, follow these precautions:

1. Remember that scan times may increase by as much as 20ms.

2. Use care when performing on-line programming operations with subroutines and certain types of NSKR instructions:

   • When adding new subroutines, add the SUB instruction first, then the JSR. Likewise, when adding new jumps, add the EOS first, then the NSKR.

   • When deleting subroutines, delete the JSR first, then the SUB. When deleting jumps, delete the NSKR first, then the EOS.

   • Do not overwrite a SUB or EOS with another SUB or EOS. The old instructions should be deleted before the new instruction is added.

   • Adjust the step number register with the new number of steps. For example, adding a step before the active step makes the sequencer appear to be moving back a step. Deleting a step before the active step makes the sequencer appear to be moving forward a step.

   • Remember the target sequencer may be deleted if Load or Unload Sequencer instructions are used. In this case, the Load/Unload instruction would operate on the next sequencer in the program.

3. If a power loss occurs during a RUN mode programming operation, it could cause a "write in progress" failure. This causes the Control Processor Module to shut down. The only way to recovery is to reload memory.

4. When inserting or adding a new section of program:

   • Insert an EOS with an unused reference number such as 999.

   • Ahead of the EOS 999, insert a false NSKR line (example below):

```
                        never true or forced OFF
                    /
            990 /
            +-]/[-+---+---+---+---+---+---+---+-NSKR
                                              999
```
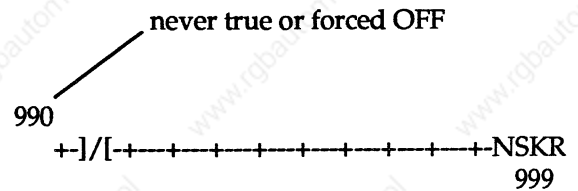
   • Insert new program lines between the NSKR and EOS lines.

   • Review the new program lines for errors.

   • Delete the NSKR line.

   • Delete the EOS line.

CONTROL PROCESSOR MODULE (CPM) DIAGNOSTICS

The 620-11/14/16 Control Processor Module self-diagnostics enable the user to locate system faults at the module level. These troubleshooting aids are designed to reduce service time and increase uptime.

LED indicators signify the occurrence of system faults and direct the user to fault locations. The series of self-diagnostic tests begin with the CPM, and proceed through the processor backplane and other modules within the processor rack. The four diagnostic categories include:

- Power-up Self-Test
- Program Memory Check
- On-Line Checks
- Loader/Terminal Diagnostics

POWER-UP SELF-TEST

The CPM begins the self-diagnostic test program stored in the executive ROM. Power-up steps include:

1. Testing data flow through the microprocessor and operation of the microprocessor registers.

2. Verifying checksum of executive ROMs.

3. Verifying configuration and exercise control outputs of the Logic Cell Array (LCA).

4. Testing User Data Stack overflow detection and recovery mechanism.

5. Performing serial asynchronous communication device internal loopback test.

6. Performing serial asynchronous communication device/microprocessor crystal tolerance test.

7. Performing 10ms time base interrupt logic test.

8. Testing single-bit I/O Read circuitry used in solving ladder logic.

9. Testing option card bus interface.

10. Performing System RAM Read/Write test (non-destructive).

11. Performing Input Status Table RAM Read/Write test.

12. Performing Output Status Table RAM Read/Write test (non-destructive).

13. Performing Card Select RAM Read/Write test.

PROGRAM MEMORY CHECK

The user program memory is checked through a comparison of checksum calculations. If any on-line changes are made, the initial checksum is recalculated. The checksum calculation and comparison check follows:

1. The CPM calculates the initial checksum of the user program during the retentive scan.

2. The CPM calculates the checksum of the user program while the program is running. To do this it reads 12 memory words per scan. If any on-line changes are made, the CPM starts over by recalculating the initial checksum.

3. If the two checksum calculations match, no error has been detected.

4. If the two checksum calculations do not match, the CPM sets the error flag (see Table 5) and assumes the PROGRAM mode. The Loader/Terminal will display a LCS Diagnostics Fail message. The Loader/Terminal will display "program checksum error" when the processor is placed in PROGRAM mode. Recovery from a checksum requires reloading program memory.

Table 5 describes the function of System Status Table registers involved in the checksum calculation and comparison procedure.

TABLE 5 - CHECKSUM REGISTER

REGISTER	CONTENT	FUNCTION
2395 2394	Checksum	These registers store the calculated user program memory checksum.
2393 2392	Checksum Error Flag	The most significant bit (MSB) is 0 when no error is detected. The MSB is 1 when an error is detected.
2391	Initial Flag	System Use Only.
2390	Initial Pass	Returns 0 when the initial checksum is being calculated and 1 when the initial checksum is completed.

ON-LINE CHECKS

On-line Checks are functional tests performed at the beginning of every scan, before inputs are updated. The functional tests do the following:

1. Perform a running logic cell arrray configuration test (complete test takes approximately 1000 scans).

2. Perform a running card select RAM checksum test (16 scans).

3. Test single-bit I/O Read circuitry used in solving ladder logic.

4. Test for an Input Status Scan instruction in the first user memory location.

5. Test for End of Memory Instructions in proper places in the user program.

6. Reset scan loss timer (Scan loss time delay: 150ms minimum, 200ms maximum).

If any of these steps fail, the CPM immediately goes into the complete self-test. The output modules also check for proper data flow during the program scan.

MONITORING DIAGNOSTICS

The 623-6100/6150 Loader/Terminal or 623-60 MS-DOS Loader (with Software Revision 3.0 or greater) allows you to examine the results of 620-11/14/16 diagnostics. LCS hardware and software status may be accessed and monitored using the Loader/Terminal CRT.

The HARDWARE STATUS display provides data about Control Processor Module revision and test status, program scan time, and the status of software-configurable selection options.

The SELF-TEST display indicates the pass/fail status of the individual hardware elements involved in the self-test routine. Sometimes the Control Processor Module has passed in the SELF-TEST and LCS DIAGNOSTIC FAIL appears in the Loader/Terminal edit line; this indicates a software error. To correct this error, clear the program memory and reload the program.

The I/O MODULE STATUS display lists the total I/O module faults at any given time and the most significant addresses associated with each of the first eight faulted modules detected.

REMOTE SERIAL I/O OPERATION

GENERAL OPERATION

Serial I/O is only supported by the 620-16 Logic Controller. The 620-16 permits serial I/O operation through the installation of a 621-9939 Serial Link Module (SLM) in slot H of the processor rack (see Figures 3 and 4).

WARNING
A revision has been made to the 621-9939 SLM to make it compatible with the 620-16 Control Processor Module. Do not install a 621-9939 SLM into a 620-16 Processor Rack unless the SLM has a printed circuit board label with Assembly Level C030012132G or greater.

621-9939 SLMs manufactured before January 10, 1989 need to be made compatible with the 620-16 CPM. Order Upgrade Kit No. 221-0012 and install it before applying power to the unit. Improper I/O system operation could result if this procedure is not followed.

SERIAL I/O SPECIFICATIONS

DATA TRANSFER MEDIUM........... Serial 4-wire full duplex (asynchronous to processor scan)

DATA RATE..115.2K baud

ELECTRICAL FORMAT...RS422

SERIAL CHANNEL SCAN RATE......Depends on the number of racks per link, number of discrete points per link, number of racks containing PUSH/PULL cards, and the number of PUSH/PULL cards updated in each rack per scan (all or 1 per scan).

MAXIMUM DROPS
PER CHANNEL...16

MAXIMUM I/O
PER CHANNEL..2040

MAXIMUM CHANNEL
LENGTH.......................4000ft. (Belden 9729, using 200 ohm terminating resistor)

10,000ft. (Belden 9182, using 300 ohm terminating resistor)

ERROR CHECKING..........Cyclical redundancy check plus data receive time out.

SERIAL I/O INSTALLATION

Serial I/O allows I/O racks to be mounted close to the machine or process being controlled instead of at the Logic Controller. This eliminates the high cost of installing long wire runs. The 620-16 Processor Rack provides one slot — H only — for a Serial Link Module (SLM). Two channels are available on the SLM.

Serial I/O Modules (SIOM's), which are installed in each I/O rack, connect to the serial channel in a multi-drop arrangement. This allows an I/O rack to be disconnected while communication to the other remote I/O racks on the link is maintained.

Refer to the 620 Installation Manual (Form No. 620-8996) for Serial Link Module (621-9939) and Serial I/O Module (621-9940) operational and address DIP switch settings.

Be careful when selecting the CLEAR/FREEZE operational setting for an I/O rack on the SIOM, some Logic Controller I/O operational settings are not compatible with SIOM settings. Table 6 describes the operational function of an I/O rack based on CPM and SIOM settings.

TABLE 6 - I/O CLEAR/FREEZE SETTINGS

CPM* I/O SETTING	SIOM SETTING	FUNCTION IN SERIAL I/O RACK
Clear	Clear	Clear
Clear	Freeze	Freeze
Freeze	Clear	Freeze
Freeze	Freeze	Freeze

*CPM = Control Processor Module

NOTE
Card (module) faults detected in a remote serial I/O rack will cause the SIOM to function according to its DIP switch settings and are not affected by the Logic Controller I/O setting.

SERIAL ADDRESSING

SERIAL ADDRESSING

Any mix of 0-, 8-, 16- and 32-point I/O modules may be used in a serial I/O rack. Address by setting DIP switches on the SIOM. Setting an 8-position DIP switch establishes the starting address for each rack. Also, a pair of switches identifies each I/O slot within a rack for 0, 8, 16 or 32 points. Rack addresses are set in multiples of 8 by setting the appropriate DIP switches to the CLOSED/ON position and adding their values.

For example, in Figure 14, the starting address of the first serial I/O rack (rack 2) is 192. Switches 4 and 5 (64 + 128 = 192) are set CLOSED/ON to assign a starting address of 192. Since rack 2 has 384 I/O points, the starting address of rack 3 is 576 (192 + 384 = 576). Switches 4 and 7 (64 + 512 = 576) are CLOSED/ON to asssign a starting address of 576. Serial racks may not share the same starting address or have overlapping addresses.

Figure 4 shows the serial racks with consecutive adresses; however, this is not necessary. Real I/O addresses may be skipped between racks or the first rack on the link may have a higher starting address than the second rack, provided addresses do not overlap. Because of this feature, serial racks may be laid out to accommodate future expansion or the physical layout of the plant.

DIP switches SW3, SW4 and SW5 are set to designate the number of I/O points per slot. Each pair of switches from these banks designates the number of I/O points for an individual slot. Starting with slot A and assuming a 16-point I/O module, switch 7 of SW5 is OPEN/OFF and switch 8 of SW5 is CLOSED/ON to identify a 16-point module in slot A. This same procedure is used to set the remaining I/O slots for the corresponding point configuration. The most points per rack is 384 (32 pts. x 12 slots).

NOTE
The combination of the starting address and the total assigned I/O count in a rack may not exceed 2039 in Version 2.0 or higher. If that sum does exceed 2039, the rack will not come on line.

Serial I/O Channel No. 1

Rack No. 1
620-16 Processor Rack (No I/O modules) | S L M | | 620-16 Control Processor Module

Rack No. 2
12, 32-pt. Modules
Starting Addr. 192
Total Points 384 | S I O M

Rack No. 3
8, 16-pt. Modules
4, 32-pt. Modules
Starting Addr. 576
Total Points 256 | S I O M

Serial I/O Channel No. 2

"Slave" I/O Rack (No. 1)
8, 8-pt. Modules
4, 32-pt. Modules
Starting Addr. 0
Total Points 192

Slave I/O Extender Module 621-9000

Rack No. 4
6, 8-pt. Modules
6, 16-pt. Modules
Starting Addr. 832
Total Points 144 | S I O M

Rack No. 5
7, 8-pt. Modules
5, 32-pt. Modules
Starting Addr. 976
Total Points 216 | S I O M

Rack No. 6
6, 16- pt. Modules
Starting Addr. 1192
Total Points 96 | S I O M

RACK	I/O MODULES		I/O PTS. PER RACK	STARTING ADDRESS	ENDING ADDRESS
	NO.	PTS.			
1	8	8	192	0	191
	4	32			
2	12	32	384	192	575
3	8	16	256	576	831
	4	32			
4	6	8	144	832	975
	6	16			
5	7	8	216	976	1191
	5	32			
6	6	16	96	1192	1287

Note: This example Processor Rack does not have any I/O modules installed.

FIGURE 14 - EXAMPLE OF LOCAL/SLAVE AND SERIAL I/O ADDRESSING CONFIGURATION

CONTROL NETWORK CONFIGURATION

A Control Network is a high speed peer-to-peer communication system. As many as eight Logic Controllers can share I/O status over a serial channel. Installing the Control Network Module in a 620-11/14/16 option slot enables the Logic Controller to communicate with as many as seven other controllers that are connected by a multi-drop, single twisted pair half-duplex link. Each CNM on the network can transmit either 32 or 64 discrete I/O points or two or four 16-bit registers onto the network.

All Logic Controllers on the Control Network operate asynchronously. The network is fast enough to provide real-time control. The trunk line can extend a maximum of 8000 feet. The transmission distance can be extended with the use of modems.

Two types of Control Network configurations are possible. Typically, each controller on the network will contain only one CNM. It is optional though to install a maximum of two CNM's in the 620-11/14/16, enabling it to pass information from one network to another or to collect information from different networks. In such applications each CNM has a unique module number and a unique transfer table. Figure 15 illustrates a Control Network configuration.
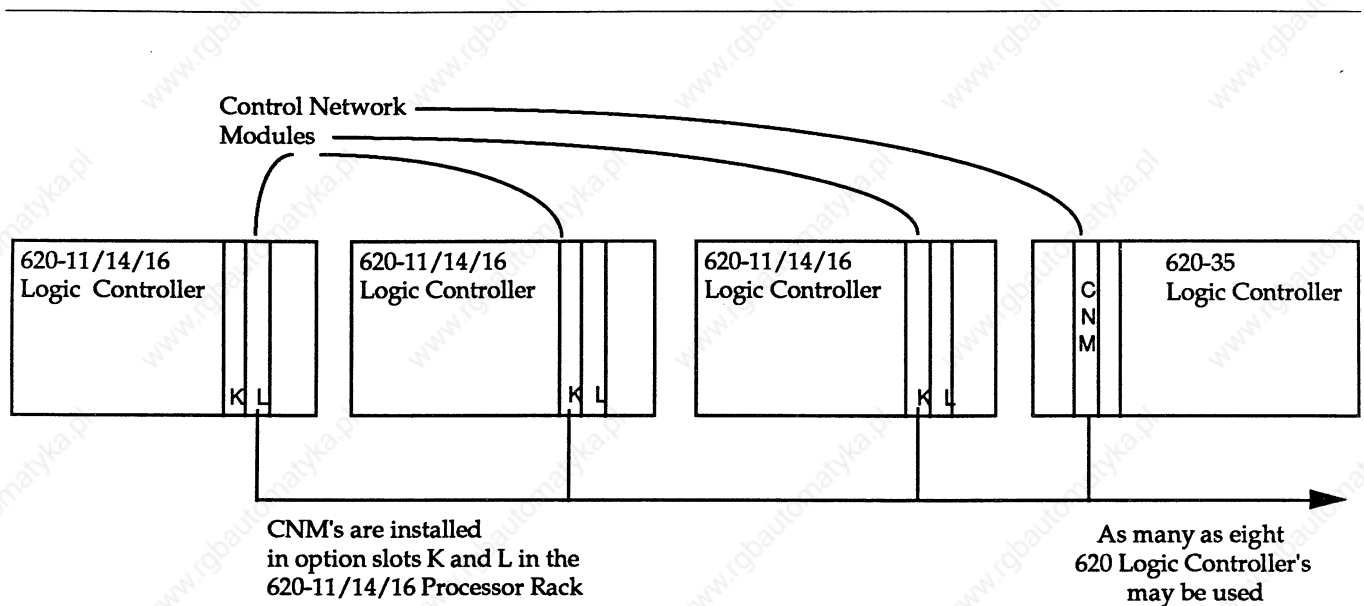
FIGURE 15 - EXAMPLE OF CONTROL NETWORK CONFIGURATION

SYSTEM CONFIGURATION

The 620-11/14/16 Logic Controller, I/O, and communication port are configured through the 623-60 Loader/Terminal software, the communication port, or 620-0048/0052 Data Collection Modules (DCMs).

This section addresses Logic Controller and I/O configuration through software on the 623-60 MS-DOS Loader/Terminal. Software configuration of the on-board Communication Port is discussed in detail in the Communication Port section of this manual.

NOTE
The Control Processor Module is inhibited from entering RUN mode until a valid I/O configuration is installed.

Configuration procedures through the communication port and 620-0048/0052 DCMs are discussed in Appendix II of this manual.

For detailed information on installing and preparing the system for configuration, refer to the 620 Installation User Manual (Form No. 620-8996), the 620 Configuration Guide (Form No. 6654-PR1) and the 621 I/O Specifications User Manual (Form No. 620-8995).

For information on the Loader/Terminal connection within a 620 Logic Controller System, refer to the 623 MS-DOS Loader User Manual (Form No. 623-8993), the 623-6100/6150 Loader/Terminal User Manual (Form No. 623-8940), or the 623-6000 User Manual (Form No. 623-8987).

PROCESSOR CONFIGURATION

The Processor Configuration Menu from the Selection Menu is found under the Selection Menu on the 623-60 MS-DOS Loader/Terminal. By pressing selection F5 you can enter the Processor Configuration Menu and edit the processor configuration.

The Loader/Terminal reads the current settings and displays them in the Processor Configuration Menu. Figure 16 shows a configuration screen diagram.

The Processor Configuration Menu makes the following selections available. The default settings are:

F1   ENABLE/DISABLE the AUGMENTED RUN mode programming.

F2   ENABLE/DISABLE force function.

F3   ENABLE/DISABLE scan with low battery.

NOTE
Scan will be prevented only after the control processor keyswitch mode is changed to RUN or upon power-up.

F4   ENABLE/DISABLE data change.

F5   ENABLE/DISABLE scan watchdog timer.

F6   CLEAR/FREEZE processor rack and slave rack (local) outputs upon transition to SOFTWARE PROGRAM, PROGRAM or DISABLE mode and upon scan loss.

Under power fail conditions, the local I/O always will clear regardless of the FREEZE/CLEAR setting. Additionally, if an SLM is present and set to signal I/O power fail, then a power fail condition will cause both local and remote I/O outputs to clear.

F7   ENABLE/DISABLE serial port (communication port) to make the on-board communication interface active or inactive.

F8   Enter the Communication Port Configuration menu (for communication port configuration details, see the Communication Port section of this manual.

F9   Loads a processor configuration previously saved to the Processor Configuration Menu.

F10   Saves the processor configuration on a disk file.

ENTER   Installs the configuration data on the menu to the Control Processor Module.

```
┌─ 620 Selection Menu ──────────────────────────────────────────────┐
│                                                                     │
│  ┌────┐  ┌──────────────────────────┐  ┌────┐  ┌──────────────────┐ │
│  │ F1 │  │ Model Number: 620-16     │  │ F2 │  │ Memory Size: 8192│ │
│  └────┘  └──────────────────────────┘  └────┘  └──────────────────┘ │
│                                                                     │
│  ┌────┐  ┌──────────────────────────┐  ┌────┐  ┌──────────────────┐ │
│  │ F3 │  │ Register Size: 4096      │  │ F4 │  │ Real I/O size:2048│ │
│  └────┘  └──────────────────────────┘  └────┘  └──────────────────┘ │
│                                                                     │
│  ┌────┐  ┌──────────────────────────┐  ┌────┐  ┌──────────────────┐ │
│  │ F5 │  │ Edit Processor Configura.│  │ F6 │  │ Edit I/O Config. │ │
│  └────┘  └──────────────────────────┘  └────┘  └──────────────────┘ │
│                                                                     │
│  ┌────┐  ┌──────────────────────────┐  ┌────┐  ┌──────────────────┐ │
│  │ F7 │  │ Verify Processor Config. │  │ F8 │  │ Verify I/O Config.│ │
│  └────┘  └──────────────────────────┘  └────┘  └──────────────────┘ │
│                                                                     │
│  ┌────┐  ┌──────────────────────────┐  ┌────┐  ┌──────────────────┐ │
│  │ F9 │  │                          │  │F10 │  │                  │ │
│  └────┘  └──────────────────────────┘  └────┘  └──────────────────┘ │
│                                        Press [Enter] to continue     │
└─────────────────────────────────────────────────────────────────────┘
```

Press F5 to enter Processor Configuration Menu

```
┌─ Processor Configuration Menu ───────────────────────────────────────┐
│                                                                       │
│ ┌────┐ ┌───────────────────────────┐ ┌────┐ ┌──────────────────────┐ │
│ │ F1 │ │Run Mode Programming:DISABLE│ │ F2 │ │Force Functions:DISABLE│ │
│ └────┘ └───────────────────────────┘ └────┘ └──────────────────────┘ │
│                                                                       │
│ ┌────┐ ┌───────────────────────────┐ ┌────┐ ┌──────────────────────┐ │
│ │ F3 │ │Scan with Low Battery:DISABLE││ F4 │ │Data Change Function:DISABLE│
│ └────┘ └───────────────────────────┘ └────┘ └──────────────────────┘ │
│                                                                       │
│ ┌────┐ ┌───────────────────────────┐ ┌────┐ ┌──────────────────────┐ │
│ │ F5 │ │Scan Watchdog Timer:ENABLE │ │ F6 │ │On Mode Change I/O will:CLEAR│
│ └────┘ └───────────────────────────┘ └────┘ └──────────────────────┘ │
│                                                                       │
│ ┌────┐ ┌───────────────────────────┐ ┌────┐ ┌──────────────────────┐ │
│ │ F7 │ │Serial Port: DISABLE       │ │ F8 │ │Serial Port Configuration│
│ └────┘ └───────────────────────────┘ └────┘ └──────────────────────┘ │
│                                                                       │
│ ┌────┐ ┌───────────────────────────┐ ┌────┐ ┌──────────────────────┐ │
│ │ F9 │ │Load Processor Configuration│ │F10 │ │Save Processor Configuration│
│ └────┘ └───────────────────────────┘ └────┘ └──────────────────────┘ │
│  Press [Enter] To Keep Changes                    [Esc] to Exit       │
└───────────────────────────────────────────────────────────────────────┘
```

SELECTIONS

F1 - ENABLE, *DISABLE   F6 - *CLEAR, FREEZE
F2 - ENABLE, *DISABLE   F7 - ENABLE, *DISABLE
F3 - ENABLE, *DISABLE   F8 - Enter Communication Port Configuration Menu
F4 - ENABLE, *DISABLE   F9 - Loads configuration from file to menu
F5 - *ENABLE, DISABLE   F10 - Saves configuration to disk; names the file
                                    ENTER - Installs the configuration selections to processor

* Denotes default settings
   on initial power-up.

FIGURE 16 - 620-11/14/16 PROCESSOR CONFIGURATION SELECTIONS

I/O CONFIGURATION

The user may select the I/O Configuration Menu from the 620 Selection Menu on the 623-60 MS-DOS Loader/Terminal. The user can edit the I/O Configuration Menu by pressing selection F6 to enter the I/O configuration.

The processor rack and slave rack I/O slots must be configured to the number of points assigned to each slot according to the following selections:

F1	=	0 points	**F2** =	8
F3	=	16	**F4** =	32
F5	=	SLM (Processor Rack slot H only)		

All I/O slots on the processor rack or slave rack will accommodate 0, 8-, 16- and 32-point I/O modules. All I/O module slots are default set for 0 on initial power-up.

F9 Loads the I/O configuration data from disk file to the I/O Configuration Menu.

F10 Saves the configuration to disk file.

ENTER Installs the I/O configuration from the menu to the CPM.

Figure 17 shows a sample 620-11/14/16 I/O Configuration Menu.

---

620 Selection Menu

F1	Model Number: 620-16	F2	Memory Size: 8192
F3	Register Size: 4096	F4	Real I/O size: 2048
F5	Edit Processor Configuration	**F6**	Edit I/O Configuration
F7	Verify Processor Configuration	F8	Verify I/O Configuration
F9		F10	

Press [Enter] to continue

Press F6 for I/O Configuration Menu

Local I/O Slot Configuration

	Slot	Points	Slot	Points
Processor	A	8	C	16
	B	8	D	16
	C	8	E	32
	D	8	F	32
	E	8	G	32
	F	8	H	32
	G	8	I	32
	H	SLM	J	32
Slave	A	16	K	32
	B	16	L	32

F1 - 0   F2 - 8   F3 - 16   F4 - 32   F5 SLM   F9 LOAD   F10 SAVE

Press [ENTER] To Install Configuration

FIGURE 17 - EXAMPLE 620-11/14/16 I/O CONFIGURATION SELECTIONS

I/O SLOT ASSIGNMENT FOR CONFIGURATION

Slots A-H and A-L in the I/O Configuration Menu correspond with slots in the processor rack and slave I/O rack. Figure 18 show diagrams that specify the number of points for each I/O module when configuring through the I/O Configuration Menu. Descriptions follow below.

I/O slots in any 620-11/14/16 configuration must be defined on the I/O Configuration Menu. Each slot on the menu must be assigned a value (0, 8, 16, 32 or SLM) regardless of whether all slots exist or whether all slots are being used in a particular configuration.

Processor Full Rack Assignments

In the 620-1690 Standard and 620-1693 Augmented Processor Rack for the 620-11/14/16, I/O module slots A-H correspond directly with slots A-H in the I/O Configuration Menu. Note that slots I-J are designated for the power supply, K-L for option modules, and M-N for the Control Processor Module and these slots are not defined in the I/O Configuration Menu. (See Figure 18.) Slot H can be designated for an I/O module or for the SLM in the 620-16 configuration.

Processor Half Rack Assignments

In the 620-1692 Processor Half Rack and the 620-1695 Augmented Processor Half Rack, I/O module slots A-D correspond directly with slots A-D in the I/O Configuration Menu. (See Figure 18.) Menu slots E-H, corresponding with I/O slots E-H, must be configured for 0 points (the default setting).

I/O Full Rack Assignments

In a 621-9990 Standard I/O Slave Rack or 621-9992 Augmented I/O Slave Rack, I/O module slots A-L correspond directly with slots A-L in the I/O Configuration Menu. Slot M is designated for the 621-9001 Power Supply Extender Module or an independent power supply module. Slot N is designated for the 621-9000 I/O Extender Module. (See Figure 19.)

I/O Half Rack Assignments

In a 621-9991 Half Rack, I/O module slots A-F correspond directly with slots A-F in the I/O Configuration Menu. Slot G is designated for the 621-9000 Power Supply Extender Module or an independent power supply module. Slot H is designated to the 621-9000 I/O Extender (see Figure 19).

Serial I/O Assignments

The 620-16 supports Serial I/O by designating Slot H for the Serial Link Module in the I/O Configuration Menu. Serial I/O slot types and starting addresses are configured by DIP switches on the Serial I/O Modules (SIOM's).

> **NOTE**
> SLM addresses must start at some address greater than the highest address used in the last processor rack or slave rack slot assigned. For instance, if the highest address in slot L is 191, the SLM addresses must start at 192 or higher (see Figure 14).

19-inch Processor Full Rack
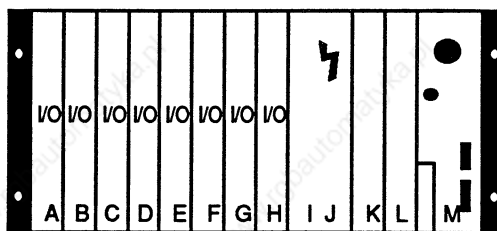
Slot Assignment On I/O Configuration Menu

A = I/O   H = I/O or SLM
B = I/O   I-J = Power Supply
C = I/O   K = Option Module
D = I/O   L = Option Module
E = I/O   M-N = Processor Module
F = I/O
G = I/O

11-inch Processor Half Rack
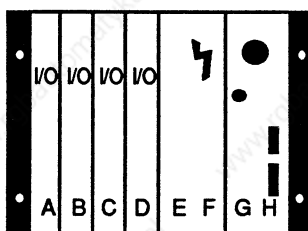
Slot Assignment On I/O Configuration Menu

A = I/O
B = I/O
C = I/O
D = I/O
E-F = Power Supply
G-H = Processor

Default settings = 0 points
Unused slots = 0 points

FIGURE 18 - I/O SLOT ASSIGNMENTS FOR PROCESSOR RACKS

19-inch Slave I/O Full Rack

Slot Assignment On I/O Configuration Menu

A = I/O	H = I/O
B = I/O	I = I/O
C = I/O	J = I/O
D = I/O	K = I/O
E = I/O	L = I/O
F = I/O	M = Power Supply or PS Extender
G = I/O	N = I/O Extender

11-inch Slave I/O Half Rack
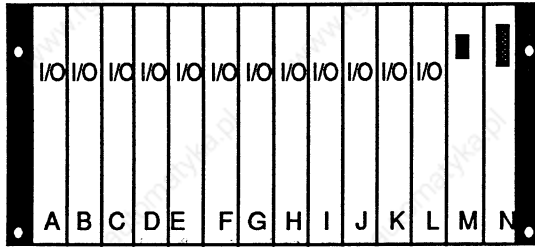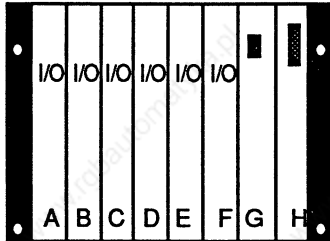
Slot Assignment On I/O Configuration Menu

A = I/O
B = I/O
C = I/O
D = I/O
E = I/O
F = I/O
G = Power Supply or PS Extender
H = I/O Extender

Default settings = 0 points
Unused slots = 0 points

FIGURE 19 - I/O SLOT ASSIGNMENTS FOR SLAVE I/O RACKS

= Unused or empty slot
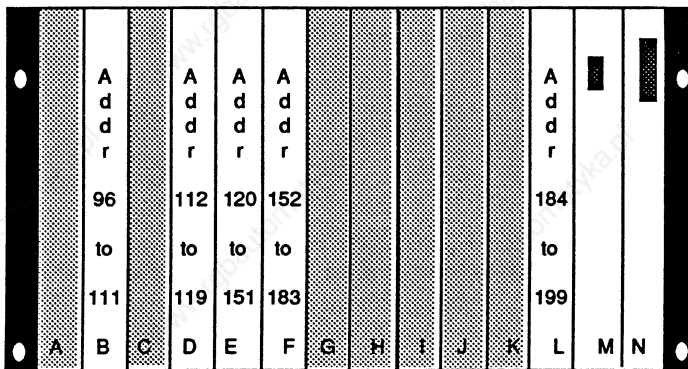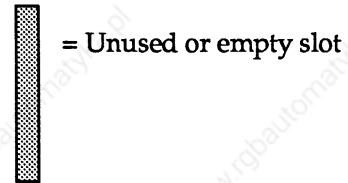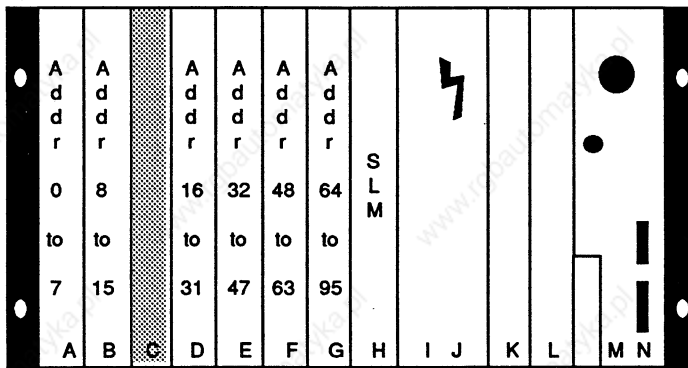
Local I/O Slot Configuration Menu

	Slot	Points	Slot	Points
PROCESSOR	A	8	C	0
	B	8	D	8
	C	0	E	32
	D	16	F	32
	E	16	G	0
	F	16	H	0
	G	32	I	0
	H	SLM	J	0
SLAVE	A	0	K	0
	B	16	L	16

FIGURE 20 - EXAMPLE OF SEQUENTIAL I/O ADDRESSING IN PROCESSOR AND SLAVE RACKS

COMMUNICATION PORT

The 620-11/14/16 Control Processor Modules (CPMs) feature a 25-pin communication port for serial communication with host computers. The port supports current Honeywell Asynchronous Byte Count (ABC) protocol, MODBUS Remote Terminal Unit (RTU) protocol, and the RS422/485 specification.

NOTE
The communication port does not support RS232 communication.

The communication port provides the on-board functions of the 620-0043 Communication Interface Module or the 620-0048 Data Collection Module (with some limitations). The port allows the 620-11/14/16 Logic Controller System to accept commands, carry out data exchanges, and return responses to the host computer.

The communication port is serviced directly by the 620-11/14/16 CPM. The CPM treats the port as an additional option card in the processor rack by giving it a "window" at the end of each processor scan in which to access the processor data base. This "window" occurs during Memory Word Zero (MWZ). However, any transmit or receive activity through this port will generate an interrupt that temporarily halts ladder logic processing and will slightly increase processor scan time.

The average time required by the 620-11/14/16 processor to service a communication port interrupt is 60 µsec per character for the Honeywell ABC protocol and 92 µsec per character for the MODBUS RTU protocol.

A worst-case situation, where the port is configured for 19.2K baud and is continuously interrupted, will cause the program scan to increase by 12 percent for Honeywell ABC protocol and 18 percent for MODBUS RTU protocol. The sections of this manual devoted specifically to the individual ABC and RTU protocols define the impact of the MWZ windows.

SPECIFICATIONS

RS422/RS485 ELECTRICAL SPECIFICATIONS

All signals adhere to EIA RS422/RS485 Standard specifications, in addition to the following specifications:

- Common mode output voltage line drivers: -7V, +12V
- Tristate control through RS or SD line drivers for half duplex/multidrop applications.
- Thermal shutdown protection on line drivers
- Positive and negative current limiting on line drivers
- Input impedance of line receivers: 12K ohm minimum
- 120-ohm line termination on RD, CS receivers (RD selectable)

CABLE RECOMMENDATIONS

When selecting data communication cable, observe the following guidelines:

- High-quality twisted pair cables should be used. (Recommended cables are listed in Table 7.)
- Individual shielding of each pair is preferred.
- Characteristic cable impedance should be set. ($100 \leq Z \leq 150$ ohms)
- Construction should meet local building codes.

TABLE 7 - CABLE RECOMMENDATIONS

CABLE	BELDEN	ALPHA
Single Twisted Pair	9182	9823
Two Twisted Pair	9729	——
Three Twisted Pair	9730	6073

CALCULATING NETWORK TRUNK LENGTH

The length of any network trunk is limited by cable characteristics. Use the following equations to calculate network trunk length for a specific cable.

Maximum Trunk Length (ft). =
(Z/2R) x 1000

Z = Cable characteristic impedance (ohms)
R = Cable conductor resistance per 1000 feet (ohms)

Example: Belden 9182 cable
Z = 150 ohms
R = 14 ohms

Maximum Trunk Length (ft.) =
(150 ohms/28 ohms) x 1000 = 5357 ft.

Example: Belden 9729
Z = 100 ohms
R = 24 ohms

Maximum Trunk Length (ft.) =
(100 ohms/48 ohms) x 1000 = 2083 ft.

CONNECTOR

The port is a 25-pin D series subminiature receptacle connector. It is an AMP HDP-20 series metal shell connector and equipped with an AMP 206512-1 locking post assembly.

PIN ASSIGNMENTS AND REFERENCE DESIGNATORS

Table 8 lists pin assignments and reference designators.

RS422/RS485 SIGNAL FUNCTIONAL DESCRIPTIONS

In the following descriptions, Data Terminal Equipment (DTE) refers to the 620-11/14/16 Communication Port or host, and Data Communication Equipment (DCE) refers to a modem.

SHIELD GROUND

The shield ground input provides a direct connection to chassis ground. The cable shield may be terminated at only one end in some applications.

TABLE 8 - PIN ASSIGNMENTS AND REFERENCE DESIGNATORS

PIN NUMBER	SIGNAL I/O DESCRIPTION	CONNECTOR DESIGNATOR
1	Shield	---
7	Signal Ground	---
12	Request to Send (Output)	RS-A
13	Request to Send, Inv.	RS-B
14	Transmit Data, Inv. (Output)	SD-B
15	Transmit Data	SD-A
16	Clear to Send, Inv. (Input)	CS-B'
17	Clear to Send	CS-A'
21	Receive Data, Inv. (Input)	RD-B'
22	Receive Data	RD-A'

TRANSMIT DATA (TD)

Signals on this circuit are generated by the 620-11/14/16 Communication Port. These signals transmit data to an attached DCE (into Transmit Data) or to an attached DTE (into Receive Data). The communication port holds Transmit Data in a marking condition during intervals between characters or words, and at all times when no data is being transmitted. The communication port transmits data only when an ON condition is present in the following two circuits:

- Request to Send
- Clear to Send

RECEIVE DATA (RD)

Signals on the Receive Data Circuit are generated in response to data signals generated by the attached DCE through Receive Data, or by the attached DTE through Transmit Data.

The Receive Data function is disabled when the Request to Send output is in the ON condition in a half duplex mode. This disabling function is implemented through executive firmware in the 620-11/14/16 Communication Port.

REQUEST TO SEND (RS)

This circuit conditions the attached DCE for the transmit mode of the DTE. In the full duplex mode, Request to Send has no internal control of the DTE transmitter or receiver. In the half duplex/multidrop mode, Request to Send has the following internal control functions:

- When Request to Send is ON, the receive mode is disabled.
- Request to Send (OFF state) switches the Transmit Data line driver and the RS driver into the tri-state mode.

NOTE
The host computer must be prepared to handle the following possibilities: the port transmit drivers becoming tri-stated and the host's RS422/485 differential line receiver inputs left floating. Spurious receiver interrupts may occur at the host. These interrupts must be filtered out or suppressed by the host's interface hardware or software.

(Consult Multidropping Figures in the MiniCOP/COP User Manual Form No. 627-8991 for more information.)

The Request to Send function is not used between DTE's attached directly to one another. In this configuration, jumper the Request to Send output to its Clear to Send input on the local connecter of each DTE.

CLEAR TO SEND (CS)

When the communication port is attached to a DCE, the Clear to Send Signal is generated by the DCE in response to the port's Request to Send input. The signal indicates if the DCE is ready to transmit. The communication port will not enter the transmit mode when Clear to Send is in the OFF condition.

The Clear to Send signal is not used between DTE's attached to one another. In this configuration, jumper the Clear to Send input to the Request to Send output at each communication port's local attached connector. Note that jumpering this input to a fixed voltage also provides the ON condition. However, the definition of the RS/CS interchange requires the CS to turn OFF before the RS is asserted. Connecting the CS to a fixed level does not satisfy this requirement.

The DCE has the following control functions.

1. A transition of the communication port's RS signal from OFF to ON instructs the DCE to enter the transmit mode. After the DCE enters the transmit mode, it turns ON its Clear to Send Circuit. The port will not enter the transmit mode until its Clear to Send input is ON.

2. A transition of the communication port's RS signal from ON to OFF instructs the DCE to complete the transmission of all data, to assume a non-transmit mode, and to remove the Clear to Send signal when the DCE is again prepared to receive another Request to Send input. Request to Send will not turn ON again until Clear to Send turns OFF.

CONFIGURATION

The communication port is configured through menu selections made on the 623-60 MS-DOS Loader or the 623-6100/6150 Loader/Terminal, which then stores these selections in the System Status Table of the 620-11/14/16 Logic Controller. (See Appendix II for full definitions.)

In order to enter the Communication Port Configuration Menu, the user must first access the 620 Selection Menu, then enter the Processor Configuration Menu. (See Figure 21.)

The following selections are in the Loader/ Terminal Port Configuration menu:

- Port Enable.................................. (Enable, *Disable)
- Protocol............(*Honeywell ABC, MODBUS RTU)
- Nodal Address.................................(*0 - 255)
- Baud Rate...................................(110, 300, 600, *1200, 2400, 4800, 9600, 19,200)
- Parity...(*Odd, Even, None)
- Stop Bits...(*1, 2)
- Port Operation..............(*Full Duplex, Half Duplex)
- Memory Write Protect................................(*On, Off)
- Output Write Protect..................................(*On, Off)
- Flag Mode..................................... (Enable, *Disable)
- Test Mode.......................................(Enable, *Disable)

* denotes default selections

Figure 21 shows a sample Loader/Terminal configuration screen for the communication port. All settings pictured are default settings.

NOTE
The default setup only applies to the first application of power to a non-configured system. Once configuration selections are made, they are retained in the Control Processor Module's battery-backed memory. As long as memory remains intact, the communication port will configure itself according to user selections on subsequent power cycles.

The user can edit the Serial Port Configuration by pressing F8 on the Processor Configuration Menu. The individual options on the Serial Port Configuration Menu can be selected by pressing the appropriate function key (F1-F10). Keys with multiple options can be selected by pressing the key repeatedly to examine all options.

620 Selection Menu

F1	Model Number: 620-16	**F2**	Memory Size: 8192
F3	Register Size: 4096	**F4**	Real I/O size: 2048
F5	Edit Processor Configuration	**F6**	Edit I/O Configuration
F7	Verify Processor Configuration	**F8**	Verify I/O Configuration
F9		**F10**	

Press [Enter] to continue

Press F5 to enter Processor Configuration Menu

Processor Configuration Menu

F1	Run Mode Programming: DISABLE	**F2**	Force Functions: DISABLE
F3	Scan with Low Battery: DISABLE	**F4**	Data Change Function: ENABLE
F5	Scan Watchdog Timer: ENABLE	**F6**	On Mode Change I/O will: CLEAR
F7	Serial Port: DISABLE	**F8**	Serial Port Configuration
F9	Load Processor Configuration	**F10**	Save Processor Configuration

Press [Enter] To Keep Changes   [Esc] to Exit

Press F8 to enter Serial Port Configuration Menu

Serial Port Configuration

F1	Port Operation:FULL DUPLEX	**F2**	Baud Rate: 1200
F3	Parity: ODD	**F4**	Stop Bits: 1
F5	Nodal Address: 0	**F6**	Protocol: ABC
F7	I/O Write Protect: ON	**F8**	Memory Write Protect: ON
F9	Flag Mode: DISABLE	**F10**	Test Mode: DISABLE

FIGURE 21 - COMMUNICATION PORT CONFIGURATION SCREEN ON LOADER/TERMINAL

MENU SELECTIONS

Processor Configuration Menu

F7 Port Enable - This selection determines the active or inactive status of the port. This selection is located in the Processor Configuration Menu.

F8 Serial Port Configuration - Allows the user to view the Serial Port Configuration Menu.

Serial Port Configuration Menu

F1 Port Operation - This selection determines how the port Transmit and RTS drivers are controlled. In the Full Duplex/Point-to-Point mode, the drivers are always enabled. In the Half Duplex/Multidrop mode, the drivers are tri-stated whenever the port is not transmitting.

F2 Baud Rate - This selection determines the baud rate at which the port transmitter and receiver will operate.

110	300	600	1200*
2400	4800*	9600*	19,200*

*Rates compatible with MODBUS RTU

F3 Parity - This selection determines the parity, if any, associated with a message character.

F4 Stop Bits - This selection determines the number of stop bits that delimit a message character.

F5 Nodal Address - This selection specifies the network Nodal Address assigned to the port. The Honeywell ABC protocol is limited to addresses 0-31. The MODBUS RTU protocol allows addresses 1-255.

F6 Protocol - This selection determines the protocol under which the port will operate.

F7 Output Write Protect - This selection determines whether the port will accept or reject instructions that involve writing to real outputs, the output status table, or the register table. Selecting ON will reject such instructions.

F8 Memory Write Protect - This selection determines whether the port will accept or reject instructions that involve writing to the user program memory or System Status Table. Selecting ON will reject such instructions.

F9 Flag Mode - This selection determines whether flag mode is active. If flag mode is selected, the port will monitor specified I/O addresses and transmit an unsolicited message whenever an off-on state change is detected. Note that flag mode is only compatible with the Full Duplex/Point-to-Point mode and the ABC protocol. (See the Honeywell ABC Protocol section of this manual for more details).

F10 Test Mode - This selects a test mode in which the communication port will continuously transmit a fixed data pattern onto the serial network. The purpose of this test is to generate a symmetrical wave form that can be monitored with an oscilloscope in order to verify proper installation and wave shape at all nodes on the link.

ERROR DISPLAYS

These displays occur if a faulty configuration is entered or if there is a communication port failure.

Illegal Flag Mode - This display indicates that an invalid combination of flag mode and half duplex mode has been selected and that flag mode, though selected, is disabled. Flag mode is compatible with full duplex operation only.

Illegal Baud Rate - This display indicates that an invalid combination of baud rate and protocol has been selected.

Illegal Address - This display indicates that an invalid combination of nodal address and protocol has been selected.

Transmitter Failure - This display indicates that the port transmitter is not functional.

INSTALLATION

COMMUNICATION PORT SIGNAL CABLE WIRING

General Considerations

Observe these considerations when installing the 620-11/14/16 Control Processor Module with the communication port.

- Maintain a 60°C or less ambient air temperature at the bottom of each 620 system rack assembly.
- Separate all 440VAC (or higher) electrical supply lines as far from the 620 components as practical.
- All 440VAC lines must be run in separate conduit from I/O wiring ducts.
- Separate AC and data wiring as far as practical.
- All wiring should be installed according to IEEE Standard 518-1977.
- Two cables carrying different types of signals (Data versus power) should cross at right angles rather than running parallel for any distance.

- All data cable should be terminated at both ends, excluding the shield. If a termination is not made or is intermittent, noise immunity is lost even though the system may transmit valid data.
- Ensure that the entire Communication Network System is grounded to earth ground. The maximum ground reference voltage is 5 volts.
- Shield continuity must be maintained. Ensure that shield leads are not broken.
- Cables should be routed around rather than through high noise areas.
- Route shielded data cable along grounded surfaces such as metal cabinet walls and in conduit or trays. Single shield cable is most effective when routed along grounded surfaces.
- Allow the minimum amount of unshielded wire that will accommodate connection.

Raceway Shielding

Table 9, showing raceway shielding, is taken from IEEE standard 518 for the installation of electrical equipment. It compares different types of conduits and raceways for magnetic field attenuation at 60 Hz and for electrostatic attenuation at 100 KHz.

TABLE 9 - RACEWAY SHIELDING

RACEWAY TYPE	THICKNESS in. (mm)	60 Hz MAG. FIELD ATTENUATION		100 Hz ELEC. FIELD ATTENUATION	
		Ratio	dB	Ratio	dB
Free air		1:1	0	1:1	0
2-inch aluminum conduit	.154 (3.91)	1.5:1	3.3	2150:1	66.5
#16 gauge aluminum tray	.060 (1.52)	1.6:1	4.1	15500:1	83.9
#16 gauge aluminum tray	.060 (1.52)	3:1	9.4	20000:1	86.0
#16 gauge galv. ingot iron tray	.060 (1.52)	3.2:1	10.0-	22000:1	86.8
2-inch IPS copper pipe	.156 (3.96)	3.3:1	10.2	10750:1	80.6
#16 gauge aluminum tray	.060 (1.52)	4.2:1	11.5	29000:1	89.3
#14 gauge aluminum tray	.075 (1.90)	6:1	15.5	23750:1	87.5
2-inch metallic tubing	.065 (1.65)	6.7:1	16.5	3350:1	70.5
2-inch rigid galv. conduit	.154 (3.91)	40:1	32.0	8850:1	78.9

Conduit Shielding

Conduit or cable trays are used to route the network trunkline within the plant, for short distances or for several miles. Often the same conduit is used to carry both data and power wiring, creating a problem with electromagnetic interference. The choice of materials and configuration for the cable conduit can determine the degree of protection from this interference.

Cable Spacing

It is advisable to separate noise-creating sources (those with time-varying voltage or time-varying current) from data signal cable. Cables with similar levels of noise susceptibility should be grouped together and those with similar levels of noise generation should be grouped separately in trays and conduits.

IEEE 518 defines four classes of wiring that differ in signal level and noise susceptibility:

- Data 1 - High noise susceptibility. Analog signals of less than 50V and digital signals of less than 15V.
- Data 2 - Medium susceptibility. Analog signals greater than 50V, regulating signals of 50V with currents less than 20 amps; AC feeders less than 20 amps.
- Data 3 - Low susceptibility. Switching signals greater than 50V, analog signals of 50V with currents less than 20 amps; AC feeders less than 20 amps.
- Data 4, Power - AC and DC buses of 0-1000V with currents of 20-800 amps.

Data 3 and Data 4 classes have a subclass for applications that require special cable and spacing. In the following tables, the subclass for Data 3 is listed as 3A; the subclass for Data 4 is listed as 4A. (See IEEE 518 for complete information on wiring classes and subclasses.) Examples of Data 3A and Power 4A are:

- Signals from communicating fields and line resistors.
- Signals from shunts to regulators.
- Power greater than 1000 volts and/or 800 amps.

Tray Spacing

Tables 10, 11 and 12 list the recommended mini-mum distances between trays, trays and conduits, and conduits, respectively. The dimensions provided in the tables are between the top of one tray/conduit and the bottom of the tray/conduit above, or between sides of adjacent trays/conduits.

Trays containing Data 1 or 2 cables should have a solid bottom and covers to complete shielding. Ventilation slots or louvers may only be used in trays containing Data 3 cables.

Tray Considerations

- When separate trays are impractical, Data 1 and 2 cables may be placed in the same tray, provided that they are separated by a grounded steel barrier.
- Trays containing Data 1 and 2 cabling should have solid bottom and tray covers to provide complete shielding.
- Ventilation slots or louvers may only be used in trays containing Data 3 cables.

Grounding

Adequate grounding is important for safety considerations and to reduce electromagnetic noise interference. A grounding path for the system components and enclosures should be provided. This ground is connected to the central ground for all electrical equipment and AC power within the user's facility (earth ground). All earth ground connections must be permanent and provide a continuous low-impedance path to earth ground for induced noise currents and fault currents.

System ground is accomplished by the mounting hardware. A rack assembly grounding screw (optional) is provided with each 620 chassis for customer use to connect the system components to earth ground. Local electrical codes must be observed when installing a 620-11/14/16 Logic Controller System.

See the 620 Installation Manual (Form No. 620-8996) for more information on grounding.

TABLE 10 - TRAY SPACING (INCHES)

CABLE CLASS	DATA 1	DATA 2	DATA 3	DATA 3A	DATA 4	DATA 4A
DATA 1		NOTE 2	6	6	26	26
DATA 2	NOTE 2		6	6	18	26
DATA 3	6	6		0	NOTE 1	12
DATA 3A	6	6	0		8	18
DATA 4	26	18	NOTE 1	8		0
DATA 4A	26	26	12	18	0	

NOTE 1: Data 3 and 4 cables may be run in a common tray but should be separated by a barrier. This barrier does not have to be grounded.

NOTE 2: Data 1 and 2 cables may be run in a common tray, provided they are separated by a grounded steel barrier.

TABLE 11 - TRAY — CONDUIT SPACING (INCHES)

CABLE CLASS	DATA 1	DATA 2	DATA 3	DATA 3A	DATA 4	DATA 4A
DATA 1		1	4	4	18	18
DATA 2	1		4	4	12	18
DATA 3	4	4		0	0	8
DATA 3A	4	4	0		6	12
DATA 4	18	12	0	6		0
DATA 4A	18	18	8	12	0	

TABLE 12 - CONDUIT SPACING (INCHES)

CABLE CLASS	DATA 1	DATA 2	DATA 3	DATA 3A	DATA 4	DATA 4A
DATA 1		1	3	3	12	12
DATA 2	1		3	3	9	12
DATA 3	3	3		0	0	6
DATA 3A	3	3	0		6	9
DATA 4	12	9	0	6		0
DATA 4A	12	12	6	9	0	

NETWORKING

COMMUNICATION CONFIGURATIONS

There are two types of configurations for interconnecting the communication port of a 620-11/14/16 Logic Controller System to a host computer.

A point-to-point connection is between only two points. A multidrop configuration connects three or more points on a common line. There is a single master and a series of slaves in this configuration. (See Figure 22.)

COMMUNICATION WIRING DIAGRAMS

Figures 23, 24, 26 and 27 show RS422/485 network wiring information for all communication port configurations.

CABLE IDENTIFICATION

Cable manufacturers color code multipair cable to aid in the identification of conductors. Identify the cable conductors to network function before installation.
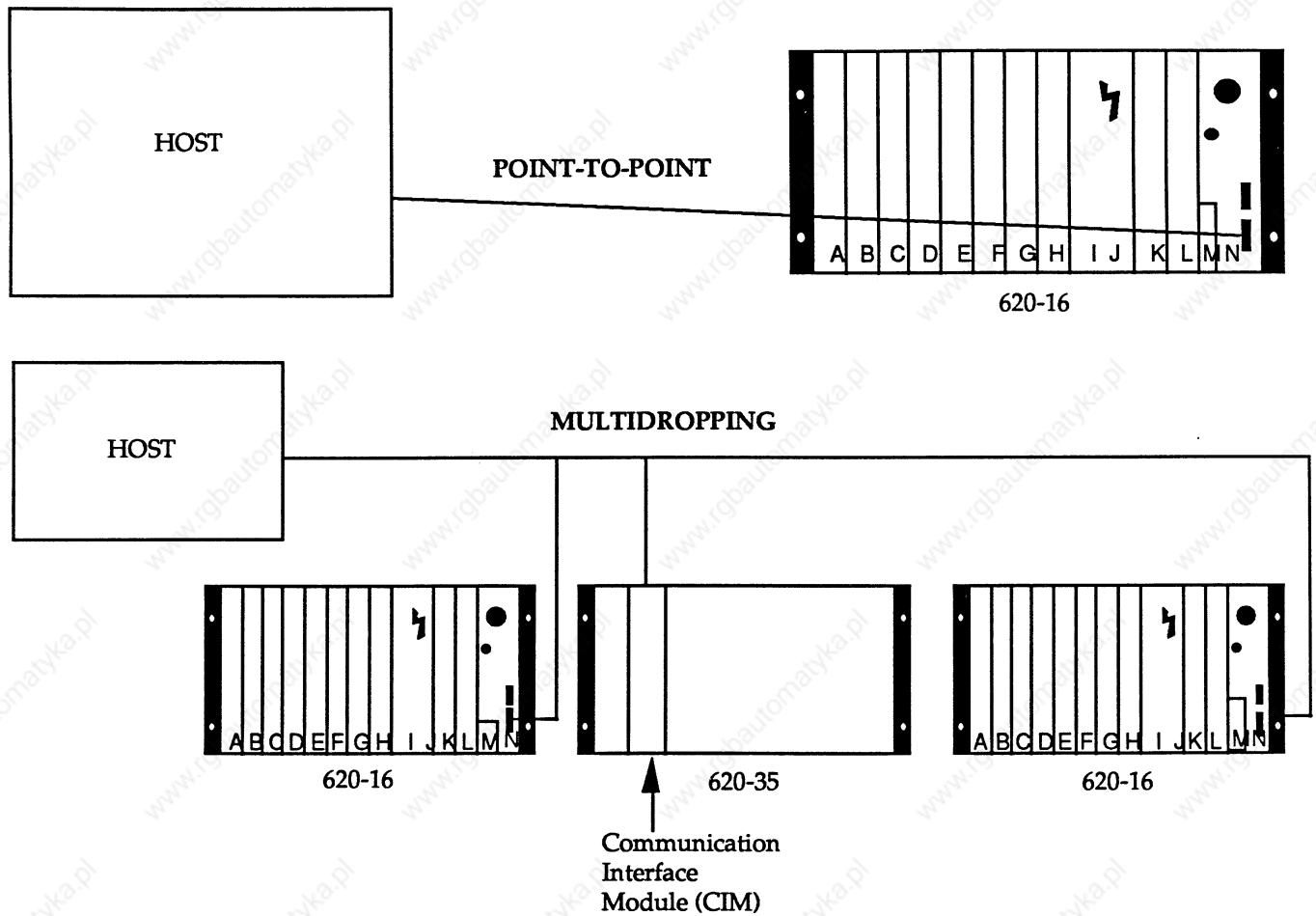
FIGURE 22 - EXAMPLE POINT-TO-POINT AND MULTIDROP CONFIGURATION

POINT-TO-POINT NETWORKING

RS422/485 point-to-point network specifications are:

- Maximum Trunk Length: Cable dependent
- Data Rates: 110, 300, 600, 1200, 2400, 4800, 9600 & 19.2K baud
- Configuration Selection: Full duplex required

POINT-TO-POINT NETWORK TOPOLOGY

Point-to-point networking of 620-11/14/16 communication ports to a host can be implemented with either single or multiple twisted pair cable.

Figure 23 illustrates the basic point-to-point network topology when connected to a modem. The connection may be either three single twisted pair cables or one three-twisted pair cable.

The connection of the RS422/485 interface to a modem (DCE) that operates on a multidrop network is actually a point-to-point connection from the port standpoint. The line configuration should be set for full duplex, so that the Logic Controller communication port operates in a point-to-point mode.

Figure 24 illustrates the basic point-to-point network topology when connected directly to the host. The connection consists of either two single twisted pair cables or one two twisted pair cable.

NETWORK TERMINATION

Resistors must be attached across each twisted pair at the receiving end. For best results, the resistor value should equal or closely approximate the characteristic impedance of the cable. The resistor power rating should be 1/8 watt or greater.

The 620-11/14/16 Logic Controllers have jumper-selectable 120-ohm terminating resistors installed on the processor board. In the point-to-point mode, the RD line is terminated by installing jumper P6 at the port (see Figure 25). The resistors can be disconnected from the network by removing the jumper.

The SD line and RS line (if used) must be terminated at the host or DCE. The CS line (if used) has a fixed terminating resistor (120 ohms) installed at the port.

```
          620-11/14/16 LCS                    MODEM
          COMMUNICATION PORT
    *SHIELD  ——————————————————————  SHIELD
      SD-A    15 ———————————————————  SD-A'
      SD-B    14 ———————————————————  SD-B'
     RD-A'    22 ———————————————————  RD-A
     RD-B'    21 ———————————————————  RD-B
      RS-A    12 ———————————●————————  RS-A'
      RS-B    13 ———————●————┘         RS-B
     CS-A'    17 ————————┘
     CS-B'    16 ————————┘
```
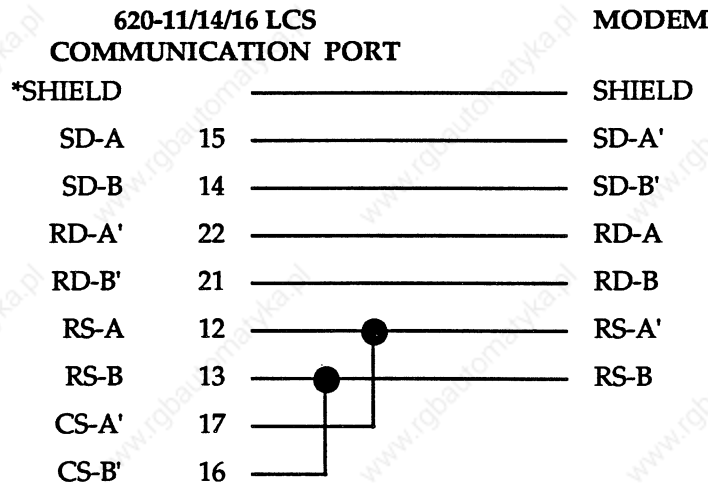
* Connect shield to connector housing.

FIGURE 23 - RS422/485 CONNECTION TO MINIMUM FUNCTION MODEM (POINT-TO-POINT)

620-11/14/16 LCS
COMMUNICATION PORT   **HOST**

*SHIELD		SHIELD
SD-A	15	SD-A
SD-B	14	SD-B
RD-A'	22	RD-A'
RD-B'	21	RD-B'
RS-A	12	RS-A
RS-B	13	RS-B
CS-A'	17	CS-A'
CS-B'	16	CS-B'
		RR-A'
		RR-B'
		GND
		+12V/+5V

*Connect shield to connector housing.

FIGURE 24 - RS422/485 CONNECTION TO HOST (POINT-TO-POINT)

Note: 620-11/14/16 Control Processor Modules are shipped with Jumper P6 installed. Removal of Jumper P6 disconnects the terminating resistor from the network.

Battery holder

Keyswitch cylinder

Front of 620-11/14/16 Control Processor Module

P6

Bottom of printed circuit board

P5 P6
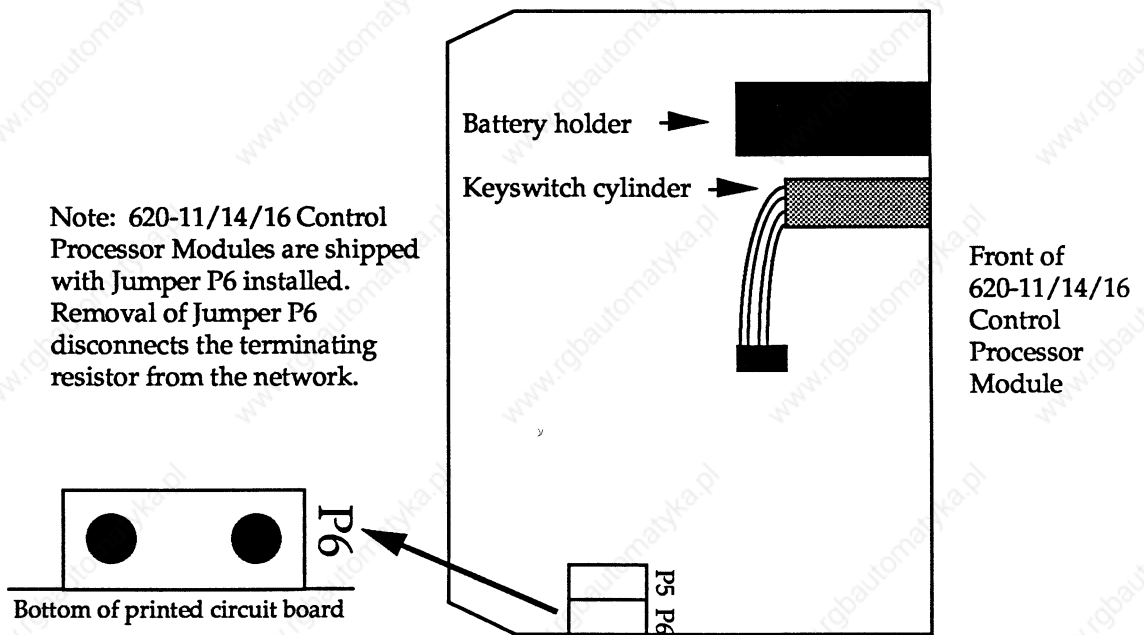
FIGURE 25 - JUMPER P6 INSTALLED FOR TERMINATING RESISTOR

MULTIDROP NETWORKING

The 620-11/14/16 communication port is designed as an RS422/485 multidrop compatible serial port, therefore it is possible to configure a multidrop network without modems. Multidrop network specifications are:

* Maximum Population: 32 compatible communication devices per network trunk
* Maximum Trunk Length: Cable dependent
* Maximum Branch Length: 2 feet (61 cm)

NOTE
The branches may be located at any point along the network trunk without restrictions.

* Data Rates: 110, 300, 600, 1200, 2400, 4800, 9600 & 19.2K baud
* Requires half duplex configuration selection

MULTIDROP NETWORK TOPOLOGY

Multidrop networking of 620-11/14/16 communication ports to a host can be implemented with either single or two twisted pair cable.

Figure 26 illustrates the basic single twisted pair network topology. The network trunk consists of a single twisted pair cable. The cable serves as an output line for host transmissions to the communication port and as an input line for communication port response transmissions to the host.

NOTE
To operate a single twisted pair network, the host Send Data (SD) line driver must be configured to switch into the tri-state mode when its serial interface is not in the transmit mode. To do this, connect the tri-state control of the SD line driver to the Request to Send signal.

Figure 27 shows the basic two twisted pair network topology. The network trunk consists of two twisted pair cables. Trunk T serves as an output line for host transmission to the communication ports. Trunk R serves as an input line for communication port response transmissions to the host. Either two single twisted pair cables or one two-twisted pair cable may be used for two twisted pair networks.

MULTIDROP NETWORK INSTALLATION

The network trunk cable must be routed past the 620-11/14/16 Control Processor Module. Branches from the network trunk connect the communication port to the trunk and are limited to two feet. The branch cable may be the same type as the trunk or a less rigid type of the same quality (e.g., Belden 9182 for the network trunk and Belden 9729 for the branches).

MULTIDROP NETWORK TERMINATION

Resistors must be attached to each end of each pair of network trunk cable. Two resistors are required for single pair networks and four are required for two pair networks (see Figure 28). For best results, the resistor value should equal or closely approximate the characteristic impedance of the cable. The resistor power rating should be 1/8 watt or greater.
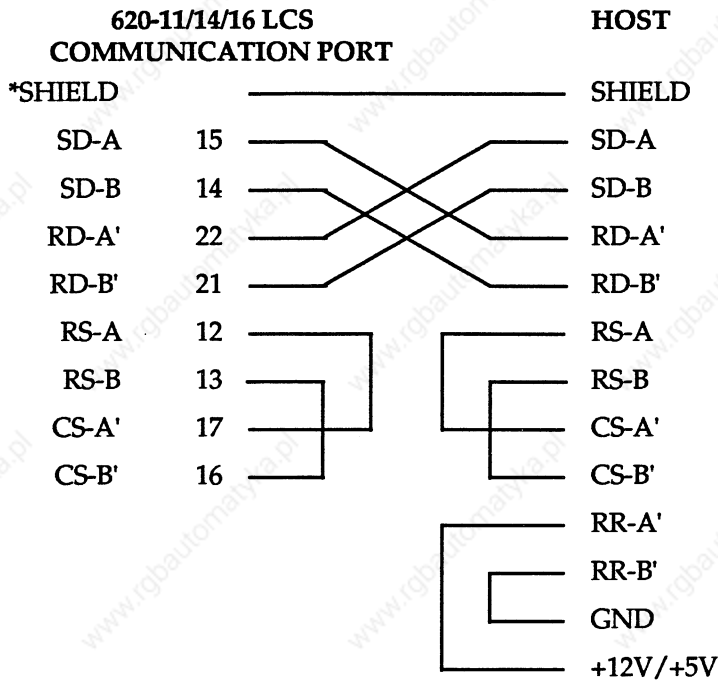
For single twisted pair networks, the termination can be accomplished by installing jumper P6 (see Figure 25) on the ports at the ends of the trunk. Jumper P6 must be removed on ports that are not at the ends of the trunk. For two twisted pair networks, the termination of the T trunk can be accomplished in the same fashion. Termination of the R trunk can be done by installing discrete resistors across the Send Data (SD) terminals by soldering at the end port connector or branch junction box. Note that Figure 28 and the above discussion assume that ports are at both ends of the network. If however, the host is at one end, the proper terminating resistors must be installed at the host.

620-11/14/16 LCS COMMUNICATION PORT

NETWORK TRUNK

*SHIELD	
SD-A	15
SD-B	14
RD-A'	22
RD-B'	21
RS-A	12
RS-B	13
CS-A'	17
CS-B'	16

SD/RD-A   SD/RD-B
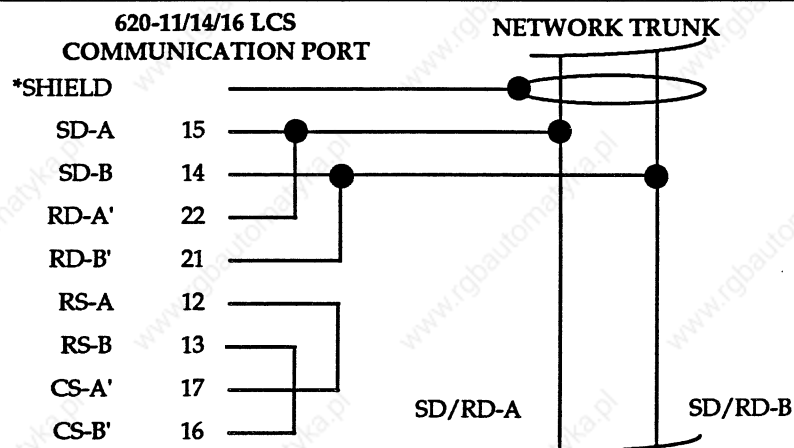
*Connect shield to connector housing.

FIGURE 26 - RS422/485 SINGLE TWISTED PAIR NETWORK CONNECTION (MULTIDROP)

620-11/14/16 LCS
COMMUNICATION PORT

NETWORK TRUNK

*SHIELD		
SD-A	15	
SD-B	14	
RD-A'	22	
RD-B'	21	
RS-A	12	
RS-B	13	
CS-A'	17	
CS-B'	16	

TRUNK R

TRUNK T
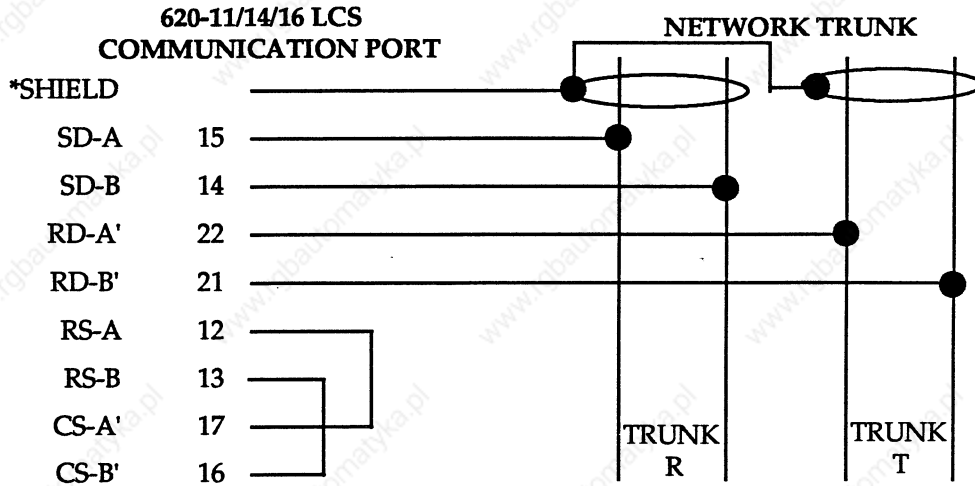
*Connect shield to connector housing.

FIGURE 27 - RS422/485 TWO TWISTED PAIR NETWORK CONNECTION (MULTIDROP)

HOST COMPUTER

R (t)   TRUNK R   R (t)

TERMINATING RESISTOR

R (t)   TRUNK T   R (t)

TERMINATING RESISTOR

PORT   PORT   PORT   PORT
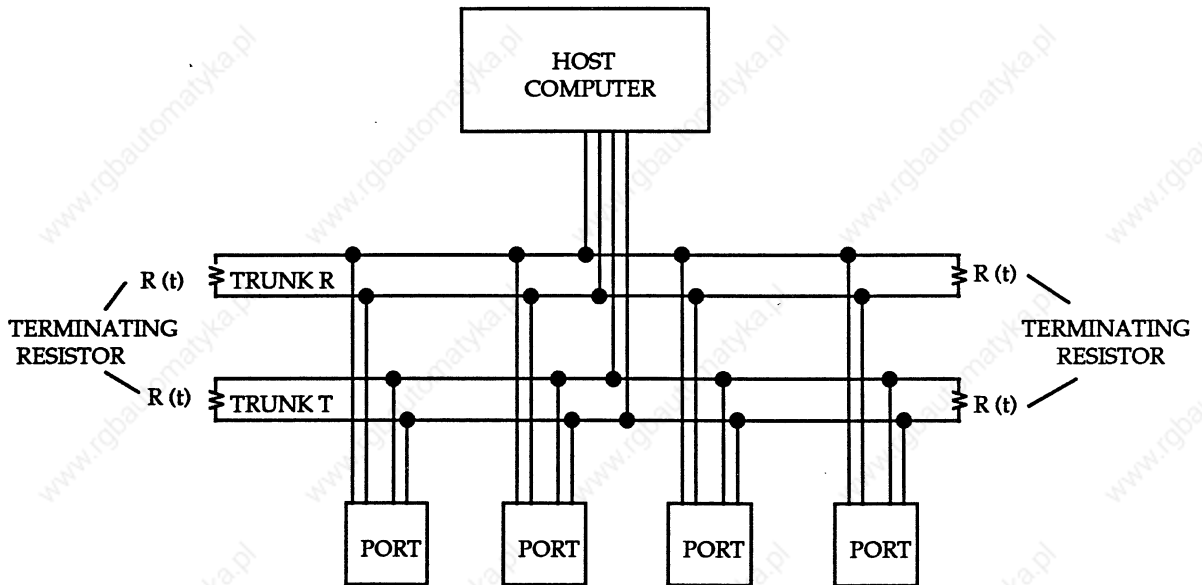
FIGURE 28 - TERMINATING RESISTOR LOCATION

HONEYWELL ABC PROTOCOL

When configured for the Honeywell Asynchronous Byte Count protocol, the communication port serves as a general purpose communication interface for the 620-11/14/16 Logic Controller. The Control Processor Module's (CPM's) user program memory contents, input/output status, or register contents may be examined or modified through the port. The port provides this access for manipulating or modifying data and for other services provided by external devices or host computers.

The communication port provides low-to-medium speed connection for the 620-11/14/16 Control Processor Module's to another computing device. When configured for Honeywell ABC protocol, the port provides a simple and easy to implement interface suitable for use in both point-to-point and multidrop network applications. Data transparency is achieved through a byte count procedure, eliminating the need for special data encoding or for character insertion and deletion.

GENERAL OPERATION

The 620-11/14/16 Control Processor Module gives the built-in communication port a time slot at the end of program scan. The communication port is synchronized to processor scan and partially dependent on the processor scan for its response time to received commands. During the time slot given, the communication port has access to the controller's I/O status, register contents, system registers, and program memory.

NOTE
Use of the communication port will increase scan times of the 620-11/14/16 Logic Controller by as much as 12 percent. (This refers to transmit/receive interrupts only.) MWZ windows may add more time. Maximum time for any given window in RVN mode is 19.1ms.

I/O Status Tables, Data Registers and System Registers can be read while the Control Processor Module is in the PROGRAM, RUN/PROGRAM or DISABLE mode. I/O tables and registers also can be written in any mode. If the CPM is in the DISABLE or PROGRAM mode, the write I/O instructions write to only the I/O table locations. The real I/O is not updated. If the CPM is in RUN/PROGRAM, the write instructions write to the I/O status table and the real I/O.

Program memory can be uploaded or downloaded while the CPM is in the PROGRAM, RUN/PROGRAM or DISABLE mode. Only one peripheral device can be downloading program memory at a time. Other memory instructions can be done only if the communication port has the CPM in the software PROGRAM mode.

FLAG MODE OPERATION

The flag mode, selectable through the Communication Port Configuration Menu, provides an alternative mode of operation. It allows the port to provide data to the host without the host requesting it. This data exchange occurs when specific control relays within the controller change from an OFF to ON state.

The flag bits are read at every Memory Word Zero (MWZ) window if the flag mode is enabled and the communication port is not receiving a message or servicing a command.

The communication port reads specified flag bits at the beginning of program memory scan. If an OFF to ON change has occurred since the last read, a response is prepared and transmitted to the host. See Flag Mode Operation Response, in the ABC Protocol Instruction Set section, for flag mode response format.

The following conditions must be met for flag mode operation:

1. Flag mode operation must be enabled by the communication port configuration selections.
2. Point-to-point serial port configuration must be selected. A direct connect full duplex connection is necessary.

In the 620-11/14/16 CPM, the range of flag bits is programmable. That is, the communication port defines a block of 16 addresses specified in the System Status Table for OFF-ON transition. The user can write to addresses 2501 (LSB) and 2502 (MSB) in the System Status Table or the Auxiliary menu (F12) on the Loader/Terminal to specify the most significant address of the desired range of flag bits. Otherwise, the 620-11/14/16 CPM defaults to addresses 2031-2016 to set the range of flag bits and the port will monitor these addresses for OFF-ON transitions.

DATA LINK CONTROL

The ABC procedures are written for general data link control, however the procedures involve characteristics specific to the port (see Appendix II).

PORT RECEIVER LIMITATIONS

The communication port receive buffer is 606 bytes. The port compares the message length character of any incoming instruction with the available buffer space. Any instruction that exceeds the buffer space is rejected.

The port does not support the reception of multiple messages. It allows for the reception of any one of the recognized instructions or a Poll command. After one instruction has been received, the receiver is disabled until that instruction is processed.

In the event of an immediate response session, the receiver is re-enabled at the completion of the response transmission. In the event of a polled response session, the receiver is re-enabled at the completion of the response preparation.

The receiver buffer does not hold the complete received instruction. The port receiver firmware removes these characters: Start of Header (SOH), End of Transmission Block (ETB), Start of Text (STX), checksum, and End of Text (ETX). The port stores nodal address and message length separately.

EXCHANGE PROCEDURES

The ABC protocol defines four exchange procedures:

1. Immediate Response
2. Polled Response Without Acknowledge
3. Polled Response With Acknowledge
4. Flag Response

In addition, there is a <u>Poll</u> command that operates as a subset of the Immediate Response exchange procedure. The port enters these response modes (see the flow diagram in Figure 29).

The Poll and Flag responses are single-window responses, requiring only one Memory Word Zero (MWZ) for data exchange. The others are single- or multiple-window responses, which may require the MWZ of more than one scan. See Figure 30 and the Multiple Window Exchange section of this manual.

Immediate Response Session

During this session the port receiver is disabled until completion of the response transmission. This includes the response to a Poll command.
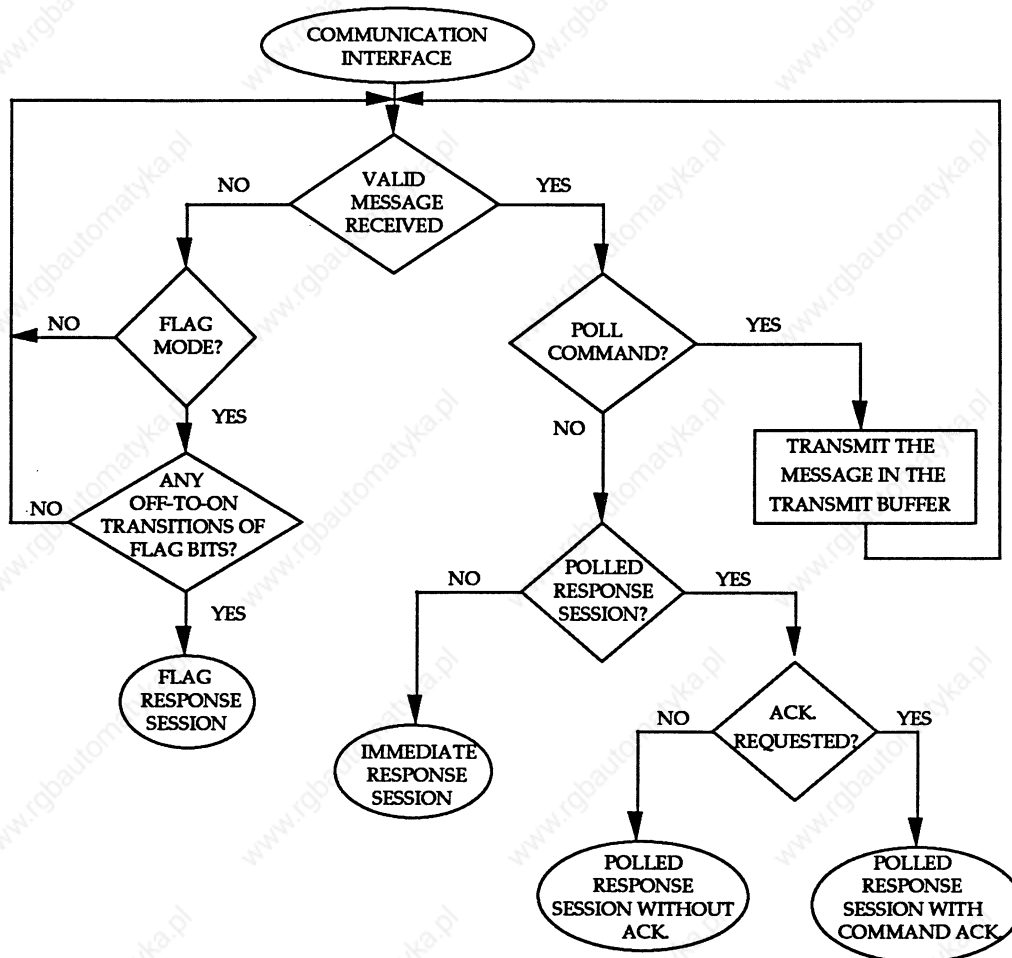
FIGURE 29 - COMMUNICATION PORT ABC PROTOCOL RESPONSE FLOW DIAGRAM

Polled Response Session With/Without Acknowledge

During the polled response session with or without immediate acknowledge, the receiver is disabled until the completion of the response preparation.

Flag Response Session

During the flag response session, the port receiver is enabled until a valid message is received.

Port Transmitter Limitations

The transmit buffer on the 620-11/14/16 Communication Port holds 610 bytes. This is sufficient to hold one complete response message.

Session Execution Time

Total exchange time is the sum of the times required by the operations listed in Table 13. This time frame extends from the host computer's decision to acquire certain information until the data is in the computer's data base.

- **Command Preparation and Response Processing** - Time for these operations is a function of the host computer.

- **Command/Response Transmission and Reception** - Time for these operations is a function of the baud rate and message size based on the following formula:

Transmission Time (ms) =

(1/Baud Rate) x (1000ms/sec.)
x (Bits/Character) x (No. of Characters)

- **Command Processing/Response Preparation** - Time for these operations varies slightly with each instruction.

- **Processor Scan Synchronization** - This is the time that elapses while the port waits for its window at the beginning of each scan (Memory Word Zero). The time is less than 2ms if the CPM is in the PROGRAM mode, or potentially equal to controller scan time if the processor is in the RUN/PROGRAM mode.

- **Processor Irregular Overhead** - This time is the result of external stimuli, such as Communication Interface Modules, the Loader/Terminal or the processor keyswitch, which extend Control Processor Module scan time between Communication Interface access windows. The Loader/Terminal can add up to 125ms to a scan, and each Communication Interface Module can add up to 90ms. If the CPM is switched from PROGRAM to RUN/PROGRAM mode, the communication port is denied access during processor diagnostics, which requires approximately 725ms.

- **Command Execution** - This is the time required by the communication port to execute the exchange once it receives a window at MWZ.

SESSION EXECUTION AND LOGIC CONTROLLER SYSTEM (LCS) EXCHANGE PROCEDURES

Since the 620-11/14/16 LCS built-in Communication Port is not an independent processor, much of the session execution processing is done directly by the CPM. This will result in slightly increased scan times for 620-11/14/16 CPMs performing communication tasks.

TABLE 13 - ABC OPERATIONS IN SESSION EXECUTION TIMES

COMPUTER OPERATIONS	620-11/14/16 LCS COMMUNICATION INTERFACE OPERATIONS
Command Preparation Command Transmission ⟶	Command Reception *Command Processing LCS Scan Synchronizations LCS Irregular Overhead *Command Execution *Response Preparation Response Transmission
Response Reception ⟵ Response Processing	
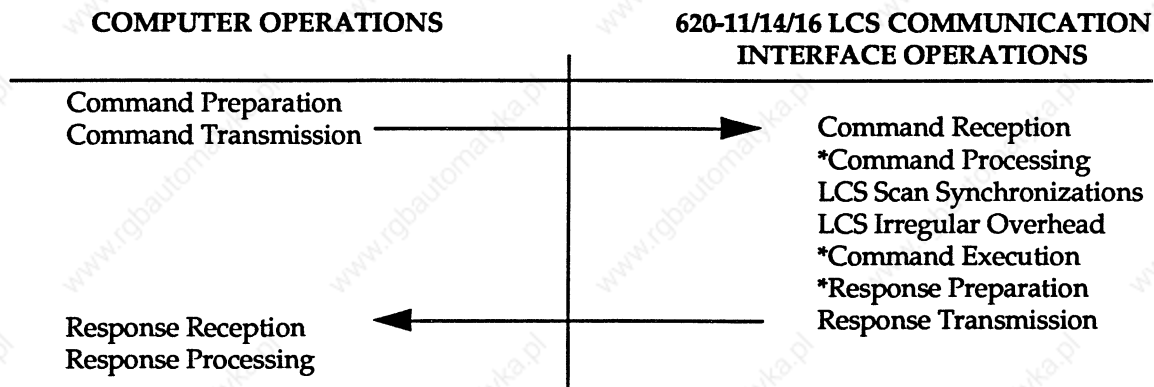
*These operations are performed during time slots granted by the 620 Logic Controller.

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With an independent CIM, the only effect of a communication session on an LCS was the "window" granted to the CIM for accessing the LCS data base. With the communication port, however, the LCS's scan is increased to receive and transmit interrupt service, command processing and response generation.

Multiple-Window Exchange

In order to keep scan-time increase at a minimum, the 620-11/14/16 Communication Port will service a communication session over a series of LCS scans. This is called a multiple-window exchange and it applies to most instructions.

In a typical communication port exchange, three LCS scans will be required to service a communication session (see Figure 30).

EXAMPLE:

- The Command Processing operation will perform message decoding/validation at Memory Word Zero (MWZ) on one scan;
- The Command Execution operation will access the LCS database at MWZ on the next scan;
- The Response Preparation operation will occur at MWZ on yet another LCS scan.

Single-Window Exchange

For ABC diagnostic instructions or ABC instructions in which no extensive interaction with the LCS database is required, the communication port will execute the command at the first MWZ slot granted by the LCS scan. These instructions are:

- 00 Read Port Status
- 54 Remove Software Program Mode Request
- 56 Modify Write Protect
- 80 Loop Back Test

Also, error detections will result in an immediate single-window execution.

NOTE
Equations listed in Table 14 (ABC Protocol Instruction, Opcodes, and Execution Times) determine the total time required within the MWZ time slot(s) for Command Processing, Command Execution and Response Preparation operations.

Transaction Records

An area has been reserved in the System Status Table to provide direct indication of communication port activity through the LCS. The data is a copy of the counters normally returned in response to a Read Port Status instruction. The user may access these records by executing a PULL from the System Status Table. See Read Port Status instruction for details.

EXAMPLE:

Status Table Organization

2504	Invalid Message Counter	LSB
2505		MSB
2506	Receiver Error Counter	LSB
2507		MSB
2508	Transmitted Message Counter	LSB
2509		MSB
2510	Receive Message Counter	LSB
2511		MSB

```
   2511                    AAAA = Data Register
-[PULS]--------------------(PSH)--
    4                        4
                         BBBB = Rcv. Mess. Counter
                         CCCC = Xmt. Mess. Counter
                         DDDD = Rcv. Error Counter
                         EEEE = Inv. Mess. Counter
```

SINGLE-WINDOW EXCHANGE — Interrupts → Receive Message ← Interrupts — **MULTIPLE-WINDOW EXCHANGE**

MWZ → Decode/Validate Message ← MWZ

Error

Execute Command ← MWZ

Prepare Response ← MWZ

Interrupts → Transmit Response ← Interrupts

IMMEDIATE RESPONSE

SINGLE-WINDOW EXCHANGE — Interrupts → Receive Message ← Interrupts — **MULTIPLE-WINDOW EXCHANGE**

MWZ → Decode/Validate Message ← MWZ

Error

Execute Command ← MWZ

Prepare Response ← MWZ

POLLED RESPONSE WITHOUT ACKNOWLEDGE

Execute Flag Window ← MWZ

Prepare Flag Response

Transmit Flag Response ← Interrupts

FLAG RESPONSE

SINGLE-WINDOW EXCHANGE — Interrupts → Receive Message ← Interrupts — **MULTIPLE-WINDOW EXCHANGE**

MWZ → Prepare Ack. Response ← MWZ

Interrupts → Transmit Ack. Response ← Interrupts

WAIT FOR ACK. COMPLETE

MWZ → Decode/Validate Message ← MWZ

Error

Execute Command ← MWZ

Prepare Response ← MWZ

POLLED RESPONSE WITH ACKNOWLEDGE

Receive Message ← Interrupts

Prepare Response ← MWZ

Transmit Response ← Interrupts

POLL RESPONSE

FIGURE 30 - ABC DATA EXCHANGE PROCEDURE DIAGRAMS

ABC PROTOCOL INSTRUCTION SET

The ABC protocol instruction descriptions that follow are separated into functional categories. Each actual instruction description includes title, definition and instruction, and response message formats. Only the text portion of the message format is provided. Figure 31 defines various characters of this text.

Table 14 lists the ABC protocol instructions, opcodes, and execution times that the communication port is programmed to recognize. Total ABC message format is listed in Appendix II.

The variable M represents the highest memory address available. The value of M depends on the type of 620 LCS, its memory configuration, and the type of memory accessed. The variable L represents the highest real I/O address available. The value of L depends on the type of 620 Control Processor Module. Table 15 shows these legal range values

In responses, opcodes will always be zero (0), indicating the instruction was executed with no errors. If the response opcode does not read zero, refer to the error codes in Table 16 at the end of the ABC protocol instruction set descriptions.

STX - (Start of Text) A data link control character.

Opcode - An 8-bit character that defines the instruction being given to the communication port, or the response being returned by the port.

Show Order of Transmission

Message Length - A 16-bit word which represents the number of bytes of data that follow this character in the message.

5	STX	OPCODE	6
7	MESSAGE LENGTH	8
9	N	10
11	STARTING ADDRESS	12
13	DATA	14
15	DATA	16

DATA FIELD — (bracket covering rows 9–15)

MSB   LSB

Starting Address - An opcode modifier representing the starting address for the operation. In most cases this address represents the least significant address of the data block involved.

N - An opcode modifier representing the number of bits, bytes, or words involved in the operation.

Data - The data involved in the message transfer. The organization of this data is defined for each instruction in the sections that follow.

FIGURE 31 - GENERAL ABC MESSAGE TEXT STRUCTURE

TABLE 14 - ABC PROTOCOL INSTRUCTION, OPCODES, AND EXECUTION TIMES

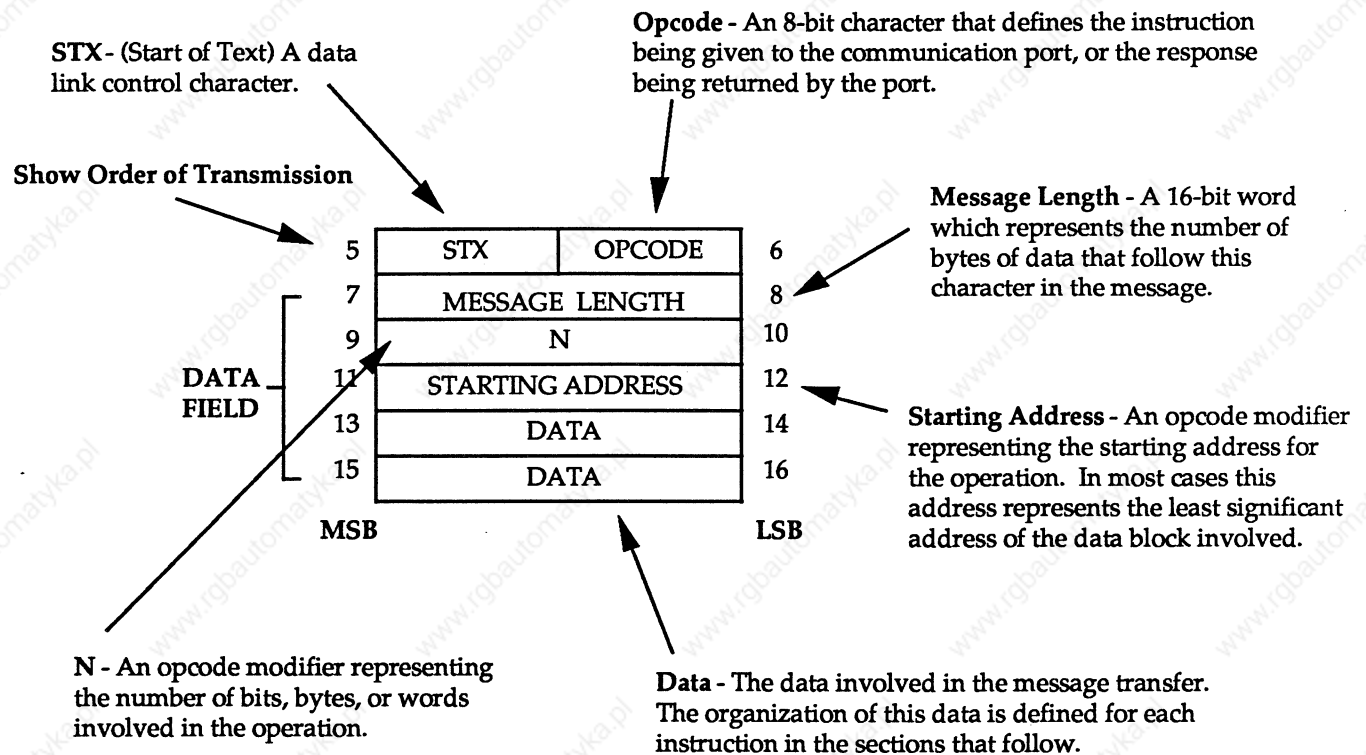| OPCODE (DECIMAL)	INSTRUCTION	EXECUTION TIMES
	Input/Output Instructions	
2	Read 16N I/O	227 µsec + N (36.2 µsec)
20	Read 16N Scattered I/O	203 µsec + N (51.8 µsec)
12	Write N Outputs	231 µsec + N (5.7 µsec)
14	Write 16N Outputs	235 µsec + N (60.7 µsec)
24	Write N Scattered Outputs	210 µsec + N (19.5 µsec)
	Register Instructions	
4	Read N Registers	229 µsec + N (10.8 µsec)
6	Read N Signed Registers	242 µsec + N (11.4 µsec)
22	Read N Scattered Registers	205 µsec + N (25.8 µsec)
16	Write N Registers	238 µsec + N (3.8 µsec)
18	Write N Signed Registers	238 µsec + N (3.8 µsec)
26	Write N Scattered Registers	210 µsec + N (19.8 µsec)
28	Pull N I/O Registers	237 µsec + N (55.5 µsec)
30	Push N I/O Registers	257 µsec + N (48.6 µsec)
8	Read N System Status Registers	216 µsec + N (12.3 µsec)
10	Write N System Status Registers	225 µsec + N (2.2 µsec)
	620 Processor Control Instructions	
52	Request PROGRAM Mode	200 µsec
54	Remove PROGRAM Mode Request	164 µsec
76	Write I/O Configuration	231 µsec + N (2.2 µsec)
78	Write Processor Control Configuration	202 µsec
	Program Memory Instructions	
34	Upload N Program Memory Words	227 µsec + N (36.6 µsec)
36	Download N Program Memory Words	314 µsec + N (125.3 µsec)
38	Clear Program Memory	22.2 msec
40	Insert N Program Memory Words	311 µsec + 3.2 µsec (EOP - SA) + N (78.5µsec)
42	Delete N Program Memory Words	297 µsec + 3.1 µsec [EOP - (SA + (N-1))] + N (48 µsec)
	Program Header Instructions	
64	Upload Program Date	225 µsec
66	Upload Programmer	348 µsec
68	Upload Title	773 µsec
70	Download Program Date	218 µsec
72	Download Programmer	261 µsec
74	Download Title	413 µsec
	Diagnostic Instructions	
0	Read DCM Status	234 µsec
80	Loop Back Test	176 µsec
	Other Instructions	
56	Modify Write Protect	166 µsec

N = N value from command
SA = Starting address from command
EOP = End of Program Address
(prior to command execution)

TABLE 15 - ABC LEGAL RANGES FOR COMMAND PARAMETERS

COMMAND TYPE	ABC LEGAL RANGES		
	620-1131 CPM	620-1431 CPM	620-1631 CPM
Real I/O	0-255	0-639	0-2039
Control I/O	0-4095	0-4095	0-4095
Registers	4096-8191	4096-8191	4096-8191
Status Registers	0-4095	0-4095	0-4095
Program Memory	8K	8K	8K

INPUT/OUTPUT INSTRUCTIONS

Input/output instructions provide access to the ON/OFF status of individual or groups of addresses in the 620/11/14/16's Input and Output Status Tables. READ I/O instructions obtain the status, and WRITE I/O instructions set the status.

The response to a successful READ I/O instruction is the logical "OR" of the input and output status locations asked for in the read I/O instruction. The response to a successful WRITE I/O instruction is an acknowledgement that the write was successful.

Read 16N I/O

This instruction reads the logical "OR" of N contiguous 16-bit address locations within the Input/Output Status Tables.

Instruction Format:
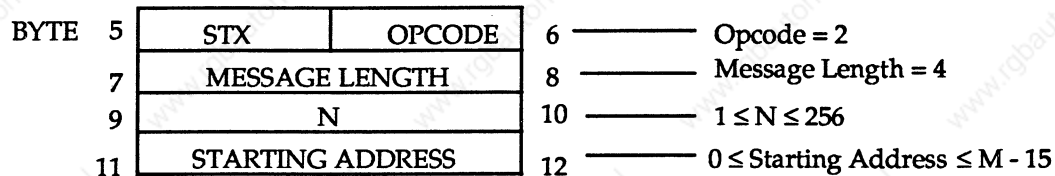
BYTE	5	STX	OPCODE	6	Opcode = 2
	7	MESSAGE LENGTH		8	Message Length = 4
	9	N		10	$1 \le N \le 256$
	11	STARTING ADDRESS		12	$0 \le$ Starting Address $\le M - 15$

Response Format (Instruction Executed):

Note: Data is justified to the least significant bit of the 16-bit word. The LSB of the first word (bytes 9, 10) is the data assigned to the starting address.

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	DATA		10	Data at Starting Address
	11	DATA		12	Data at Starting Address + 16 Addresses

Status 0 = OFF
1 = ON
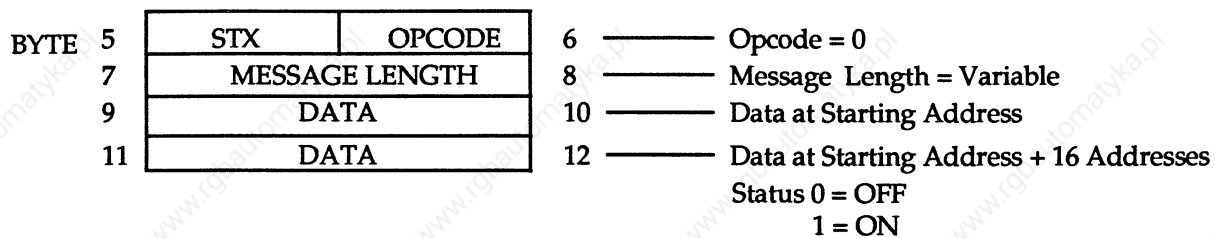
Read 16N Scattered I/O

This instruction reads the logical "OR" of non-contiguous, 16-bit groups of Input/Output addresses at various locations within the Input and Output Status Tables and control relay memory areas.

Instruction Format:

BYTE 5	STX	OPCODE	6 ——————— Opcode = 20
7	MESSAGE LENGTH		8 ——————— Message Length = Variable
9	N		10 ——————— $1 \leq N \leq 64$
11	STARTING ADDRESS A		12 ——————— $0 \leq$ Starting Address $\leq M - 15$
13	STARTING ADDRESS B		14
15	STARTING ADDRESS C		16

Response Format (Instruction Executed):

Note: Data is justified to the least significant bit of the 16-bit word. The LSB of the first word (bytes 9, 10) is the data assigned to the starting address.

BYTE 5	STX	OPCODE	6 ——— Opcode = 0
7	MESSAGE LENGTH		8 ——— Message Length = Variable
9	DATA A		10 ——— Data at Address A
11	DATA B		12 ——— Data at Address B
13	DATA C		14 ——— Data at Address C

Status 0 = OFF
1 = ON

Write N Outputs

This instruction writes N contiguous individual address locations in both the Output Status Tables and the real outputs. The communication port output write protect function must be disabled to execute this instruction.

Instruction Format:

Note: The data must be packed into 16-bit words with the least significant bit of the first data word (bytes 13, 14) representing the starting address data.

BYTE 5	STX	OPCODE	6 ——————— Opcode = 12
7	MESSAGE LENGTH		8 ——————— Message Length = Variable
9	N		10 ——————— $1 \leq N \leq 256$
11	STARTING ADDRESS		12 ——————— $0 \leq$ Starting Address $\leq M$
13	DATA		14 ——————— Data at Starting Address
15	DATA		16 ——————— Data at Starting Address + 16 Addresses

Status 0 = OFF
1 = ON

Response Format (Instruction Executed):

BYTE 5	STX	OPCODE	6 ——————— Opcode = 0
7	MESSAGE LENGTH		8 ——————— Message Length = 0

Write 16N Outputs

This instruction writes N contiguous 16-bit blocks of address locations in the Output Status Table and real outputs. The output write protect function must be disabled to execute this instruction.

Instruction Format:

Note: the data must be packed into 16-bit words, with the LSB of the first data word (bytes 13,14) representing the starting address data.

BYTE	5	STX	OPCODE	6	Opcode = 14
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 256$
	11	STARTING ADDRESS		12	$0 \leq$ Starting Address $\leq M - 15$
	13	DATA		14	Data at Starting Address
	15	DATA		16	Data at Starting Address + 16 Addresses

Status 0 = OFF
       1 = ON

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0

Write N Scattered Outputs

This instruction writes individual outputs at various non-contiguous locations in the Output Status Table. The output write protect function must be disabled to execute this instruction.

Instruction Format:

Note: The least significant bit of the 16-bit data word represents the desired status of the specified addresses. All other bits are disregarded.

BYTE	5	STX	OPCODE	6	Opcode = 24
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 64$
	11	ADDRESS A		12	$0 \leq$ Address $\leq M$
	13	DATA A (LSB)		14	Data at Address A
	15	ADDRESS B		16	$0 \leq$ Address $\leq M$
	17	DATA B (LSB)		18	Data at Address B

Status 0 = OFF
       1 = ON

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0

REGISTER INSTRUCTIONS

Register instructions obtain or set the contents of individual or groups of locations in the 620-11/14/16 CPM's Data Registers; transfer multiple 16-bit groups of data from I/O modules or the Register Table to the host; transfer multiple 16-bit groups of data from host to I/O modules or to the Register Table; or provide access to 620 Logic Controller System status information.

NOTE

Some ABC Register Instructions specifically apply to CPMs with 17-bit signed registers. The 620-11/14/16 CPMs have 16-bit registers. While signed register commands will not be rejected, they are of no special value. The sign bit area within a Read N Signed Registers Response will be filled with 0's. The sign bit area within a Write N Signed Registers command will be ignored.

Read N Registers

This instruction reads N contiguous Data Registers.

Instruction Format:

BYTE

5	STX	OPCODE	6 ——— Opcode = 4
7	MESSAGE LENGTH		8 ——— Message Length = 4
9	N		10 ——— $1 \leq N \leq 256$
11	STARTING ADDRESS		12 ——— $4096 \leq$ Starting Address $\leq M$

Response Format (Instruction Executed):

BYTE

5	STX	OPCODE	6 ——— Opcode = 0
7	MESSAGE LENGTH		8 ——— Message Length = Variable
9	DATA		10 ——— Data at Starting Address
11	DATA		12 ——— Data at Starting Address + 1

Data = Contents (0-65535)

70

Read N Signed Registers

This instruction reads N contiguous Data Registers. The sign bit area within a Read N Signed Registers response will be filled with 0's since this applies only to CPMs with 17-bit registers.

Instruction Format:

BYTE 5	STX	OPCODE	6	———— Opcode = 6
7	MESSAGE LENGTH		8	———— Message Length = 4
9	N		10	———— $1 \leq N \leq 256$
11	STARTING ADDRESS		12	———— $4096 \leq$ Starting Address $\leq M$

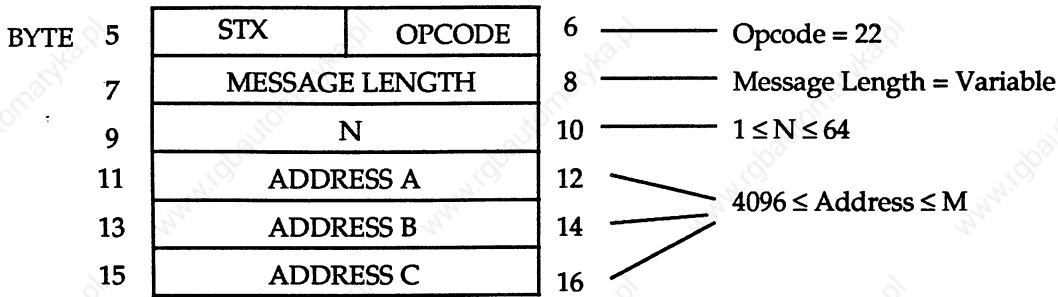Response Format (Instruction Executed):

NOTE
The sign bits are packed into 16-bit data words following the register data field, with the least significant bit corresponding to the first register's sign bit status.

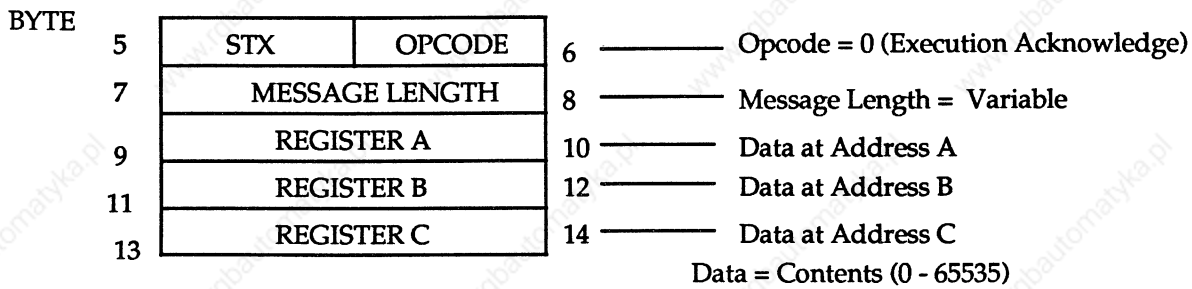| BYTE 5	STX	OPCODE	6	——— Opcode = 0
7	MESSAGE LENGTH		8	——— Message Length = Variable
9	REGISTER DATA		10	——— Data at Starting Address
11	REGISTER DATA		12	——— Data at Starting Address + 1
				Data = Contents (0-65535)
7 + 2N	REGISTER DATA		8 + 2N	
9 + 2N	SIGN BITS		10 + 2N	Sign Bits = 0
11 + 2N	SIGN BITS		12 + 2N	

Read N Scattered Registers

This instruction reads individual Data Registers at various non-contiguous locations in the Data Register Table.
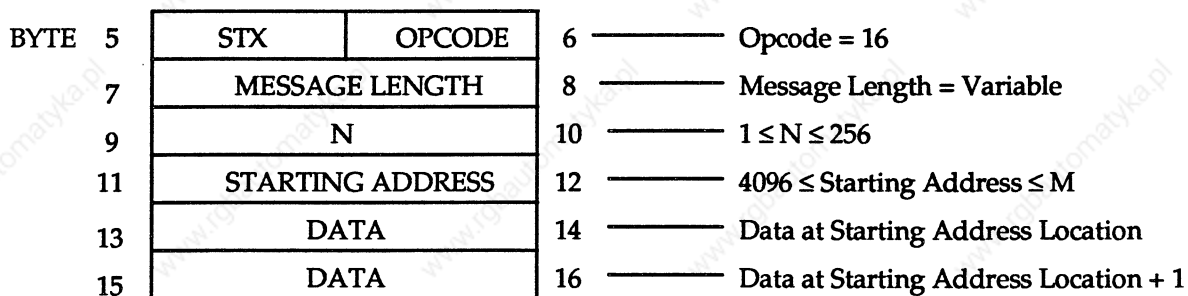
Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 22
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 64$
	11	ADDRESS A		12	
	13	ADDRESS B		14	$4096 \leq$ Address $\leq M$
	15	ADDRESS C		16	

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0 (Execution Acknowledge)
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	REGISTER A		10	Data at Address A
	11	REGISTER B		12	Data at Address B
	13	REGISTER C		14	Data at Address C

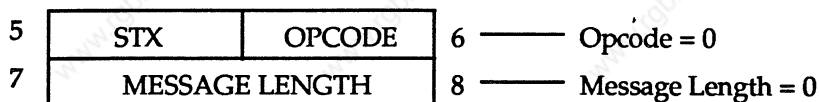Data = Contents (0 - 65535)

Write N Registers

This instruction writes to N contiguous locations in the Data Register Table. The output write protect function must be disabled to execute this instruction.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 16
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 256$
	11	STARTING ADDRESS		12	$4096 \leq$ Starting Address $\leq M$
	13	DATA		14	Data at Starting Address Location
	15	DATA		16	Data at Starting Address Location + 1

Data = Contents (0 - 65535)

Response Format (Instruction Executed):

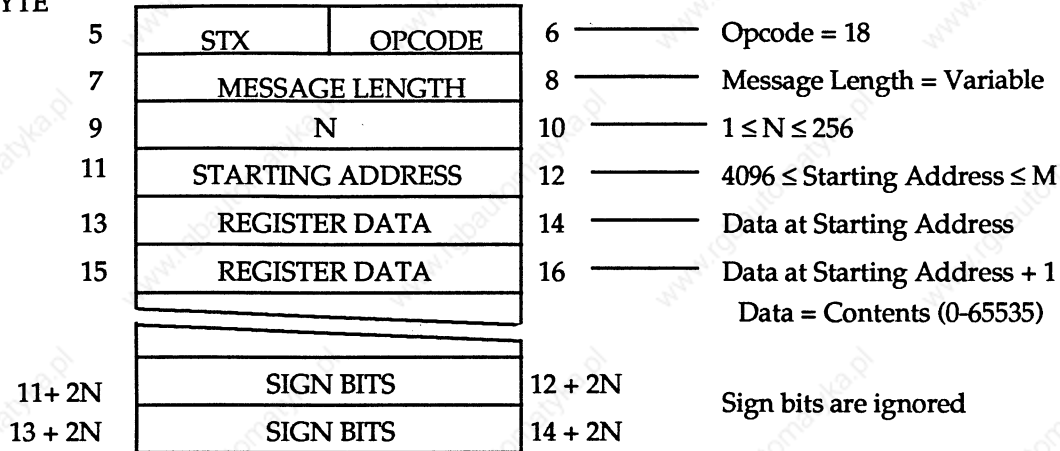|	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0

Write N Signed Registers

This instruction writes to N contiguous locations in the Data Register Table. The sign bit area within a Write N Signed Registers command will be ignored since this applies only to CPMs with 17-bit registers. The output write protect function must be disabled to execute this instruction.
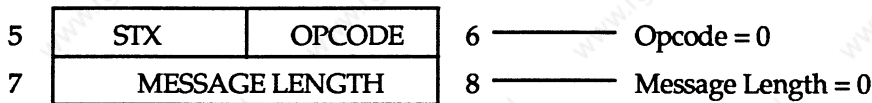
Instruction Format:

Note: The sign bits are packed into 16-bit data words following the register data field, with the least significant bit corresponding to the first register's sign bit status.
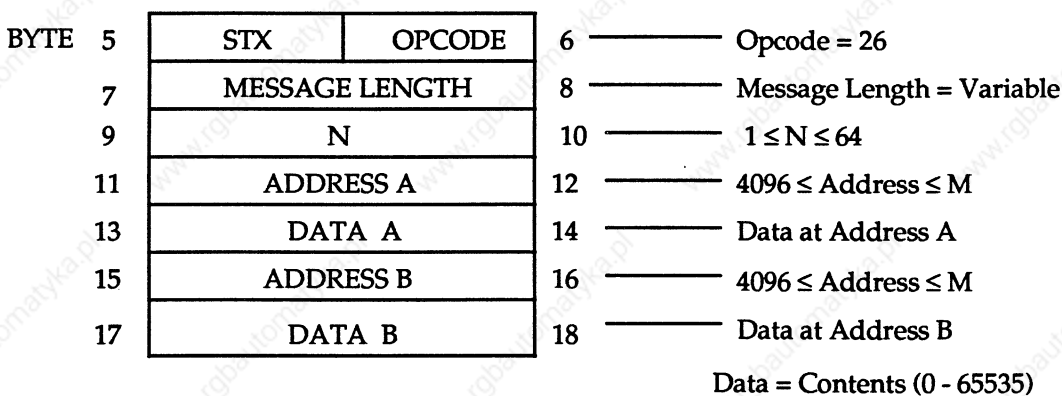
BYTE

BYTE				
5	STX	OPCODE	6	Opcode = 18
7	MESSAGE LENGTH		8	Message Length = Variable
9	N		10	$1 \leq N \leq 256$
11	STARTING ADDRESS		12	$4096 \leq$ Starting Address $\leq M$
13	REGISTER DATA		14	Data at Starting Address
15	REGISTER DATA		16	Data at Starting Address + 1
				Data = Contents (0-65535)
11+ 2N	SIGN BITS		12 + 2N	Sign bits are ignored
13 + 2N	SIGN BITS		14 + 2N	

Response Format (Instruction Executed):

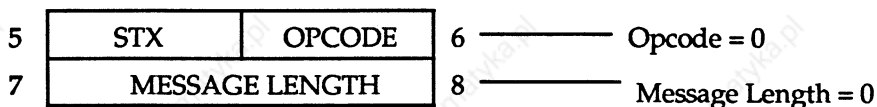|				
5	STX	OPCODE	6	Opcode = 0
7	MESSAGE LENGTH		8	Message Length = 0

Write N Scattered Registers

This instruction writes to individual registers at various non-contiguous locations in the Data Register Table. The output write protect function must be disabled to execute this instruction.

Instruction Format:

BYTE				
5	STX	OPCODE	6	Opcode = 26
7	MESSAGE LENGTH		8	Message Length = Variable
9	N		10	$1 \leq N \leq 64$
11	ADDRESS A		12	$4096 \leq$ Address $\leq M$
13	DATA A		14	Data at Address A
15	ADDRESS B		16	$4096 \leq$ Address $\leq M$
17	DATA B		18	Data at Address B
				Data = Contents (0 - 65535)

Response Format (Instruction Executed):

5	STX	OPCODE	6	Opcode = 0
7	MESSAGE LENGTH		8	Message Length = 0

PULL N I/O Registers

This instruction is used for carrying N contiguous 16-bit words of data from intelligent I/O modules. The communication port reads data from the I/O module ascending from the starting address. The instruction is only functional with the 620-11/14/16 Control Processor Module (CPM) in the RUN/PROGRAM or DISABLE mode. The PULL instruction can only be used with intelligent I/O modules. Consult the 620 System Specifications Manual, Form No. 620-8995, for information on I/O modules that support the PULL instruction.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 28
	7	MESSAGE LENGTH		8	Message Length = 4
	9	N		10	$1 \leq N \leq 128$
	11	STARTING ADDRESS		12	$0 \leq$ Starting Address $\leq L$

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = variable
	9	DATA		10	Data at Starting Address
	11	DATA		12	Data at Starting Address + 1

Data = Contents (0 - 65535)

PUSH N I/O Registers

This instruction writes N contiguous 16-bit words to intelligent I/O modules. The communication port writes data to the I/O module ascending from the starting address. The instruction is only functional with the 620-11/14/16 CPM in the RUN/PROGRAM mode. The output write protect function must be disabled to execute this instruction. The PUSH instructions can only be used with intelligent I/O modules. Consult the 620 System Specification Manual, Form No. 620-8995, for more information on I/O modules that support the PUSH instruction.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 30
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 128$
	11	STARTING ADDRESS		12	$0 \leq$ Starting Address $\leq L$
	13	DATA		14	Data at Starting Address
	15	DATA		16	Data at Starting Address + 1

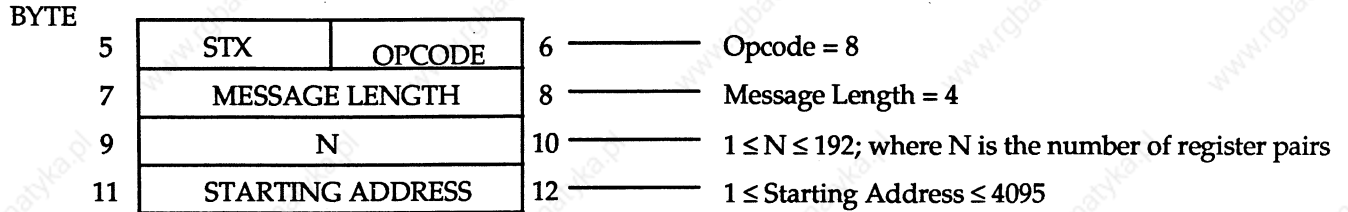Data = Contents (0 - 65535)

Response Format (Instruction Executed):

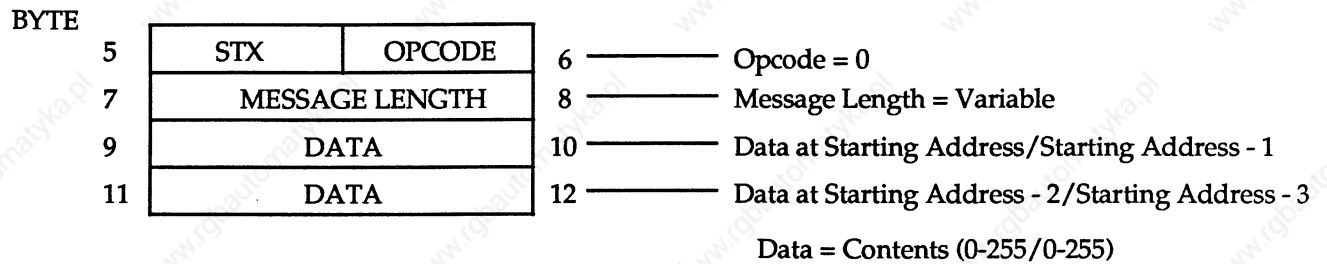| BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0

Read N System Status Registers

This instruction gathers system identification, status and diagnostic information from the 620-11/14/16 CPM. The registers are read in pairs to satisfy the word format and are read from the most significant address of the desired memory block. The 8-bit registers are read into 16-bit words downward from the starting address.

Instruction Format:

Note: Starting address is the most significant address of the system status registers.

BYTE

5	STX	OPCODE	6 ———— Opcode = 8
7	MESSAGE LENGTH		8 ———— Message Length = 4
9	N		10 ———— $1 \leq N \leq 192$; where N is the number of register pairs
11	STARTING ADDRESS		12 ———— $1 \leq$ Starting Address ≤ 4095

Response Format (Instruction Executed):

BYTE

5	STX	OPCODE	6 ———— Opcode = 0
7	MESSAGE LENGTH		8 ———— Message Length = Variable
9	DATA		10 ———— Data at Starting Address/Starting Address - 1
11	DATA		12 ———— Data at Starting Address - 2/Starting Address - 3

Data = Contents (0-255/0-255)

Write N System Status Registers

This instruction allows the user to write N contiguous, 8-bit System Status Table Registers starting at the specified address and working downward. The command can be executed in any Logic Controller System mode. The memory write protect function must be disabled.

Instruction Format:

Note: Starting address is the most significant address of the system status registers.

BYTE

5	STX	OPCODE	6 ——Opcode = 10
7	MESSAGE LENGTH		8 ——Message Length = Variable
9	N		10 ——$1 \leq N \leq 256$, where N is the No. of 8-bit registers
11	STARTING ADDRESS		12 ——$0 \leq$ Starting Address ≤ 4095
13	START DATA	DATA	14 ——Data at Starting Address/Starting Address -1
			Data = Contents (0-255)
	DATA	LAST DATA	12 + N (268 max.)
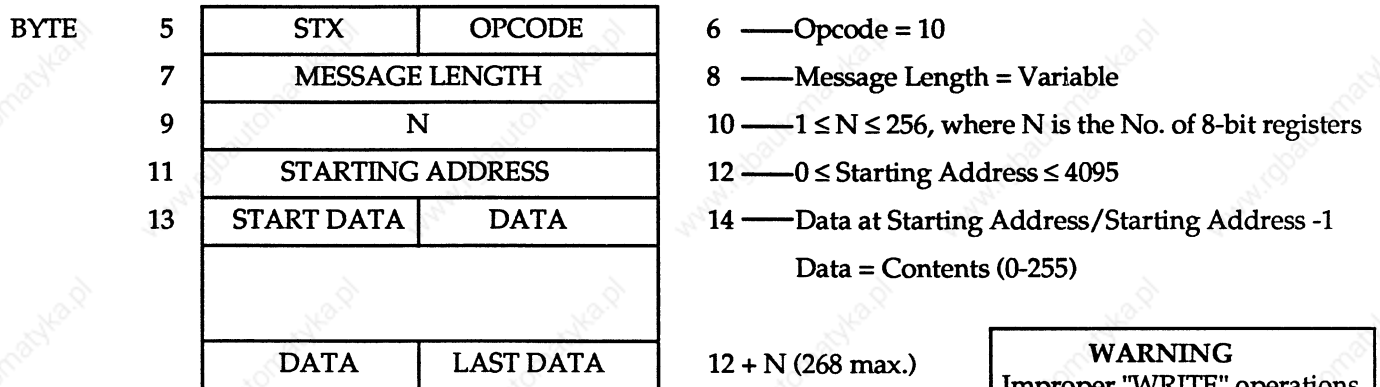
> **WARNING**
> Improper "WRITE" operations to the System Status Table may cause machine failure. Refer to Appendix II of this manual.

Response Format (Instruction Executed):

BYTE

| 5 | STX | OPCODE | 6 ———— Opcode = 0 |
| 7 | MESSAGE LENGTH | | 8 ———— Message Length = 0 |
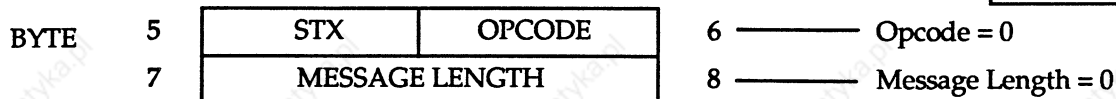
PROCESSOR CONTROL INSTRUCTIONS

These instructions place the 620-11/14/16 CPM into and remove it from the PROGRAM mode. They are used with instructions that require such a processor mode change. These instructions also include commands to configure the CPM. For specific configuration procedures, refer to Appendix II of this manual.

Request PROGRAM Mode

This instruction requests software PROGRAM mode control for the communication port. This request must be granted by the 620-11/14/16 Control Processor Module (CPM) before the communication port accepts some program memory instructions. When multiple requests are pending, the CPM grants in order of rank. The 623-6100/6150 Loader/Terminal (or 623-60 MS-DOS Loader) is given highest priority and option modules follow in order from lowest to highest card address. The communication port follows after the Loader/Terminal and any option modules in the CPM's hierarchy for granting software PROGRAM mode control. Once a request is submitted, it must be removed by the host computer when no longer needed.

Instruction Format:

BYTE	5	STX	OPCODE	6 ———— Opcode = 52
	7	MESSAGE LENGTH		8 ———— Message Length = 0

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6 ———— Opcode = 0
	7	MESSAGE LENGTH		8 ———— Message Length = 2
	9	RESULT DATA		10 ———— Result Data:

    1 = Request Granted
    2 = Request Pending

Remove PROGRAM Mode Request

This instruction removes the software PROGRAM mode request. If no other PROGRAM mode requests are pending, the 620 CPM returns to the mode specified by the processor keyswitch.

Instruction Format:

BYTE	5	STX	OPCODE	6 ———— Opcode = 54
	7	MESSAGE LENGTH		8 ———— Message Length = 0

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6 ———— Opcode = 0 (Execution Acknowledge = 0)
	7	MESSAGE LENGTH		8 ———— Message Length = 0

Write I/O Configuration

This instruction allows the user to configure the I/O module slots in the 620-11/14/16 Logic Controller System for 0, 8, 16, or 32-point operation and for local/serial operation. Remember, only the 620-16 CPM supports Serial I/O. The command writes N contiguous bytes of packed slot configuration data (2 slots/byte) to the System Status Table starting at the specified slot number and working upward. The starting slot number must be an even number. The command will be executed in any LCS mode. The memory write protect function must be disabled.

Instruction Format:

BYTE					
5	STX	OPCODE	6	——	Opcode = 76
7	MESSAGE LENGTH		8	——	Message Length = Variable
9	N		10	——	$1 \leq N \leq 138$, where N is No. of slot pairs
11	STARTING SLOT NO.		12	——	$0 \leq$ Slot No. ≤ 274
13	START DATA	DATA	14		
	DATA	LAST DATA	12 + N (150 max.)		

Slot-Pair Definition:

```
      7            4  3            0
  +------------------+------------------+
  |  CARD SLOT X + 1 |   CARD SLOT X    |
  +------------------+------------------+
```

Bits 7/3 = Local/Serial: 0 = Local I/O; 1 = Serial I/O

Bits 6,5,4/2,1,0 = No. I/O Points: 000 = 0
001 = 8
010 = 16
011 = 32
111 = SLM*   * SLM is valid in slot 7 only and must be designated "local" I/O

Response Format (Instruction Executed):

BYTE					
5	STX	OPCODE	6	——	Opcode = 0
7	MESSAGE LENGTH		8	——	Message Length = 0

Write Processor Control Configuration

This command allows the user to configure the I/O and Mode Control functions for the 620-11/14/16 Logic Controller System. The instruction will be executed in any LCS mode. The memory write protect function must be disabled.

Instruction Format:

```
BYTE  5 |   STX   |  OPCODE  |  6 —— Opcode = 78
      7 |   MESSAGE LENGTH   |  8 —— Message Length = 2
      9 |    0    |   DATA   |  10
```

Logic Controller Control Data Definition:

```
   7      6      5      4      3      2      1      0
|      |      | Scan | Data | Low  | Out  | Force| Armp |
|      |      | Loss | Chng | Batt | Stat |      |      |
```

Bits 7,6 = Not Used: 00
Bit   5 = Scan Loss Timer: 0 = disabled; 1 = enabled
Bit   4 = Data Change Function: 0 = disabled; 1 = enabled
Bit   3 = Scan with Low Battery: 0 = disabled; 1 = enabled
Bit   2 = Output Status in Program/Disable Modes: 0 = Freeze; 1 = Clear
Bit   1 = Force Function: 0 = disabled; 1 = enabled
Bit   0 = Run Mode Programming: 0 = disabled; 1 = enabled

Response Format (Instruction Executed):

```
BYTE  5 |   STX   |  OPCODE  |  6 —— Opcode = 0
      7 |   MESSAGE LENGTH   |  8 —— Message Length = 0
```

PROGRAM MEMORY INSTRUCTIONS

Program Memory instructions manipulate program memory. (See Opcode listing in Table 13).

Upload N Program Memory Words

This instruction uploads program memory. The instruction carries a maximum of 150 of the 24-bit memory words and packs each into two 16-bit data words. This instruction is executed with the CPM in any mode.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 34
	7	MESSAGE LENGTH		8	Message Length = 4
	9	N		10	$1 \leq N \leq 150$
	11	STARTING ADDRESS		12	$0 \leq$ Starting Address $\leq M$

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	0	OPCODE	10	
	11	ADDRESS		12	} 24-Bit Memory Word at the Starting Address
	13	0	OPCODE	14	
	15	ADDRESS		16	} 24-Bit Memory Word at the Starting Address +1

Download N Program Memory Words

This instruction downloads program memory. The instruction writes up to 150 of the 24-bit words, each extracted from two packed, 16-bit data words.

With the CPM in the RUN/PROGRAM or DISABLE mode, this instruction can be executed without a software PROGRAM mode request. However, an Invalid Processor Mode Error message will be generated if this command is received while an Augmented Run Mode Programming (ARMP) operation is in progress. With the CPM in the PROGRAM mode, this instruction is only accepted while the communication port has the CPM in the software PROGRAM mode. This is necessary to eliminate contention between multiple user memory programmers.

The CPM force count will be correctly maintained unless:

- The write data is at a higher address than, and is not contiguous with, the original program, or
- An End of Program (EOM) opcode is included in the write data such that the EOM is at an address lower than the original EOM or is not at the highest address of the write data.

The program memory write protect function must be disabled to execute this instruction.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 36
	7	MESSAGE LENGTH		8	Message Length = Variable
	9	N		10	$1 \leq N \leq 150$
	11	STARTING ADDRESS		12	$0 \leq$ Starting Address $\leq M$
	13	0	OPCODE	14	} 24-Bit Word for the Starting Address
	15	ADDRESS		16	
	17	0	OPCODE	18	} 24-Bit Word for the Starting Address +1
	19	ADDRESS		20	

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0
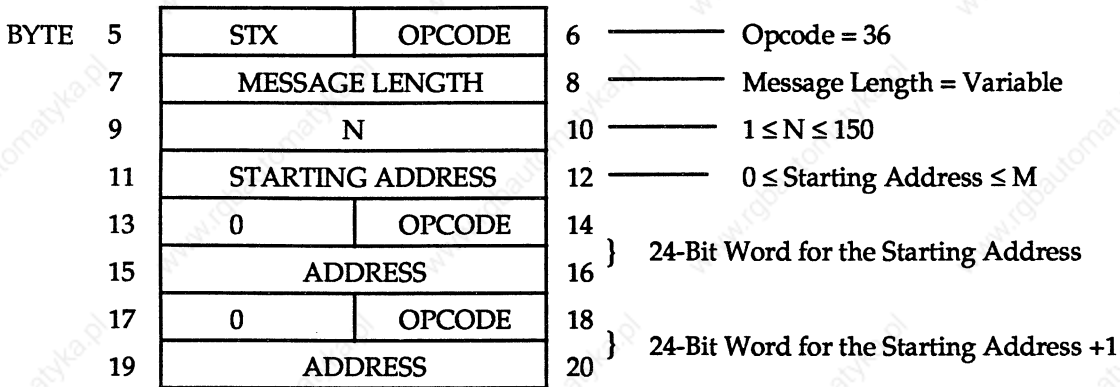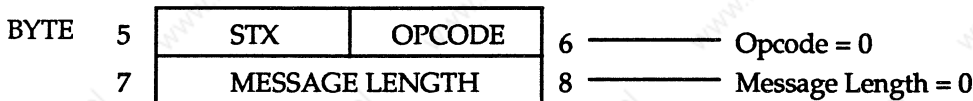
Clear Program Memory

This instruction erases the program memory, I/O status tables, Data Register tables, force count and I/O fault count. The instruction is accepted only while the communication port has the CPM in the software PROGRAM mode and the port's program memory write protect function is disabled.

Instruction Format:

BYTE 5	STX	OPCODE	6
7	MESSAGE LENGTH		8

Opcode = 38
Message Length = 0

Response Format (Instruction executed):

BYTE 5	STX	OPCODE	6
7	MESSAGE LENGTH		8

Opcode = 0
Message Length = 0
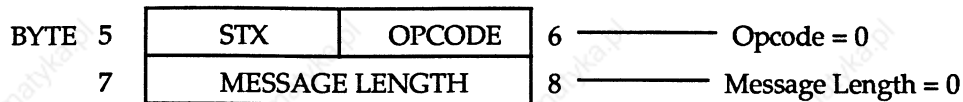
Insert N Program Memory Words

This instruction is used for editing existing program memory or writing a new program. The instruction inserts up to 150 of the 24-bit memory words by first shifting up the program memory N memory words then writing in the received words. The starting address points to the first word shifted up, therefore the insertion occurs in front of the starting address. If the processor memory is cleared, the insertion occurs before the End of Memory (EOM) opcode, therefore it is not necessary to insert an EOM opcode.

The instruction is accepted only while the communication port has the Control Processor Module (CPM) in the software PROGRAM mode. The force count will be correctly maintained unless an EOM opcode is included in the insert data. The port's program memory write protect function must be disabled.

Instruction Format:

BYTE 5	STX	OPCODE	6
7	MESSAGE LENGTH		8
9	N		10
11	STARTING ADDRESS		12
13	0	OPCODE	14
15	ADDRESS		16
17	0	OPCODE	18
19	ADDRESS		20

Opcode = 40
Message Length = Variable
$1 \leq N \leq 150$
$1 \leq$ Starting Address $\leq$ End of Program Address
} 24-Bit Word for the Starting Address
} 24-Bit Word for the Starting Address +1

Response Format (Instruction Executed):

BYTE 5	STX	OPCODE	6
7	MESSAGE LENGTH		8

Opcode = 0
Message Length = 0
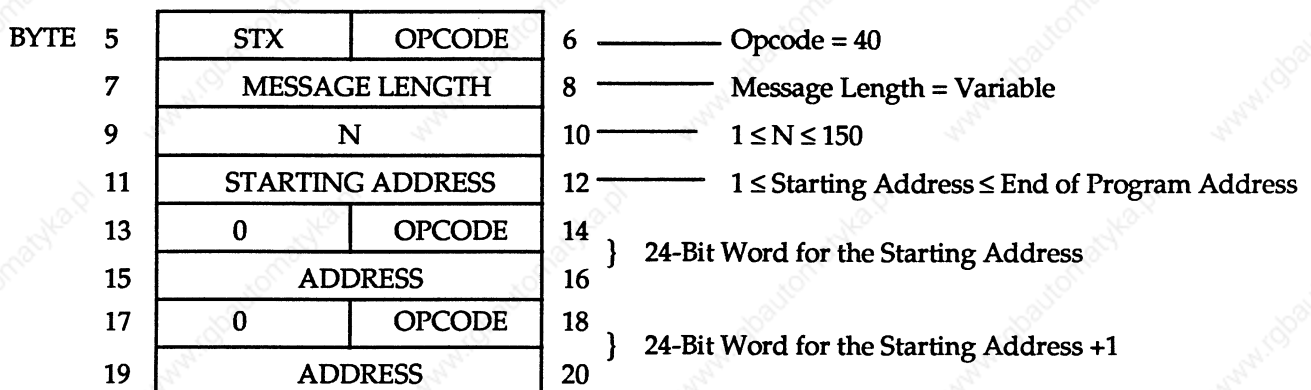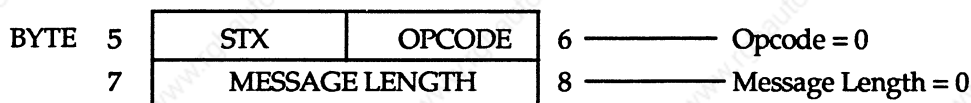
Delete N Program Memory Words

This instruction edits the program memory. The instruction deletes up to the full program memory starting with the word pointed to by the starting address. Any program memory remaining above the deleted block is then shifted to join any memory below the starting address. The force count is updated accordingly. This instruction is accepted only while the communication port has the CPM in the software PROGRAM mode. The port program memory write protect function must be disabled to execute this function.

Instruction Format:

BYTE	5	STX	OPCODE	6	Opcode = 42
	7	MESSAGE LENGTH		8	Message Length = 4
	9	N		10	$1 \leq N \leq 32764$
	11	STARTING ADDRESS		12	$1 \leq$ Starting Address $\leq$ End of Program Address - 1

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0

PROGRAM HEADER INSTRUCTIONS

Program header instructions upload and download program header information. These instructions must be encoded in ASCII. See ASCII conversions in Table 21 in Appendix II of this manual.

Upload Program Date

This instruction uploads the program date information from registers in the System Status Table. The instruction is executed with the 620-11/14/16 Logic Controller in any mode.

Instruction Format:

BYTE 5	STX	OPCODE	6 ———— Opcode = 64
7	MESSAGE LENGTH		8 ———— Message Length = 0

Response Format (Instruction Executed):

Note: The month, day, and year numbers are encoded in ASCII. The data is retrieved from these locations.

CHARACTER	STATUS REGISTER ADDRESS	CHARACTER	STATUS REGISTER ADDRESS
Month,10's	2175	Day, units	2172
Month, units	2174	Year, 10's	2171
Day, 10's	2173	Year, units	2170

BYTE 5	STX	OPCODE	6 ———— Opcode = 0
7	MESSAGE LENGTH		8 ———— Message Length = 6
9	MO - 10's	MO - UNITS	10
11	DAY - 10'S	DAY - UNITS	12
13	YR - 10'S	YR - UNITS	14

Upload Programmer

This instruction reads the programmer information registers in the System Status Table. The instruction is executed with the Logic Controller in any mode.

Instruction Format:

BYTE 5	STX	OPCODE	6 ———— Opcode = 66
7	MESSAGE LENGTH		8 ———— Message Length = 0

Response Format (Instruction Executed):

Note: Data is encoded in ASCII. It is retrieved from the System Status Table from address 2169 (byte 9) to 2144 (byte 34). Byte 9 contains the first byte of programmer information.

BYTE 5	STX	OPCODE	6 ———— Opcode = 0 (Execution Acknowledge)
7	MESSAGE LENGTH		8 ———— Message Length = 26
9	DATA	DATA	10
11	DATA	DATA	12
31	DATA	DATA	32
33	DATA	DATA	34

Upload Title

This instruction reads the program title information from System Status Registers. The instruction is executed with the CPM in any mode.

Instruction Format:

BYTE 5	STX	OPCODE	6 ——————— Opcode = 68
7	MESSAGE LENGTH		8 ——————— Message Length = 0

Response Format (Instruction Executed):

Note: Data is encoded in ASCII. It is retrieved from System Status Table Addresses from 2143 (byte 9) to 2048 (byte 104). Byte 9 contains the first byte of title information.

BYTE 5	STX	OPCODE	6 ——————— Opcode = 0
7	MESSAGE LENGTH		8 ——————— Message Length = 96
9	DATA	DATA	10
11	DATA	DATA	12
	DATA	DATA	
101	DATA	DATA	102
103	DATA	DATA	104

Download Program Date

This instruction writes program date information into System Status Table registers. The instruction is accepted only while the port has the CPM in the software PROGRAM mode. The program memory write protect function must be disabled.

Instruction Format:

Note: The data must be encoded in ASCII

BYTE 5	STX	OPCODE	6 ——————— Opcode = 70
7	MESSAGE LENGTH		8 ——————— Message Length = 6
9	MO - 10'S	MO -UNITS	10
11	DAY - 10'S	DAY - UNITS	12
13	YR - 10'S	YR - UNITS	14

Response Format (Instruction Executed):

BYTE 5	STX	OPCODE	6 ——————— Opcode = 0
7	MESSAGE LENGTH		8 ——————— Message Length =0

Download Programmer

This instruction writes programmer information into System Status Table registers. The instruction is executed only when the port has placed the CPM in the software PROGRAM mode. The program memory write protect function must be disabled to execute this instruction.

Instruction Format:

Note: Data must be encoded in ASCII. The first character of the statement is located in byte 9. Unused bytes should be filled with space characters (ASCII 20).

BYTE	5	STX	OPCODE	6	Opcode = 72
	7	MESSAGE LENGTH		8	Message Length = 26
	9	DATA	DATA	10	
	11	DATA	DATA	12	
	31	DATA	DATA	32	
	33	DATA	DATA	34	

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0 (Execution Acknowledge)
	7	MESSAGE LENGTH		8	Message Length = 0
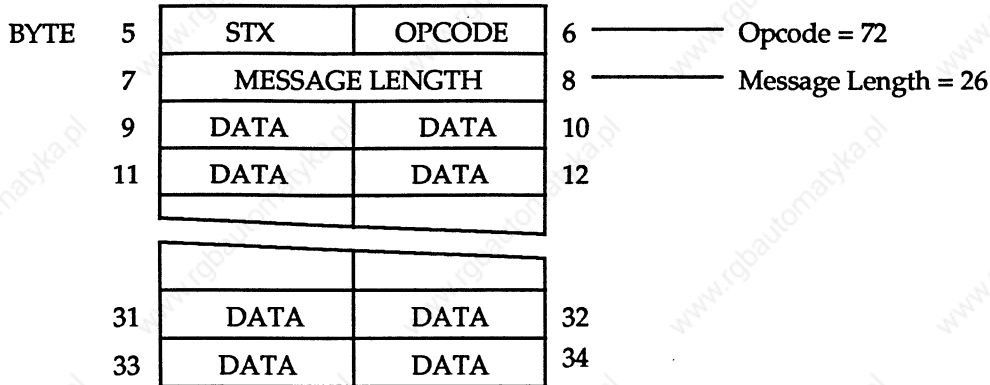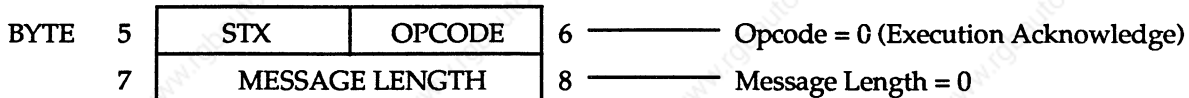
Download Title

This instruction downloads program title information in the System Status Table registers. The instruction is executed only when the communication port has placed the Logic Controller in the software PROGRAM mode. The program memory write protect function must be disabled to execute this instruction.

Instruction Format:

Note: Data must encoded in ASCII. The first character of the statement is located in byte 9. Unused bytes should be loaded with a space character (ASCII 20).
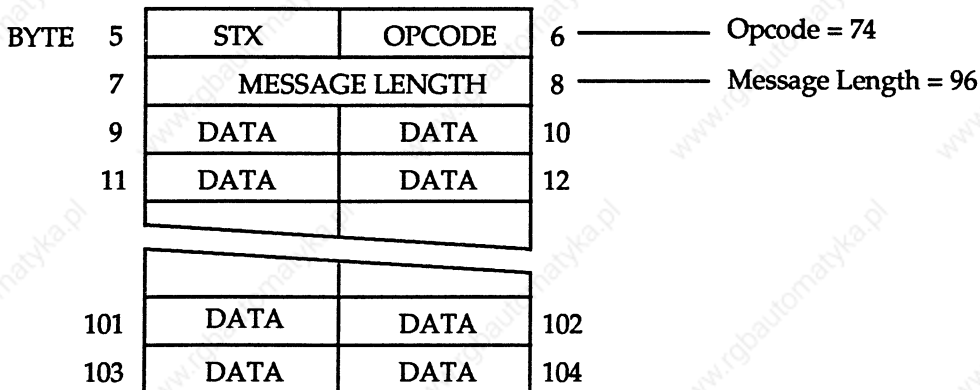
BYTE	5	STX	OPCODE	6	Opcode = 74
	7	MESSAGE LENGTH		8	Message Length = 96
	9	DATA	DATA	10	
	11	DATA	DATA	12	
	101	DATA	DATA	102	
	103	DATA	DATA	104	

Response Format (Instruction Executed):

BYTE	5	STX	OPCODE	6	Opcode = 0
	7	MESSAGE LENGTH		8	Message Length = 0
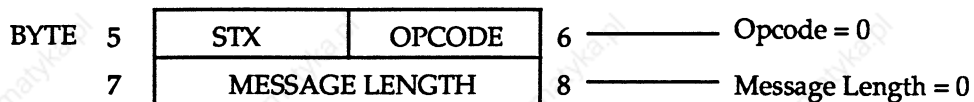
DIAGNOSTIC INSTRUCTIONS

These instructions obtain communication port and Logic Controller status information and ensure that the physical data link between host and port is functioning properly.

Read Port Status

This instruction is a diagnostic tool for the host computer. It obtains port and processor status information and provides a tabulation of message exchanges that have occurred since port power initialization or since the last Read Port Status instruction. Message exchange counters are reset as a result of the Read Port Status instruction.

Instruction Format:

BYTE 5	STX	OPCODE	6 ———— Opcode = 0
7	MESSAGE LENGTH		8 ———— Message Length = 0

Response Format (Instruction Executed): *(See the note below for further explanation of this format)

BYTE	5	STX	OPCODE	6 ———— Opcode = 0
	7	MESSAGE LENGTH		8 ———— Message Length = 14
	9	DCM REVIS.	CARD ADDR.	10
	11	PROC. MODEL	PROC. REVIS.	12
	13	PROC INTR.	PROC MODE	14
	15	RCVD MSG COUNT		16
	17	XMTD MSG COUNT		18
	19	RCVR ERROR COUNT		20
	21	INVALID MSG COUNT		22

Note :

DCM Revision - There is no applicable revision level for the communication port. The response defaults to 255 in this byte.

Card Address - There is no applicable card address. The response defaults to 255 in this byte.

Logic Controller System Model - The port will respond with a BCD value in this byte that directly denotes the LCS model number (e.g., 16 = 620-16).

Logic Controller Revision - Extracted from the processor revision byte in the processor System Status Table.

Logic Controller Interface - There is no applicable LCS interface. The response always contains a 1 (interface functional) in this byte.

LCS Mode - A representation of the general state of the LCS:

> 0 = PROGRAM Mode
> 1 = RUN/PROGRAM Mode (also
>   DISABLE)

Received Message Counter - A 16-bit binary count of the number of messages received successfully since the last Read Port Status instruction or since LCS power initialization.

Transmitted Message Counter - A 16-bit binary count of the number of messages transmitted by the port since power initialization or since the last Read Port Status instruction.

Receiver Error Count - A 16-bit binary count of the number of receiver errors, which may be checksum errors or message header errors. This count can only be incremented if an SOH followed by a valid nodal address has first been received. The counter is reset at power initialization or following the formulation of a Read Port Status response. Message aborts are not counted as receiver errors.

Invalid Message Counter - A 16-bit binary count of the number of messages received which were found to contain invalid opcodes, control characters, and modifiers. The counter is reset at power initialization or following the formulation of a Read Port Status response.

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Loop Back Test

This instruction is a diagnostic tool for the host computer. It echoes a test message sent by the host that aids in data link diagnostics. If the port does not receive the proper host data, an invalid test data response is sent.

Instruction Format:

BYTE	5	STX	OPCODE	6 ——————— Opcode = 80
	7	MESSAGE LENGTH		8 ——————— Message Length = 4
	9	0	85	10 ——————— Test Data Transmitted
	11	170	255	12 ——————— Test Data Transmitted

Response Format (Instruction Received, Data Verified):

BYTE	5	STX	OPCODE	6 ——————— Opcode = 0
	7	MESSAGE LENGTH		8 ——————— Message Length = 4
	9	0	85	10 ——————— Test Data Received
	11	170	255	12 ——————— Test Data Received

Modify Write Protect

This command allows the user to enable or disable the Memory Write Protect and the Output Write Protect functions for the communication port. The instruction will be executed in any LCS mode.

Instruction Format:

BYTE	5	STX	OPCODE	6 ——————— Opcode = 0
	7	MESSAGE LENGTH		8 ——————— Message Length = 2
	9	0	DATA	10

WRITE PROTECT DATA DEFINITION:

7	6	5	4	3	2	1	0
						Mem. Protect	Out. Protect

Bits 7, 6, 5, 4, 3, 2, = Not used = 000000

Bit 1 = Memory Protect: 0 = protected; 1 = write enabled
Bit 0 = Outputs Protect: 0 = protected; 1 = write enabled

Response Format (Instruction Executed):

| BYTE | 5 | STX | OPCODE | 6 ——————— Opcode = 0 |
| | 7 | MESSAGE LENGTH | | 8 ——————— Message Length = 0 |

FLAG MODE OPERATION RESPONSE

This response is generated if an OFF to ON change has occurred. Various methods of energizing flag outputs are available to the Logic Controller programmer. The flag outputs in the 620-11/14/16 program memory should be latch outputs to ensure that all flag responses are transmitted to the host. The host's application program should reset these latch outputs by turning them OFF, indicating it has received the flag response.

The block of flag bits may reside anywhere in the real or control I/O address space. The communication port monitors address 2016 through 2031 for OFF to ON transitions unless the user has programmed a different Most Significant Flag Address in System Status Table locations 2501-2502. The Auxiliary Menu (F12) on the Loader/ Terminal also monitors address 2016 through 2031.

Flag responses are generated automatically when a transition occurs. The flag bits are read at every CPM Memory Word Zero (MWZ) if the flag mode is enabled and the communication port is not receiving a message or servicing a command. Flag bits are packed into a 16-bit data word. The least significant bit of the data is the status of the least significant flag address.

The flag mode response function must be enabled and the point-to-point serial port configuration must be selected to execute this function. The control character for a Flag Response is 132.

Response Format:

BYTE	5	STX	OPCODE	6	———	Opcode = 0
	7	MESSAGE LENGTH		8	———	Message Length = 2
	9	FLAG BITS		10		

ERROR MESSAGES

A response occurs in most host/communication port exchanges. This response can be either an acknowledge or an error message. Table 16 lists error messages and their opcodes. Descriptions of the error messages and conditions under which they are generated follow.

Invalid Opcode

This response occurs when the port receives an opcode for which it has no service routine. The invalid opcode is returned in the least significant byte (byte 10) of a data word included with the message.

Response Format (Error Message):

BYTE	5	STX	OPCODE	6 ———— Opcode = 1
	7	MESSAGE LENGTH		8 ———— Message Length = 2
	9	0	OPCODE	10 ———— Status: 0 = Off
				1 = On

TABLE 16 - ABC ERROR MESSAGES AND OPCODES

OPCODE	ERROR MESSAGE
1	Invalid Opcode
2	N Value Exceeds System Limits
3	Starting Address Exceeds Memory Limits
4	Memory Block Exceeds Memory Limits
5	Invalid Processor Mode
6	User Memory Not Alterable (ROM)
7	Write Protect Enabled
80	Invalid Test Data

N Value Exceeds System Limit

This response indicates that the N value in the instruction exceeds the system limits. The invalid N value as well as the instruction opcode are returned with the message. The starting address is included for error message consistency.

Response Format (Error Message):

BYTE 5	STX	OPCODE	6	Opcode = 2
7	MESSAGE LENGTH		8	Message Length = 6
9	0	OPCODE	10	
11	N		12	
13	STARTING ADDRESS		14	

Starting Address Out Of Memory Limits

This response indicates that the starting address value in the instruction exceeds the system limits. The invalid starting address, N value, and opcode are returned with the error message.

Response Format (Error Message):

BYTE 5	STX	OPCODE	6	Opcode = 3
7	MESSAGE LENGTH		8	Message Length = 6
9	0	OPCODE	10	
11	N		12	
13	STARTING ADDRESS		14	

Memory Block Exceeds Memory Limit

The starting address and N value define a block of memory for the instruction opcode. This response indicates that the defined memory block does not fall within the bounds of the 620-11/14/16 CPM memory. There are situations with most instructions in which the N value and starting address are valid, but the memory block they define is not. The error opcode, the instruction opcode, the N value, and the starting address are returned.

Response Format (Error Message):

BYTE 5	STX	OPCODE	6	Opcode = 4
7	MESSAGE LENGTH		8	Message Length = 6
9	0	OPCODE	10	
11	N		12	
13	STARTING ADDRESS		14	

Invalid Processor Mode

This response occurs when the mode check fails prior to instruction execution. The response applies only to program memory, program header, System Status Table, and PUSH/PULL instructions.

Response Format (Error Message):

| BYTE 5 | STX | OPCODE | 6 ——— Opcode = 5 |
| 7 | MESSAGE LENGTH | | 8 ——— Message Length = 0 |
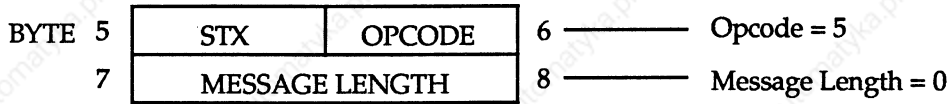
Program Memory Not Alterable

This response occurs with instructions that attempt to write to Program Memory when that memory is situated in ROM.

Response format (Error Message):

| BYTE 5 | STX | OPCODE | 6 ——— Opcode = 6 |
| 7 | MESSAGE LENGTH | | 8 ——— Message Length = 0 |
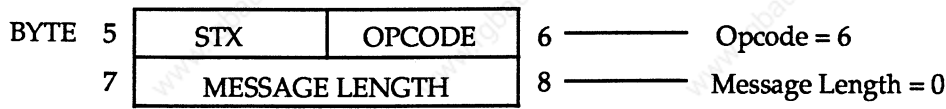
Write Protect Enabled

This response occurs with write instructions that are directed to a data resource which has its write protect function enabled.

Response Format (Error Message):

| BYTE 5 | STX | OPCODE | 6 ——— Opcode = 7 |
| 7 | MESSAGE LENGTH | | 8 ——— Message Length = 0 |
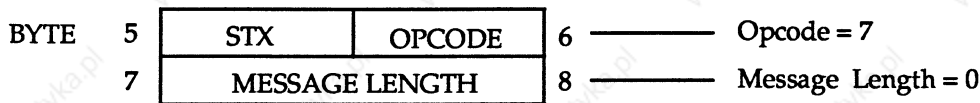
Invalid Loop Back Test

This response occurs if an error has occurred in the Loop Back Test. The faulty bit pattern received is returned in the message.

Response Format (Error Message):

BYTE 5	STX	OPCODE	6 ——— Opcode = 80
7	MESSAGE LENGTH		8 ——— Message Length = 4
9	FAULTY TEST PATTERN		10
11	FAULTY TEST PATTERN		12
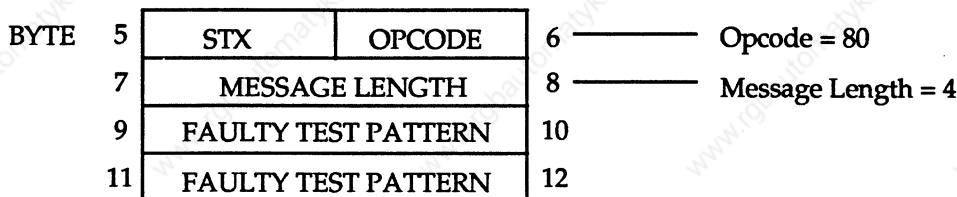
MODBUS RTU PROTOCOL

When configured for the MODBUS RTU protocol, the 620-11/14/16 Communication Port offers a specialized communication interface feature to its resident Control Processor Module (CPM). It serves as an interface between the 620-11/14/16 LCS and a Modicon MODBUS compatible communication network.

The communication port's instruction set is a subset of commands used with the Modicon MODBUS RTU protocol.

The 620-11/14/16 LCS's input/output status and register contents may be examined or modified through the communication port interface. Diagnostic instructions also are incorporated.

GENERAL OPERATION

When the communication port requests it, the 620-11/14/16 CPM gives the interface a slot at the beginning of the program scan. The communication port is synchronized to LCS scan and is partially dependent on Logic Controller System scan for its response time to received commands.

During the given time slot, the communication interface has access to the LCS's I/O status and register contents.

NOTE
Use of the communication port will increase scan times of the 620-11/14/16 Logic Controller by as much as 18 percent (in transmit and receive interrupts only). MWZ windows may add more time; maximum time for any given window in RUN MODE is 10.5ms.

Table 17 shows the memory areas compatible with read and write instructions in each LCS mode.

Legal ranges for command parameters are:

- Real I/O: 0-255 for the 620-11
  0-639 for the 620-14
  0-2039 for the 620-16

- Control I/O 0-4095 for 620-11/14/16

- Registers 4096-8191 for 620-11/14/16

DATA LINK CONTROL

In MODBUS RTU operation, the communication port uses asynchronous transmission. The messages are delimited by an idle link condition, so the gap between any two characters of a message must be limited to less than three character times (less than 1.5ms at 19.2K baud) or end of message is assumed.

EXCHANGE PROCEDURES

The link operates in a half duplex mode with the host initiating all message exchange sessions. The procedure includes these steps:

1. The host sends the command to the communication port.

2. The host starts a failsafe timer while the 620-11/14/16's communication port executes the command and prepares a response.

3. The communication port returns a response to the host.

EXCHANGE PROCEDURE EXCEPTION CONDITIONS

1. Command Message CRC Error - The communication port does not respond since the error could be the station address portion of the message. The host must recover through its response failsafe timer.

NOTE
The 620-11/14/16's communication port will not recognize broadcast commands (Nodal Address 0) and, therefore, will not respond.

2. Command Function Code or Function Code Modifier Error - The communication port qualifies these values before executing a command. An error response results.

3. LCS Mode - Certain commands require the LCS to be in the RUN/PROGRAM mode state or else a "reject" response results.

4. Response Error - If the host finds a response faulty, the host retransmits the command and the communication port executes it again.

5. Receiver Overflow - The Port Receive buffer holds 260 bytes. Any message that exceeds the buffer size is rejected. There is no response.

COMMUNICATION INTERFACE LIMITATIONS

The communication port will service only one command at a time. It will not accept new instructions until the response in progress is completed.

SESSION EXECUTION TIME

Total exchange time is the sum of the times required by the operations listed in Table 17. This time frame extends from the host computer's decision to acquire certain information until the data is in the computer's data base.

- **Command Preparation and Response Processing** - Time for these operations is a function of the host computer.

- **Command/Response Transmission and Reception** - Time for these operations is a function of the baud rate and message size according to the following formula:

  Transmission Time =

  (1/baud rate) x (1000ms/sec.)
  x (bits/character) x (no. of characters)

- **Command Processing/Response Preparation** - Time for these operations varies slightly with each instruction.

- **LCS Scan Synchronization** - This is the time that elapses while the communication port waits for its window at Memory Word Zero (MWZ). The time is less than 2ms if the LCS is in PROGRAM mode or potentially equal to LCS scan time if the LCS is in RUN/PROGRAM mode.

- **LCS Irregular Overhead** - This time is the result of external events, such as Communication Interface Modules (CIM's), the Loader/Terminal, or the Processor Keyswitch that extend time between communication port access windows. The Loader/Terminal can add as much as 125ms to a scan and each CIM can add up to 90ms. If the LCS is switched from PROGRAM to RUN/PROGRAM mode, the 620-11/14/16 built-in communication port is denied access during LCS diagnostics, which requires approximately 725ms.

- **Command Execution** - This is the time required by the communication port to execute the exchange once it receives a window at MWZ.

TABLE 17 - MODBUS RTU OPERATIONS IN SESSION EXECUTION TIMES

COMPUTER OPERATIONS	620-11/14/16 COMMUNICATION INTERFACE OPERATIONS
Command Preparation Command Transmission ⟶	Command Reception *Command Processing LCS Scan Synchronizations LCS Irregular Overhead *Command Execution *Response Preparation Response Transmission
Response Reception ⟵ Response Processing	
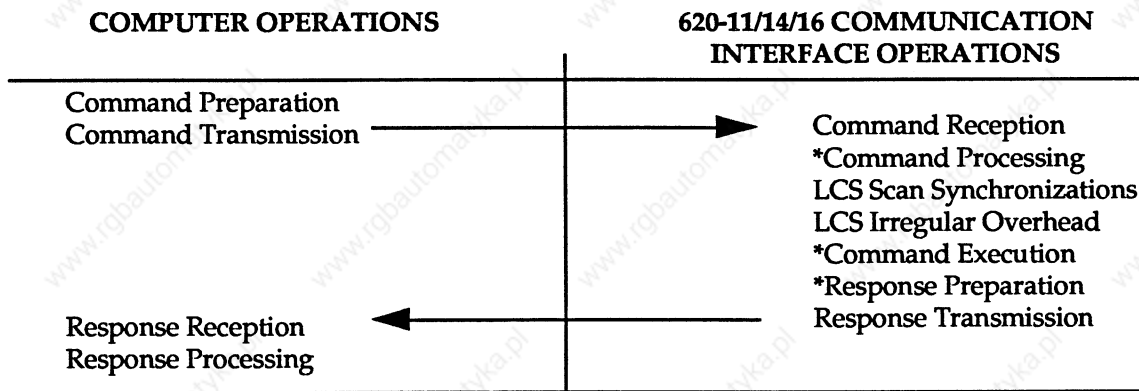
*These operations are performed during time slots granted by the Control Processor Module.

SESSION EXECUTION AND LCS EXCHANGE PROCEDURES

Since the 620-11/14/16 built-in Communication Port is not an independent processor, much of the session execution processing that a CIM would perform must be done directly by the LCS. This will result in slightly increased scan times for 620-11/14/16 Logic Controllers performing communication tasks.

With a CIM, the only effect of a communication session on an LCS was the "window" granted to the CIM for accessing the LCS data base. With the communication port, however, the LCS's scan <u>must be increased</u> to accommodate receive and transmit interrupt service, command processing, and response generation.

Multiple-Window Exchange

In order to keep scan-time increase at a minimum, the 620-11/14/16 Communication Port will service a communication session over a series of LCS scans. This is called a multiple-window exchange and it applies to most instructions.

In a typical communication port exchange, three LCS scans will be required to service a communication session (see Figure 32).

Example:

- The Command Processing operation will perform message decoding/validation at Memory Word Zero (MWZ) on one scan;
- The Command Execution operation will access the LCS database at MWZ on the next scan;
- The Response Preparation operation will occur at MWZ on yet another successive LCS scan.

Single-Window Exchange

For diagnostic instructions, the communication port will execute the command at the first MWZ slot granted by the CPM scan. These instructions are:

- 08 Loop Back Test
- 12 Report Communication Event Log

Also, error detections will result in an immediate single-window execution.

NOTE
Equations listed in Table 21 (Instruction Execution Times) determine the total time required within the MWZ time slot(s) for Command Processing, Command Execution, and Response Preparation operations.

TABLE 18 - MODBUS RTU COMMUNICATION INTERFACE ACCESS DURING LCS SCANS

LCS SCAN	PROGRAM		DISABLE		RUN/PROGRAM	
	Read	Write	Read	Write	Read	Write
I/O Status	X	X	X	X	X	X
I/O Registers			X		X	X
Real Outputs						X
Internal Responses	X	X	X	X	X	X

MULTIPLE-WINDOW
EXCHANGE
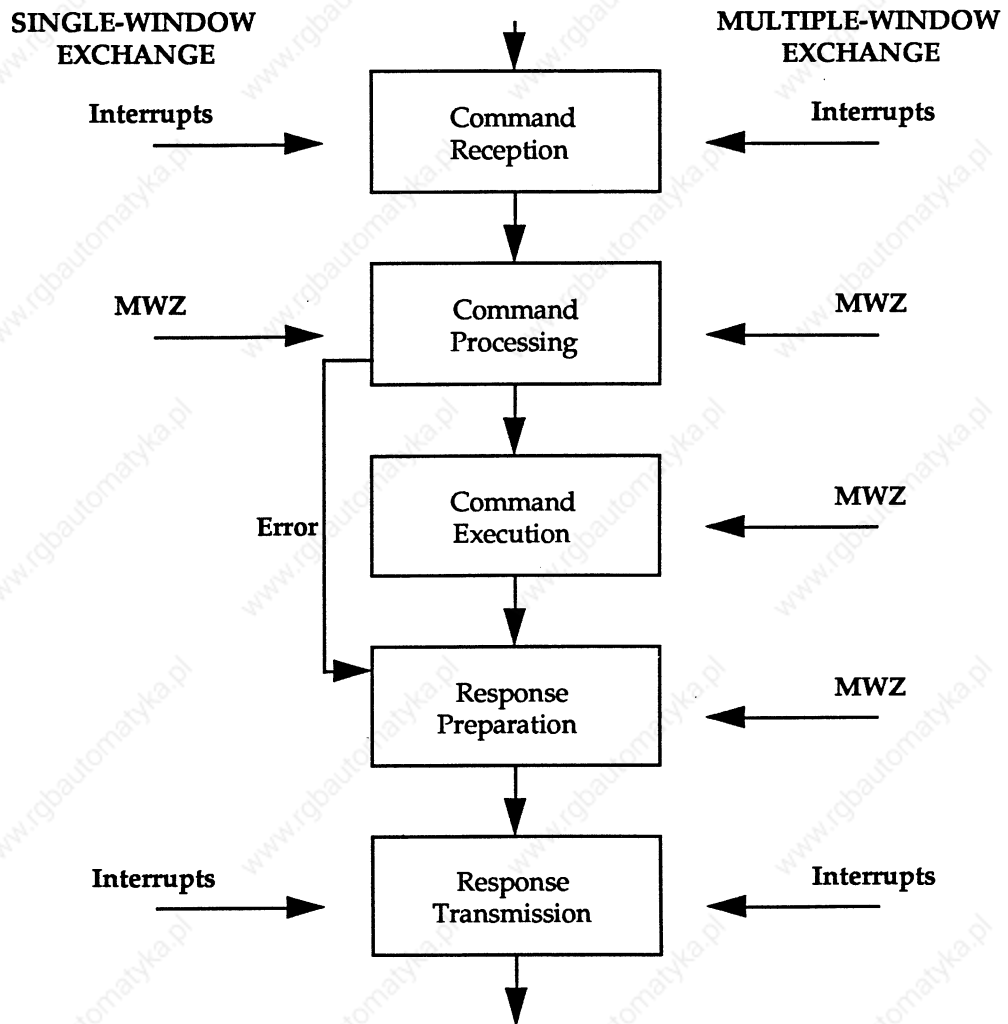
FIGURE 32 - MODBUS RTU DATA EXCHANGE PROCEDURE DIAGRAM

EVENT COUNTER

An event counter maintains a record of exchanges successfully completed between the communication port and the Logic Controller System's database. The counter is cleared at power-up and incremented with each successful execution of any Read I/O, Read Register, Read Input Register, Modify Coil, or Modify Output Register instruction. The 16-bit counter wraps around after 65,535 is reached.

The host retrieves the count by using the Report Communication Event Log Instruction. Error recovery procedures are enhanced if the host maintains a duplicate count. This allows the host computer to determine how many messages have been received by the port, and if messages should be retransmitted.

EVENT COUNTER STATUS WORD

The Event Counter Status Word is a 16-bit word. When set to -1, it indicates an execution exchange between the communication port and the 620-11/14/16 Logic Controller System. The host reads this word with the Read Communication Event Log instruction. The serial link is inactive while commands are serviced, so this word is always cleared when read by the host.

MESSAGE COUNTER

A 16-bit counter maintains a record of valid messages received by the communication port. This counter is cleared at power-up, and increments for each message received without nodal address, framing, parity, overrun or CRC errors. The host retrieves this count through a Report Communication Event Log instruction. The 16-bit counter wraps around after 65,535 is reached.

TRANSACTION RECORDS

An area has been reserved in the System Status Table to provide direct indication of communication port activity to the user through the LCS. This data is a copy of the counters normally returned in response to a Report Communication Event Log instruction. The user may access these records by executing a PULL from the System Status Table.

EXAMPLE: Status Table Organization
            2504 Message Counter LSB
            2505   MSB
            2506 Event Counter   LSB
            2507   MSB

```
  2507                    AAAA = Data Register
+[PULS]+----+----+----+----+(PSH)+
  2                      2
                        BBBB = Event Counter
                        CCCC = Message Counter
```

EVENT LOG

The Event Log consists of a 64-byte circulating buffer that records each serial port receive and transmit operation. The buffer is cleared at power-up. Each operation is recorded in one byte of the buffer in chronological order. The format of the stored information follows:

Receive Operations		Transmit Operations	
Bit 7	1	Bit 7	0
Bit 6	0 (normal nodal address)	Bit 6	1
Bit 5	0	Bit 5	0
Bit 4	0	Bit 4	0
Bit 3	0	Bit 3	0
Bit 2	0	Bit 2	0
Bit 1	0 (no transmission errors) 1 (framing, parity, overrun or CRC error)	Bit 1	0
Bit 0	0	Bit 0	0

The host retrieves the entire buffer using the Report Communication Event Log instruction. The log is sent, beginning with the most recent entry. (Please refer to the Report Communication Event Log instruction diagram for further details).

COMMUNICATION PORT RECEIVE TO COMMUNICATION PORT TRANSMIT

The following procedure occurs when the communication port receives a message that requires a response. This sequence is begun after the three-character idle state is sensed. At that point, the receiver is disabled.

1.   Message is processed and response is prepared.

2.   Request-to-send is activated.

3.   A "mark" state is held for one character time to allow the host transmitter to deactivate and allow local modem devices to become fully active.

4.   The message transmission is begun.

COMMUNICATION PORT TRANSMIT TO COMMUNICATION PORT RECEIVE

The following procedure terminates a transmission and surrenders the link to the host.

1.   A "mark" condition is held for four character times following the transmission of the last character. This insures that the host senses the required three character times.

2.   The transmitter is disabled, and the request-to-send is deactivated.

3.   The receiver is reenabled.

MODBUS/RTU INSTRUCTION SET

Table 19 lists the MODBUS RTU instructions and function codes that the communication port is programmed to recognize. The instruction descriptions that follow are separated into function categories. Each actual instruction description includes title, definition and instruction, and response message formats.

The communication port increments the starting address by 1, therefore it must receive a starting address that is one unit lower than the location desired. When addressing I/O location 0, the message must contain 65,535. The first byte of a two-byte number is always the most significant byte and the second is always the least significant byte.

Figure 33 defines various characters of the text. Instruction execution times are listed in Table 20. Legal ranges for command parameters are:

- Real I/O: 0-255 for the 620-11
                        0-639 for the 620-14
                        0-2039 for the 620-16

- Control I/O   0-4095 for 620-11/14/16

- Registers   4096-8191 for 620-11/14/16

TABLE 19 - MODBUS RTU INSTRUCTIONS AND FUNCTION CODES

FUNCTION CODE	INSTRUCTION
Input/Ouput Instructions	
01/02	Read N I/O
05	Modify Coil
15	Force Multiple Coils
Register Instructions	
03	Read N Registers
04	Read N I/O Registers
05	Modify Register or I/O Register
16	Preset Multiple Registers
Diagnostic Instructions	
08	Loop Back Test
12	Report Communication Event Log

TABLE 20 - INSTRUCTION EXECUTION TIMES

INSTRUCTION		EXECUTION TIMES
Read N I/O		353 μsec + N (6.7 μsec)
Modify Coil		399 μsec
Read N Registers		304 μsec + N (76 μsec)
Read N I/O Registers	(Register Area)	315 μsec + N (76 μsec)
	(I/O Area)	318 μsec + N (120.7 μsec)
Modify Register Or I/O Register	(Register Area)	416 μsec
	(I/O Area)	470 μsec
Loop-back Test		162 μsec + N (40 μsec)
Report Communication Event Log		3.113ms
Force Multiple Coils		413 μsec + N (6.6 μsec)
Preset Multiple Registers		422 μsec + N (3.8 μsec)

N = N value from command

Nodal Address - One character (8 bits) that contains the communication port address. The address range is 0-255.

Function Code - Control character used to specify the operation to be performed (command), or the operation that was performed (response). A response message serving as an error message has the most significant bit of the function code set to 1.
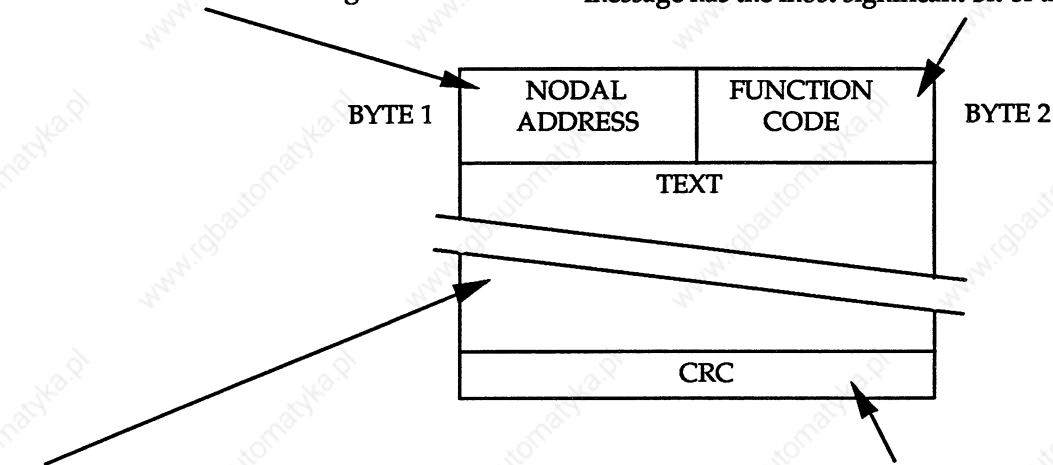
Text - Contains function code modifiers, data and/or response information. The text contains a variable number of characters. The most significant byte always leads 16-bit characters. This pertains to starting addresses and 16-bit register data.

CRC- A character containing a 16-bit check calculation of the message content ($X^{16} + X^{15} + X^2 + 1$ divisor, preset to 65535). With transmitted messages, the calculation includes the nodal address, function code and text with the result added to the end of the message. With received messages the calculation includes the nodal address, function code, text and CRC.

FIGURE 33 - GENERAL RTU MESSAGE TEXT STRUCTURE

INPUT/OUTPUT INSTRUCTIONS

Input/Output instructions provide access to the ON/OFF status of individual of groups of addresses in the 620-11/14/16 Logic Controllers Input and Output Status Tables. READ I/O instructions obtain the status and WRITE I/O instructions set the status.

The response to a successful READ I/O instruction is the logical "or" of the input and output status locations requested in the READ I/O instruction.

The response to a successful WRITE I/O instruction is an acknowledgement that the write was successful.

Read N I/O

This instruction reads the status of I/O in the 620-11/14/16 CPMs. It reads the logical "or" of the I/O Status Table. This instruction is executed for both 01 and 02 function code.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2 — Function Code = 01, 02
3	STARTING ADDRESS - 1		4 — 0 ≤ Starting Address ≤ Address Limit
5	N		6 — 1 ≤ N ≤ 2048 (N = Number of I/O Points)
7	CRC		8

Response Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2
		L	3 —— Byte Count, 0 ≤ L ≤ 255 (If L = 0, then byte count = 256)
		DATA	4
		DATA	
		DATA	x —— x = 3 + L
x + 1	CRC		x + 2 — I/O data packed into the data bytes with the least significant byte of four representing the data at the starting address.

Status: 0 = OFF
1 = ON

99
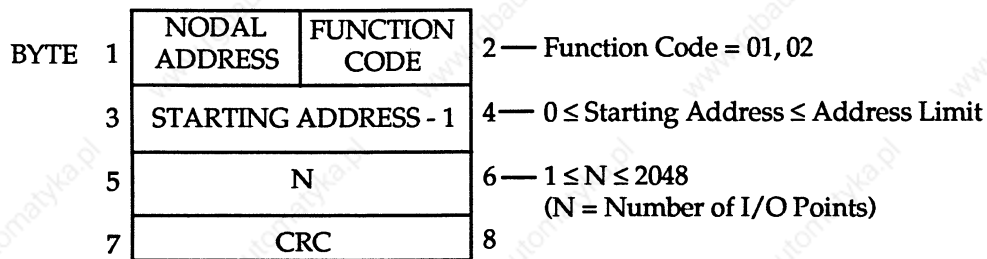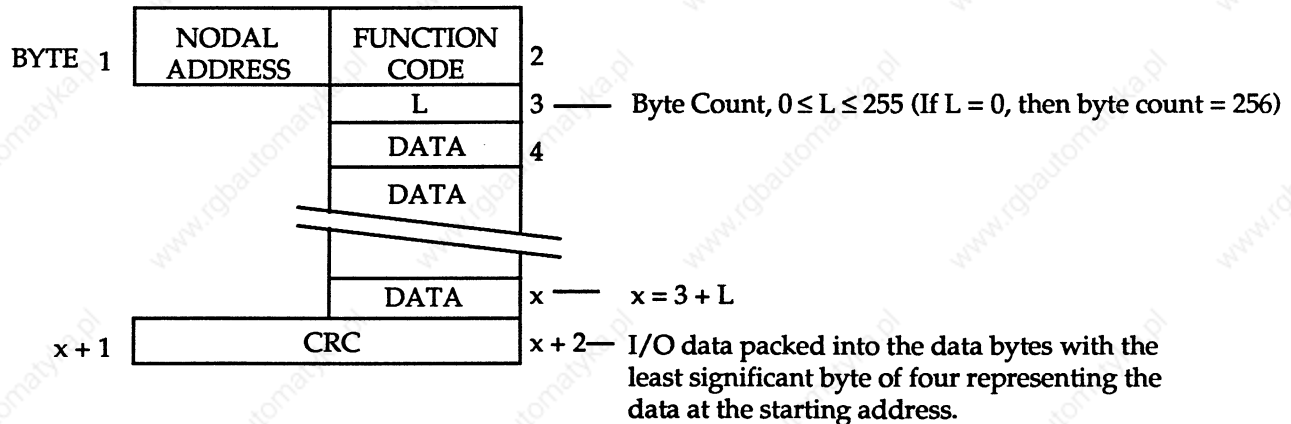
Modify Coil

This instruction writes the status of processor I/O in the 620-11/14/16 Control Processor Modules. The write operation is directed to both real outputs and to the Output Status Table. The output write protect function must be disabled through the Communication Port Configuration Menu.

Instruction Format:

BYTE	1	NODAL ADDRESS	FUNCTION CODE	2	— Function Code = 05
	3	OUTPUT ADDRESS - 1		4	— 0 ≤ Output Address ≤ Address Limit
	5	DATA		6	— Output ON = 65280 OFF = 0
	7	CRC		8	

Response Format (Instruction Executed):

BYTE	1	NODAL ADDRESS	FUNCTION CODE	2
	3	OUTPUT ADDRESS - 1		4
	5	OUT. STATUS WRITTEN		6
	7	CRC		8

6 —— Status obtained with a follow-up read of the I/O Status Table.

Output ON = 65280

OFF = 0

Force Multiple Coils

This instruction writes multiple locations in both the Output Status Tables and the real outputs. The output write protect function must be disabled through the Communication Port Configuration Menu.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2 — Function Code = 15
3	OUTPUT ADDRESS - 1		4 — 0 ≤ Output Address ≤ Address Limit
5	N		6 — 1 ≤ N ≤ 800
	7	BYTE COUNT	— 1 ≤ Byte Count ≤ 100
	8	DATA	— Packed status data, 8 per byte from starting point at LSB of first byte. Status: 0 = OFF; 1 = ON
	x	DATA	— x = 7 + Byte Count
x + 1	CRC		x + 2

Response Format (Instruction Executed):

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2
3	STARTING ADDRESS - 1		4
5	N		6
7	CRC		8

101
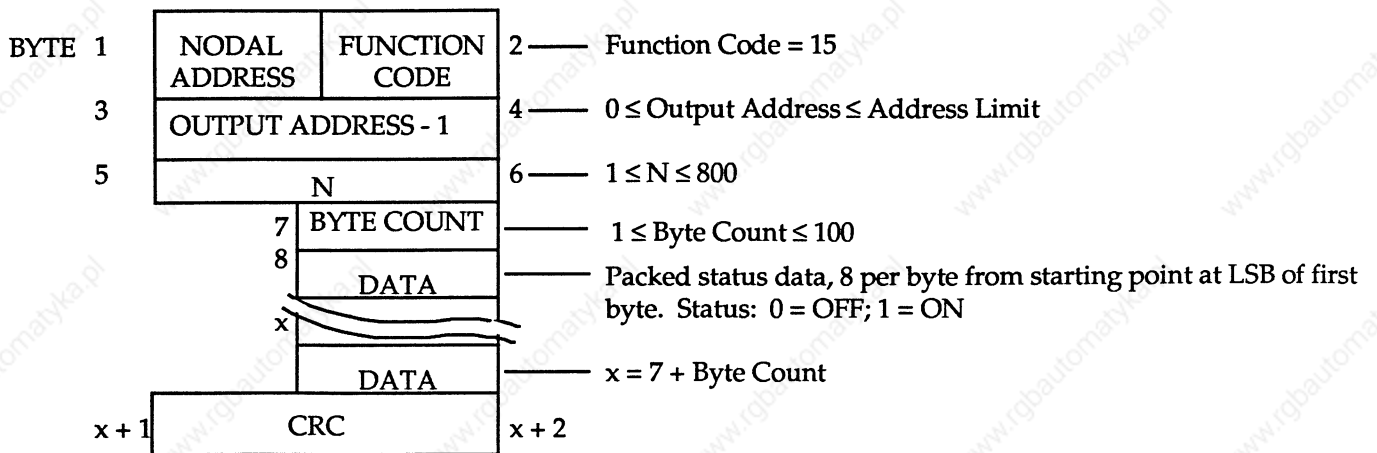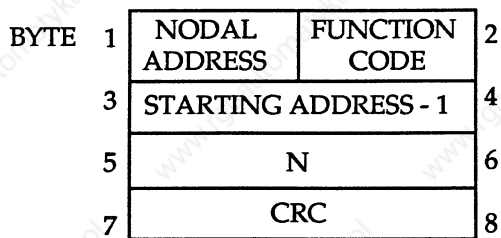
REGISTER INSTRUCTIONS

Register instructions read or write the contents of the 620-11/14/16 Logic Controller's Data Registers; transfer multiple 16-bit groups of data from I/O modules or the Register Table to the host; transfer individual 16-bit groups of data from the host to the I/O modules or to the Register Table; and transfer multiple 16-bit groups of data from the host to the Register Table.

Read N Registers

This instruction reads the contents of LCS Data Registers.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2	—— Function Code = 03
3	STARTING ADDRESS - 1		4	—— 4096 ≤ Starting Address ≤ Address Limit
5	N		6	—— 1 ≤ N ≤ 128 (N = Number of Registers)
7	CRC		8	

Response Format (Instruction Executed):

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2	
		L	3	—— Byte Count 0 ≤ L ≤ 255 (If L = 0, then Byte count = 256)
4	DATA		5	—— 1st Register
6	DATA		7	—— 2nd Register
	DATA			
x - 1	DATA		x	—— x = 3 + L
x + 1	CRC		x + 2	

102
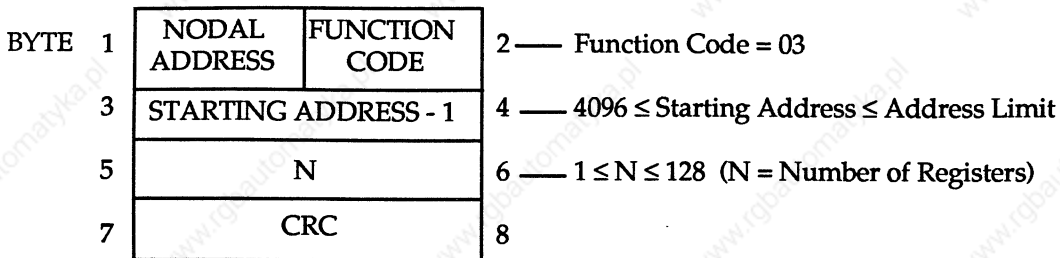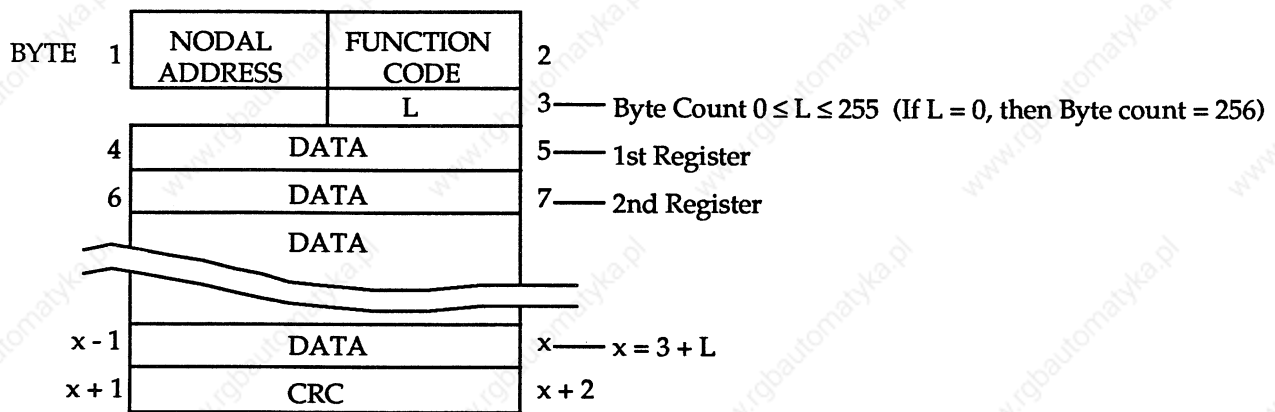
Read N I/O Registers

This instruction reads data from Data Registers and intelligent I/O modules located in the 620-11/14/16 Control Processor Module's (CPM's) real I/O. The communication port uses a PULL type instruction to the CPM to retrieve this type of register data. Read N I/O Registers cannot be performed from real output modules. This instruction cannot be executed in PROGRAM mode if directed to the I/O area.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2 — Function Code = 04
3	STARTING ADDRESS - 1		4 — Data Registers: $4096 \leq$ Starting Address $\leq$ Address Limits
			I/O Registers: $0 \leq$ Starting Address $\leq$ Address Limits
5	N		6 — $1 \leq N \leq 128$
			(N = Number of Registers)
7	CRC		8

Response Format (Instruction Executed):

BYTE 1	NODAL ADDRESS	FUNCTION CODE	
		L	2 — Byte Count, $0 \leq L \leq 255$ (If L = 0, then byte count = 256)
4	DATA		3 — 1st Register
6	DATA		5 — 2nd Register
	DATA		7
x - 1	DATA		x — x = 3 + L
x + 1	CRC		x + 2
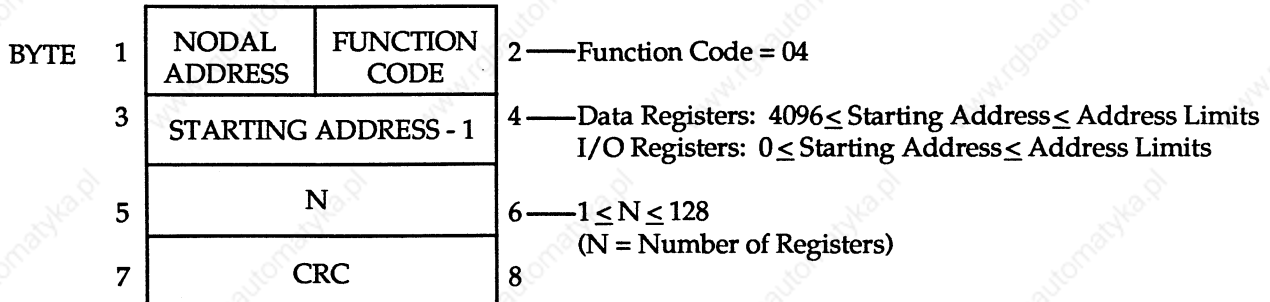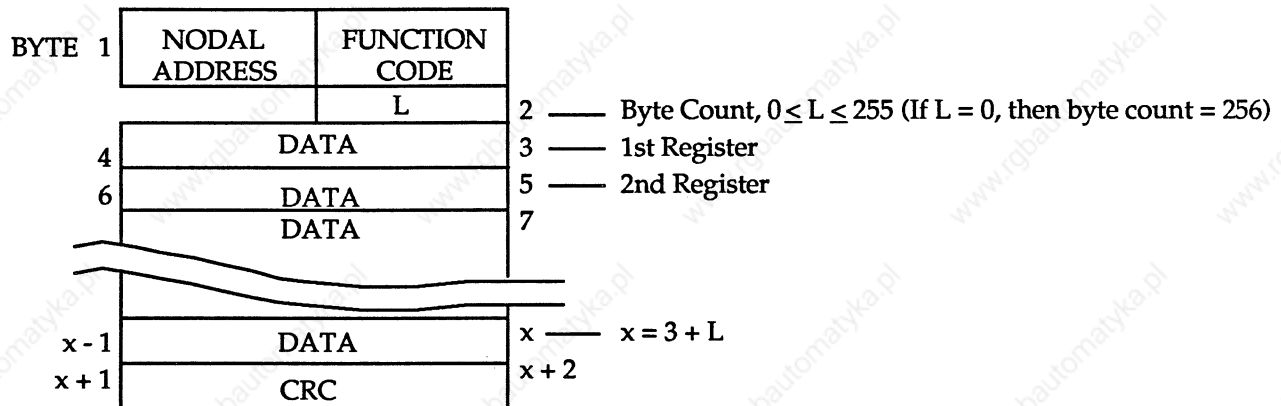
Modify Register or I/O Register

This instruction writes to intelligent I/O modules or to the Logic Controller's Data Register Table, depending on the starting address. For example, in the 620 LCS, analog outputs reside in the real I/O portion of the memory map and must be addressed accordingly.

The communication port uses a PUSH operation to write to real I/O. This can be performed only when the LCS is in RUN mode. The write output protect function must be disabled through the Communication Port Configuration Menu.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2 — Function Code = 06

BYTE 1 — NODAL ADDRESS | FUNCTION CODE — 2 —— Function Code = 06

3 — STARTING ADDRESS - 1 — 4 —— Data Registers: 4096 ≤ Starting Address ≤ Address Limit
I/O Registers: 0 ≤ Starting Address ≤ Address Limit

5 — REGISTER DATA — 6

7 — CRC — 8

Response Format (Instruction Executed):

BYTE 1 — NODAL ADDRESS | FUNCTION CODE — 2

3 — STARTING ADDRESS - 1 — 4

5 — REGISTER DATA — 6 ——Register data received in the command message.

7 — CRC — 8

104
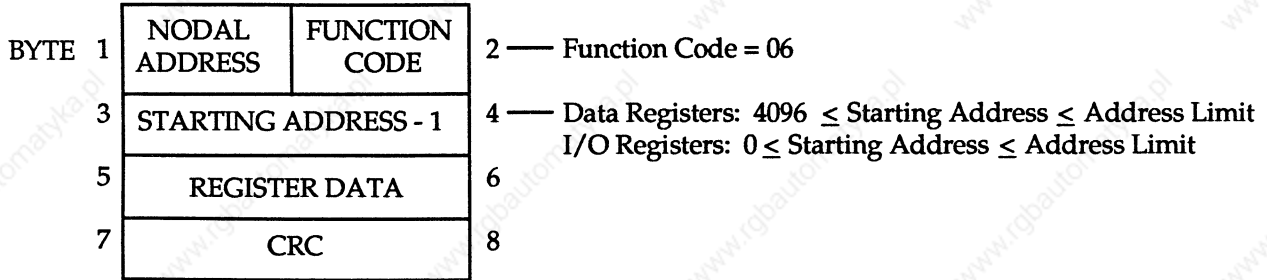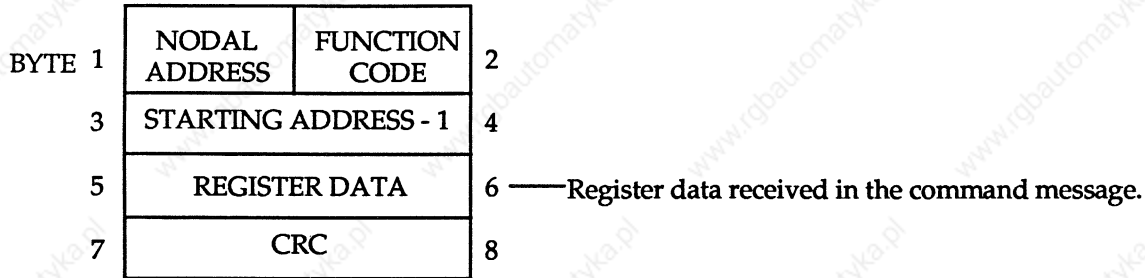
Preset Multiple Registers

This instruction writes to multiple locations in the Data Register Table. The communication port's output write protect function must be disabled through the Communication Port Configuration Menu.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2 —— Function Code = 16
3	STARTING ADDRESS - 1		4 —— $4096 \leq$ Starting Address $\leq$ Address Limit
5	N		6 —— $1 \leq N \leq 100$
7		BYTE COUNT	—— $2 \leq$ Byte Count ≤ 200
8	REGISTER DATA		9
x - 1	REGISTER DATA		x —— x = 7 + Byte Count
x + 1	CRC		x + 2

Response Format (Instruction Executed):

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2
3	STARTING ADDRESS - 1		4
5	N		6
7	CRC		8
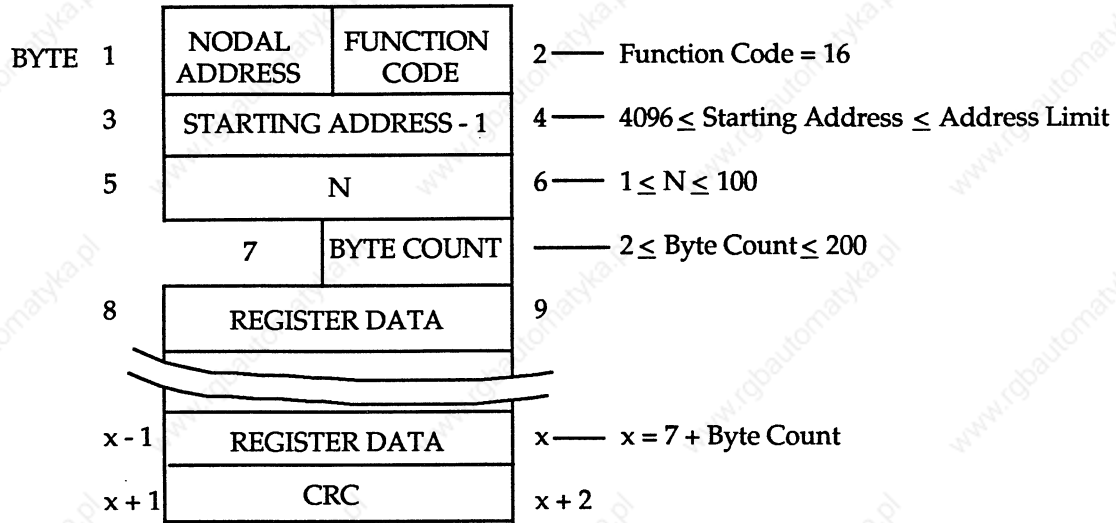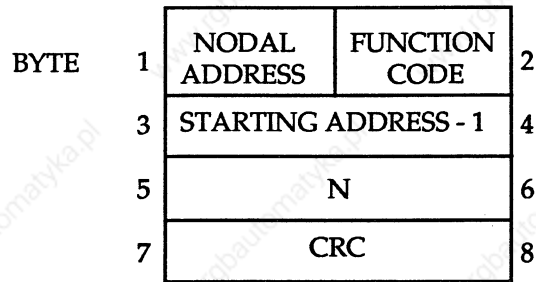
DIAGNOSTIC INSTRUCTIONS

These instructions obtain communication port and CPM status information. They also ensure that the physical data link between host and communication port is functioning properly.

Loop Back Test

This instruction enables the host to test its serial link with the communication port. When it receives this message, the communication port echoes the message back to the host.

Instruction Format:

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2
3	DATA	DATA	4 —— Data (up to 256 bytes)
x - 1	DATA	DATA	x —— x = 2 + Number of bytes of data
x + 1	CRC		x + 2

Response Format (Instruction Executed):

BYTE 1	NODAL ADDRESS	FUNCTION CODE	2
3	DATA	DATA	4 —— Data (up to 256 bytes)
x - 1	DATA	DATA	x —— x = 2 + Number of bytes of data
x + 1	CRC		x + 2

106

Report Communication Event Log

The communication port maintains an event status word, an event count, a received message count and an event log of its exchanges with the network host.

Instruction Format:

```
BYTE   1 ┌──────────┬──────────┐ 2 ── Function Code = 12
         │ NODAL    │ FUNCTION │
         │ ADDRESS  │ CODE     │
       3 ├──────────┴──────────┤ 4
         │        CRC          │
         └─────────────────────┘
```

Response Format (Instruction Executed):

```
        BYTE   1 ┌──────────┬──────────┐ 2
                 │ NODAL    │ FUNCTION │
                 │ ADDRESS  │ CODE     │
                 │          ├──────────┤ 3 ──Byte Count L = 70
                 │          │    L     │
               4 ├──────────┴──────────┤ 5 ──Status = 0
                 │       STATUS        │
               6 ├─────────────────────┤ 7
                 │    EVENT COUNTER     │
               8 ├─────────────────────┤ 9
                 │   MESSAGE COUNTER    │
Most recent  10 ├─────────────────────┤ 11 ──Next most recent event byte
event byte       │     EVENT LOG       │

63rd event   72 ├─────────────────────┤ 73 ── 64th event byte
byte             │                     │
              74 ├─────────────────────┤ 75
                 │        CRC          │
                 └─────────────────────┘
```
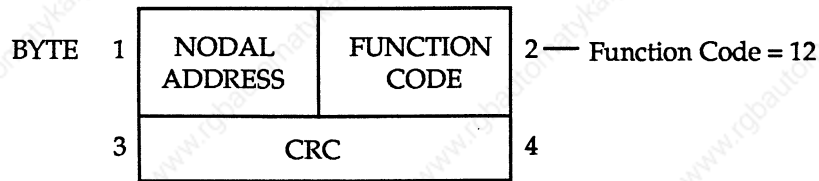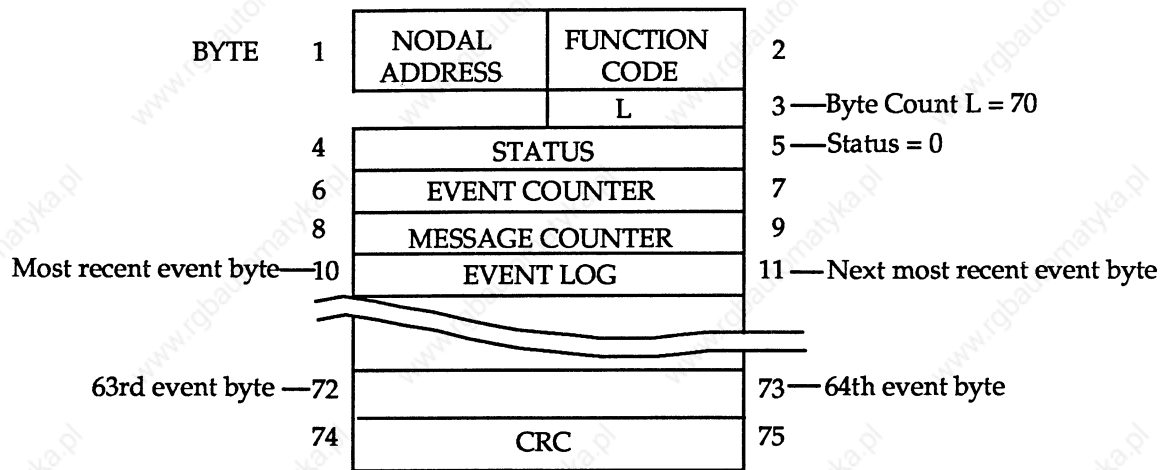
TABLE 21 - 620-11/14/16 INSTRUCTIONS, OPCODES AND EXECUTION TIMES

SYMBOL	INSTRUCTION NAME	HEX CODE	BINARY CODE								EXECUTION TIME MICRO-SECONDS	
			23	22	21	20	19	18	17	16	MINIMUM	MAXIMUM
--] [--	Normally Open	C8	1	1	D	F	1	0	0	0	3.2	3.2
--]/[--	Normally Closed	CC	1	1	D	F	1	1	0	0	3.2	3.2
--]/\[--	Transition On	43	0	1	D	F	0	0	1	1	4.0	6.0
--]\/[--	Transition Off	4B	0	1	D	F	1	0	1	1	4.0	6.0
--]BR[--	Bit Read	03	0	0	D	F	0	0	1	1	9.0	9.0
--]O[--	NOT	CB	1	1	0	0	1	0	1	1	2.8	2.8
--NOP--	No Operation	FF	1	1	1	1	1	1	1	1	2.4	2.4
--ISS--	Input Status Scan	8F	1	0	0	0	1	1	1	1	9.0	1277.0
N/A	Down Branch	C1	1	1	0	0	0	0	0	1	4.0	4.0
N/A	Double Down Branch	C2	1	1	0	0	0	0	1	0	4.2	4.2
N/A	Up Branch	C3	1	1	0	0	0	0	1	1	5.4	6.4
--(R)--	Retentive Output	C5	1	1	D	F	0	1	0	1	5.8	5.8
--( )--	Output Coil	C4	1	1	D	F	0	1	0	0	5.8	5.8
--(L)--	Latch Output	C6	1	1	D	F	0	1	1	0	5.8	5.8
--(U)--	Unlatch Output	C7	1	1	D	F	0	1	1	1	5.8	5.8
--(BW)--	Bit Write	85	1	0	D	F	0	1	0	1	11.0	12.0
--<B2>--	Indirect BringIn	89	1	0	0	0	1	0	0	1	18.0	63.0
--<I2>--	Indirect SendOut	06	0	0	0	0	0	1	1	0	15.0	108.0
--[B2]--	BringIn	88	1	0	0	0	1	0	0	0	10.0	32.0
--(S2)--	SendOut	07	0	0	D	F	0	1	1	1	9.0	75.0
--[K2]--	Kin Constant In	8B	1	0	0	0	1	0	1	1	10.0	10.0
--[FPK]--	FP Kin LS Register	9B	1	0	0	1	1	0	1	1	19.0	19.0
--[FPK]--	FP Kin MS Register	AB	1	0	1	0	1	0	1	1	N/A	N/A
--[FP]--	FP Bring In	A8	1	0	1	0	1	0	0	0	12.0	12.0
--(FP)--	FP SendOut	27	0	0	1	0	0	1	1	1	9.0	9.0
--(PSH)--	Push I/O	84	1	0	0	0	0	1	0	0	7.0	*24+32n
--(PSH)--	Push Register	86	1	0	0	0	0	1	1	0	7.0	*12+3n
--[PUL]--	Pull I/O	80	1	0	0	0	0	0	0	0	7.0	*26+32n
--[PUL]--	Pull Register	82	1	0	0	0	0	0	1	0	8.0	*14+3n
--[PULS]--	Pull Status	81	1	0	0	0	0	0	0	1	8.0	*12+5n
--EOS--	End Of Skip	34	0	0	1	1	0	1	0	0	6.0	7.0
--RBP--	Return Beginning Pgm	05	0	0	D	F	0	1	0	1	3.0	5.0
--NSKR--	Not Skip & Retain	46	0	1	D	F	0	1	1	0	7.0	23.0
--NSKD--	Not Skip & De-energize	47	0	1	D	F	0	1	1	1	5.0	16.0
N/A	End of Memory	30	0	0	1	1	0	0	0	0	3.6	3.6
--(TOF)--	TOF Timer .01	40	0	1	H	0	0	0	0	0	6.0	16.0
--(TOF)--	TOF Timer .1	41	0	1	H	0	0	0	0	1	6.0	16.0
--(TOF)--	TOF Timer 1.0	42	0	1	H	0	0	0	1	0	6.0	16.0
--(TON)--	TON Timer .01	48	0	1	H	0	1	0	0	0	6.0	16.0
--(TON)--	TON Timer .1	49	0	1	H	0	1	0	0	1	6.0	16.0
--(TON)--	TON Timer 1.0	4A	0	1	H	0	1	0	1	0	6.0	16.0
COUNTER	Up/Down Counter	4F	0	1	H	0	1	1	1	1	12.0	22.0
-TIMER	Retentive Timer .01	4C	0	1	H	0	1	1	0	0	6.0	18.0
-TIMER	Retentive Timer .1	4D	0	1	H	0	1	1	0	1	6.0	18.0
-TIMER	Retentive Timer 1.0	4E	0	1	H	0	1	1	1	0	8.0	18.0
--[DLA]--	Delay	CF	1	1	0	0	1	1	1	1	#0.0+n	#10.0+n

F, D = An "F" in bit 20 denotes a force bit that indicates if the force is ON or OFF. A "D" in bit 21 denotes a data bit that indicates the status of the force in the ON state. Note that a normally open contact has power flow in the closed position and a normally closed contact has power flow in the open position.

* Where 'n' equals the number of registers (1-8).

Where 'n' equals the amount of delay (10-32760 micro-seconds)

SYMBOL	INSTRUCTION NAME	HEX CODE	BINARY CODE 23	22	21	20	19	18	17	16	EXECUTION TIME (MICROSECONDS) MINIMUM	MAXIMUM
SEQNCR	Sequencer										45.0	109.0
	Sequencer Size	8A	0	1	0	0	1	0	1	0		
	Step Number Address	8C	1	0	0	0	1	1	0	0		
	Data Table Step 1	8B	1	0	0	0	1	0	1	1		
	Control Output Addr.	07	0	0	0	0	0	1	1	1		
--(LS2)--	Load Sequencer	44	0	1	0	0	0	1	0	0	6.0	61.0
--(US2)--	Unload Sequencer	45	0	1	0	0	0	1	0	1	6.0	91.0
--SUB--	Subroutine	24	0	0	1	0	0	1	0	0	5.0	13.0
--RTS--	Return to Sub	14	0	0	0	1	0	1	0	0	5.0	19.0
--JSR--	Jump to Sub	04	0	0	0	0	0	1	0	0	11.0	31.0
--[BIN]--	BCD -- BIN Conversion	0F	0	0	0	0	1	1	1	1	38.0	38.0
--[BCD]--	BIN -- BCD Conversion	1F	0	0	0	1	1	1	1	1	39.0	39.0
--[INT]--	FP -- INT Conversion	3F	0	0	1	1	1	1	1	1	33.0	44.0
--[FLT]--	INT -- FP Conversion	2F	0	0	1	0	1	1	1	1	33.0	43.0
--]*[--	Multiply	0C	0	0	0	0	1	1	0	0	6.0	109.0
--]/[--	Divide	0B	0	0	0	0	1	0	1	1	6.0	184.0
--]>[--	Greater Than	0A	0	0	0	0	1	0	1	0	7.0	21.0
--]<[--	Less Than	09	0	0	0	0	1	0	0	1	7.0	21.0
--]=[--	Equal To	08	0	0	0	0	1	0	0	0	7.0	21.0
--]Z[--	Test For Zero	8D	1	0	D	F	1	1	0	1	4.8	16.0
--]+[--	Add	0E	0	0	0	0	1	1	1	0	6.0	99.0
--]-[--	Subtract	0D	0	0	0	0	1	1	0	1	6.0	99.0
--[&]--	And	2C	0	0	1	0	1	1	0	0	6.0	12.0
--[OR]--	Or	2E	0	0	1	0	1	1	1	0	6.0	12.0
-[XOR]-	Exclusive Or	3E	0	0	1	1	1	1	1	0	6.0	13.0
-[ABS]-	Absolute Value	1C	0	0	0	1	1	1	0	0	6.0	76.0
-[SQRT]-	FP Square Root	2D	0	0	1	0	1	1	0	1	177.0	689.0
-[NOT]-	Invert (1s Compliment)	1D	0	0	0	1	1	1	0	0	6.0	8.0
-[NEG]-	Negate (2s Compliment)	1E	0	0	0	1	1	1	1	0	6.0	76.0
MATRIX	Matrix										15.0	1675.0
	Size	88	1	0	0	0	1	0	0	0		
	Source Matrix	8E	1	0	0	0	1	1	1	0		
	Reference Matrix	9E	1	0	0	1	1	1	1	0		
	Operator	AE	1	0	1	0	1	1	1	0		
	Destination Matrix	BE	1	0	1	1	1	1	1	0		
			MATRIX BIT ARRAY									
	Matrix Instructions Of 8 Real I/O	00	7	6	5	4	3	2	1	0		
	Move	02	0	0	0	0	0	0	0	0	15.0	1120.0
	Invert	04	0	0	0	0	0	0	1	0	15.0	1125.0
	Or	06	0	0	0	0	0	1	0	0	15.0	1423.0
	And	08	0	0	0	0	0	1	1	0	15.0	1423.0
	Exclusive Or	0A	0	0	0	0	1	0	0	0	15.0	1429.0
	Set 0	0A	0	0	0	0	1	0	1	0	15.0	842.0
	Set 1	0C	0	0	0	0	1	0	1	0	15.0	842.0
	Compare		0	0	0	0	1	1	0	0	15.0	1675.0

F, D = An "F" in bit 20 denotes a force bit that indicates if the force is ON or OFF. A "D" in bit 21 denotes a data bit that indicates the status of the force in the ON state. Note that a normally open contact has power flow in the closed position and a normally closed contact has power flow in the open position.

* Where 'n' equals the number of registers (1-8).

Where 'n' equals the amount of delay (10-32760 microseconds)

620-11/14/16 LOGIC CONTROLLER SYSTEM INSTRUCTION SET

RELAY LOGIC INSTRUCTIONS

Normally Open Contact - Examines an input for an ON condition; and an output for an energized condition.

Normally Closed Contact - Examines an input for an OFF condition; examines an output for a de-energized condition.

Transition On Contact - Acts as a one-shot; ON for one scan when its address energizes and OFF thereafter.

Transition Off Contact - Acts as a one-shot; ON for one scan when its address de-energizes and OFF thereafter.

Branch - Creates parallel branch circuits in a logic line.

Output - Energizes when preceding logic is true.

Retentive Output - Logic status is retained ON or OFF when power is removed. At program power-up all retentive outputs assume their last state before the power-down.

Latch Output - Energizes when preceding logic is true and remains energized regardless of logic changes. Must be unlatched to be de-energized.

Unlatch Output - De-energizes a latch output with an identical address when preceding logic is true. Remains unlatched regardless of logic changes.

Not - Inverts the state of the result register in a logic line. The visable effect is that normal line power flow logic is inverted.

Bit Read - Allows the user to read specified bit status within a register. This operates similar to a normally open contact. Example: Bit off (0) = no power flow; Bit on (1) = power flow.

Bit Write - Allows the user to write specified bit location within a register. Operates like a coil; for example, power flow sets the bit and no power clears the bit.

TIMER AND COUNTER INSTRUCTIONS

All timer instructions increment from zero toward the preset value.

Delay - Delays the scan for a period of time defined by the user. Valid time periods are expressed as integer from 0 to 65,535. When the Logic Controller System is in the Skip and De-energize Retentive Scan or Skip and Retain state, the operation is not executed. When the LCS is in the RUN/PROGRAM state, the status of conditional math within a line is examined. If the conditional logic is false, the delay is not executed. If it is true, the delay is executed and the scan delayed.

On Delay Timers (.01, .1, 1 second) - Start to time when the preceding logic is true. The output turns ON when the accumulated value equals the preset value. The accumulated time is reset to zero when the preceding logic is false.

Off Delay Timers (.01, .1, 1 second) - Start to time when preceding logic is false. The output turns OFF when the accumulated value equals preset. The accumulated time is reset to zero when the preceding logic is true.

Retentive On Delay Timer (.01, .1 and 1 second) - Separate timer RUN and RESET inputs. When the RUN input is false, the timer will not run and the accumulated value is retained. When the RESET input is false, the timer is reset. An ON signal is transferred to the output status table and I/O system when the accumulated value equals the preset value.

Up/Down Counter - Counts from - 32768 to + 32767 transferring an ON signal to the output status table and I/O system when the accumulated value equals the preset value. When a COUNT input toggles OFF to ON, the accumulated count changes. When the RESET input is false, the accumulated value is reset to zero.

SKIP INSTRUCTIONS

Not Skip and Retain - When preceding logic is false, all following logic line terminators are skipped, retaining their terminators present status, until a matching End of Skip instruction is encountered.

Not Skip and De-energize - When preceding logic is false, all following logic line terminators are skipped and their terminators are de-energized until a matching End of Skip instruction is encountered.

End of Skip - Marks the point where memory scan terminates skipping and resumes executing lines following Not Skip and Retain or Not Skip and De-energize instructions. Addresses must match.

Jump - When preceding logic is false, all following logic is jumped and not executed until a matching end of jump instruction is encountered.

Return To Beginning of Program - Instructs program scan to return to the beginning of the program.

INTEGER DATA MANIPULATION INSTRUCTIONS

Bring In - Transfers 16 bits of data from the I/O Status Table or 16 bits from the Register Table, to the CPM for use within the logic line.

Send Out - Transfers 16 bits of data from the preceding instructions to the I/O system and the Output status or 16 bits to the Register Table.

Pull - Transfers multiple 16-bit groups of data from the I/O modules (with PUSH/PULL capability) or the Register Table, to the Control Processor Module.

Push - Transfers multiple 16-bit groups of data from preceding logic to I/O modules (with PUSH/PULL capability), or to the Register Table.

Indirect Bring In - Transfers 16 bits of data from the address pointed to by the Indirect Bring In address in the I/O Status or Register Table. Allows multiplexing of input data.

Indirect Send Out - Transfers 16 bits of data from the preceding data instructions, to an address pointed to by the Indirect Send Out address. Allows multiplexing of data.

Signed Constant - Transfers a number between -32,768 and +32,767 from the user memory to the Control Processor Module.

Pull System Status Table - Transfers multiples of two 8-bit values from the system status table to the Control Processor Module, for use by the user.

INTEGER ARITHMETIC INSTRUCTIONS

Addition - Adds two 16-bit signed numbers.

Subtraction - Subtracts two 16-bit signed numbers.

Multiplication - Multiplies two 16-bit signed numbers.

Division - Divides a 32-bit signed dividend by a 16-bit signed divisor to yield a 16-bit signed quotient and a 16-bit remainder.

Equality Comparison - Compares for equality between two signed or unsigned data values.

Less Than Comparison - Compares for less than condition between signed data values.

Greater Than Comparison - Compares for greater than condition between signed data values.

Less Than Or Equal Comparison - Compares for less than or equal condition between signed data values.

Greater Than Or Equal Comparison - Compares for greater than or equal condition between signed data values.

Not Equal - Compares for inequality between two signed or unsigned data values.

Unsigned Less Than Comparison - Compares for less than condition between unsigned data values.

Unsigned Greater Than Comparison - Compares for greater than condition between unsigned data values.

Unsigned Less Than Or Equal Comparison - Compares for less than or equal condition between unsigned data values.

Unsigned Greater Than or Equal Comparison - Compares for greater than or equal condition between unsigned data values.

Test For Zero - Control Processor Module tests the specified register or 16 consecutive I/O status table locations for a zero condition. If a zero condition is detected, the contact will be ON.

Invert - Changes the state of each bit in a 16-bit register, producing the 1's complement of the value that was present.

Negate - Converts a positive integer number into a negative number or a negative number into a positive integer number in a 2's complement format.

Absolute Value - Converts any number contained in a register to a positive integer.

FLOATING POINT DATA MANIPULATION INSTRUCTIONS

Floating point operations use the same math operators as integer operations. The identifier of a floating point operation is in the type of data instructions associated with the operator.

Floating Point Bring In - Transfers two 16-bit data registers containing a floating point value from the Register Table to the Control Processor Module for use in the logic line.

Floating Point Send Out - Transfers two 16-bit data registers containing a floating point value from the preceding instructions to the Register Table.

Floating Point Constant - Transfers a floating point number stored as two 16-bit constants from the user memory to the Control Processor Module.

NOTE
Floating point numbers are stored in two consecutive 16-bit registers. The user always specifies the most significant register address.

FLOATING POINT ARITHMETIC INSTRUCTIONS

Addition - Calculates the sum of two 32-bit floating point values.

Subtraction - Calculates the difference of two 32-bit floating point values.

Multiplication - Calculates the product of two 32-bit floating point values.

Division - Calculates the quotient of two 32-bit floating point values, yielding a 32-bit, floating-point result.

Equality Comparison - Compares for equality of two floating point values.

Less Than Comparison - Compares for a less than condition between two floating point values.

Greater Than Comparison - Compares for greater than condition between two floating point values.

Not Equal Comparison - Compares for inequality between two floating point values.

Less Than Or Equal Comparison - Compares for less than or equal condition between two floating point values.

Greater Than Or Equal Comparison - Compares for greater than or equal condition between two floating point values.

Square Root - Returns the square root of a floating point number.

SEQUENCER INSTRUCTIONS

Sequencer - Allows the CPM to store up to 1024 16-bit groups of user-defined data in main memory. The data may be used to control repetitive operations or to store bulk data.

Load Sequencer - Allows data to be transferred to sequencer tables.

Unload Sequencer - Allows data to be transferred from sequencer tables before the sequencer table is executed.

CONVERSION INSTRUCTIONS

Binary To BCD Conversion - Converts a binary number into a 4-digit Binary Coded Decimal number. The BCD number can range from 0-9999.

BCD To Binary Conversion - Converts a 4-digit Binary Coded Decimal number obtained from a preceding Bring-In or PULL instruction to binary format.

Integer To Floating Point Conversion - Converts an integer obtained from a Bring-In or PULL to a 32-bit floating point number.

Floating Point To Integer Conversion - Converts a floating point number from a floating point Bring-In or from a preceding calculation to a 16-bit signed integer.

LOGIC INSTRUCTIONS

And - Performs a logical AND on two 16-bit registers.

Or - Performs a logical OR on two 16-bit registers.

Exclusive Or - Performs a logical EXCLUSIVE OR function on two 16-bit registers.

MATRIX INSTRUCTIONS

Move - Transfers data stored in a specified area of the I/O Status Table or Register Table to another area.

Invert - Inverts and transfers data stored in a specified area of the I/O Status Table or Register Table to another area.

Set Zero - Sets every bit of a matrix to zero.

Set One - Sets every bit of a matrix to one.

Or - Performs an OR of the contents of two matrices and transfers the results to a third matrix.

Exclusive Or - Performs an Exclusive OR of two matrices and transfers the result to a third matrix.

And - ANDs the contents of two matrices and transfers the result to a third matrix.

Compare - Compares two matrices for equality and stores the addresses of miscompares in a third matrix.

SUBROUTINE INSTRUCTIONS

Subroutine - Allows the Control Processor Module (CPM) to execute defined portions of the program on command.

Jump to Subroutine - Causes the CPM to jump immediately to an identified subroutine in the program and begin executing the subroutine program.

Return from Subroutine - Identifies the end of a subroutine.

MISCELLANEOUS INSTRUCTIONS

Input Status Scan - Temporarily halts program execution, allowing the Input Status Table to be updated.

No Operation - No operation occurs. Other than the program counter, the CPM state, is unaffected. Execution resumes with the instruction after the NOP.

APPENDIX II

COMMUNICATION PORT

PARAMETER STORAGE

Communication port parameters are stored in the Configuration area of the System Status Table in the 620-11/14/16 Control Processor Module.

Locations 09BBH (2491) through 09C0H (2496) are reserved for this purpose. The definition of these registers is listed in Figure 34.

	7							0	
09BBH **2491**	New Data	Port Enable	Test Mode	Memory Protect	Output Protect	Baud Rate			**PORT** **CONFIG.**
	Protocol	Duplex Mode	Flag Mode			Stop Bits	Parity		**PROTOCOL** **CONFIG.**
	0 - 255								**NODAL** **ADDRESS**
				Bad Flag	Bad Baud	Bad Addr	Xmtr Down		**PORT** **STATUS**
	Bit Pattern						LSB		**WARM**
09C0H **2496**	MSB	Bit Pattern							**START** **FLAG**

FIGURE 34 - PARAMETER STORAGE

PORT CONFIGURATION

Bit 7 **New Data** - This bit is a flag to the LCS that the configuration data has been modified and the communication port must be reconfigured. This bit is set by the Loader/Terminal whenever it writes new data to the System Status Table. It is cleared by the LCS when the reconfiguration is complete.

0 = No new configuration
1 = Configuration is new; reconfigure port.

Bit 6 **Port Enable** - This bit determines the active or inactive status of the port.

0 = Port disabled.
1 = Port enabled.

Bit 5 **Test Mode** - This bit selects a test mode in which the communication port will continuously transmit a fixed data pattern onto the serial network. The purpose of this test is to generate a symmetrical wave form that can be monitored with an oscilloscope in order to verify proper installation and wave shape at all nodes on the link.

0 = Normal mode.
1 = Test mode.

Bit 4 **Memory Write Protect** - This bit determines whether the port will accept or reject instructions that involve writing to the user program memory or the System Status Table

0 = User memory protected
1 = User memory write accepted

Bit 3 **Output Write Protect** - This bit determines whether the port will accept or reject instructions that involve writing to real outputs, the output status table or the register table.

0 = Outputs protected
1 = Output write accepted

Bits 2,1,0 **Baud Rate** - These bits are encoded to select the baud rate at which the Port transmitter and receiver will operate.

000 = 110   001 = 300
010 = 600   011 = 1200*
100 = 2400   101 = 4800*
110 = 9600*   111 = 19200*
* Only rates compatible with MODBUS RTU

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PROTOCOL CONFIGURATION

Bit 7   **Protocol** - This bit determines the protocol under which the port will operate.

      0 = Honeywell ABC
      1 = MODBUS RTU

Bit 6   **Duplex Mode** - This bit determines how the port Transmit and RTS drivers are controlled. In the Full Duplex/Point-to-Point mode, the drivers are always enabled. In the Half Duplex/Multidrop mode, the drivers are tri-stated whenever the port is not transmitting.

      0 = Full Duplex/Point-to-Point
      1 = Half Duplex/Multidrop

Bit 5   **Flag Mode** - This bit determines whether flag mode is active. If flag mode is selected, the port will monitor specified I/O addresses and transmit an unsolicited message whenever an off-on state change is detected. Note that flag mode is only compatible with the Full Duplex/Point-to-Point mode and the ABC protocol.

      0 = Flag mode
      1 = Normal mode

Bit 4,3 Not used.

Bit 2   **Stop Bits** - This bit determines the number of stop bits that delimit a message character.

      0 = 1
      1 = 2

Bit 1,0 **Parity** - This bit determines the parity, if any, associated with a message character.

      00 = Odd
      01 = Even
      10 = No parity
      11 = No parity

NODAL ADDRESS CONFIGURATION

Bits 7-0 **Nodal Address** - These bits specify the network Nodal Address assigned to the port. The Honeywell ABC protocol is limited to addresses 0-31. The MODBUS RTU protocol allows addresses 1-255.

      0000000 = 0
      0000001 = 1   ...etc.
      1111111 = 255

PORT STATUS

Bits 7,
6,5,4   Not used

Bit 3   **Bad Flag Mode** - This bit indicates that an invalid combination of flag mode and duplex mode has been selected and that flag mode, though selected, is disabled.

      0 = Flag mode selection OK
      1 = Flag mode selection is invalid

Bit 2   **Bad Baud Rate** - This bit indicates that an invalid combination of baud rate and protocol has been selected.

      0 = Baud rate OK
      1 = Baud rate faulty

Bit 1   **Bad Address** - This bit indicates that an invalid combination of nodal address and protocol has been selected.

      0 = Nodal address OK
      1 = Nodal address faulty

Bit 0   **Transmitter Down** - This bit indicates that the port transmitter is not functional. The bit is set whenever there is a fail/safe timeout on the port transmitter and is cleared at the successful completion of any message transmission.

      0 = Transmitter OK
      1 = Transmitter failure

WARM START FLAG

Bits 7-0 **Bit Pattern (LSB)**
Bit Pattern (MSB) - This bit pattern indicates to the port configuration routine in the LCS that the port has been configured at some time previously. If this pattern is not detected at power-up, the port will be configured according to the default set-up guidelines. If the pattern is detected, the port will be configured according to the configuration data in the System Status Table.

      01010000
      11111010 = Warm Start

PORT CONFIGURATION SEQUENCE THROUGH THE COMMUNICATION PORT AND 620-0048/0052 MODULES

The built-in communication port may be configured through the port itself or a 620-0048/0052 Data Collection Module by writing to locations 2491, 2492 and 2493 in the System Status Table.

The configuring device writes the Port Configuration (2491), Protocol Configuration (2492) and Nodal Address (2493) bytes to the System Status Table. The New Data bit (7) must be set to 1 in the Port Configuration byte if anything other than Memory Protect or Output Protect has changed. (Memory Protect and Output Protect have a dedicated command in the ABC Protocol instruction set). This flags the LCS that the set-up data has been modified and the communication port must be reconfigured.

When the communication port service routine in the LCS notes that a reconfiguration has been requested, action will be taken immediately.

Any operation in progress (receive, transmit or command execution) will be terminated. The communication port will be configured according to the set-up data and operation will resume from scratch. This means a response to the WRITE N SYSTEM STATUS REGISTERS command will not be returned if the communication port is used to configure itself.

The configuring device may elect to follow up the write command with a read of the Port Status (2494) byte. This allows for the detection of any errors that resulted from the configuration.

ASYNCHRONOUS BYTE COUNT PROTOCOL

The Honeywell defined Asynchronous Byte Count Protocol (ABC protocol) is designed for use in localized point-to-point and multidrop applications. It accommodates the use of modems where RTS is the only active modem control line involved. Special data encoding (e.g., ASCII) or control character insertion and deletion is unnecessary because of data transparency. This simplifies the process of developing communication.

MESSAGE STRUCTURE

Standard configuration character format contains 11 bits (start, 8 data, parity, and stop) and has odd parity. Optional configuration character format contains 10 bits (start, 8 data, 1 stop bit). See Figures 35 and 36 for more details.

DATA

| START BIT | LSB | | | | | | | MSB | PARITY BIT | STOP BIT |

ORDER OF TRANSMISSION
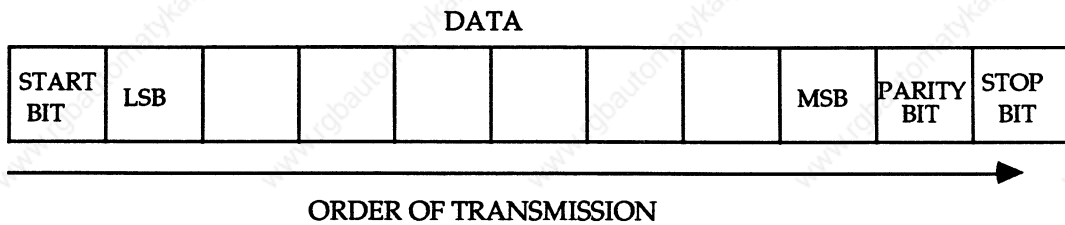
FIGURE 35 - ABC PROTOCOL CHARACTER FORMAT

DATA

| START BIT | LSB | | | | | | | | MSB | STOP BIT |

ORDER OF TRANSMISSION
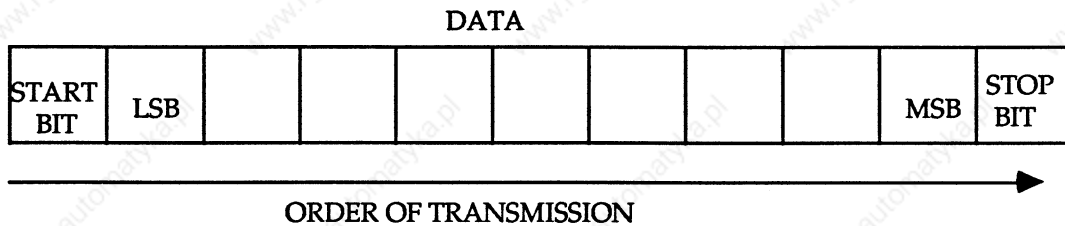
FIGURE 36 - ABC PROTOCOL OPTIONAL CHARACTER FORMAT

MESSAGE FORMAT

Figure 37 summarizes message format. Character definitions for message format follow.

SOH - (1) Start of header, 8 bits.

Nodal Address - An 8-bit binary number that identifies the secondary station involved in the message exchange. Addresses available for communication port applications range from 0 to 31. No two devices may have the same nodal address if the secondaries are to respond to received commands. Nodal address 255 is reserved for broadcast applications.

Control -An 8-bit character that identifies the message type.

ETB - (23) - End of transmission block, 8 bits.

STX - (2) - Start of text, 8 bits.

Opcode - This is the first character of the message proper and is defined by the application. It consists of 8 bits, and it identifies the type of operation that the receiving device is to perform. This character is 0 in response messages to the host device.

Message Text Length - This is a 16-bit binary number that specifies the number of characters contained in the message text. The upper limit of this value depends on the buffer size of the devices involved.

Byte count vs. word count is used to accommodate transmit/receive routines that interface with 8-bit ACIA's communication interfaces.

Text - This consists of 16-bit words that contain opcode modifiers and/or data. Data less than 16 bits is justified to the LSB of the word.

Checksum - This is an 8-bit byte that represents the binary addition, with carry between bits of each character between and including the nodal address and the last text character.

ETX - (3) - End of text.

SUMMARY

MSB   LSB

SOH	NODAL ADDRESS
CONTROL CHARACTER	ETB
STX	OPCODE
MESSAGE LENGTH	
CHECKSUM	ETX

TEXT

HEADER AND TEXT

SOH	NODAL ADDRESS
CONTROL CHARACTER	ETX
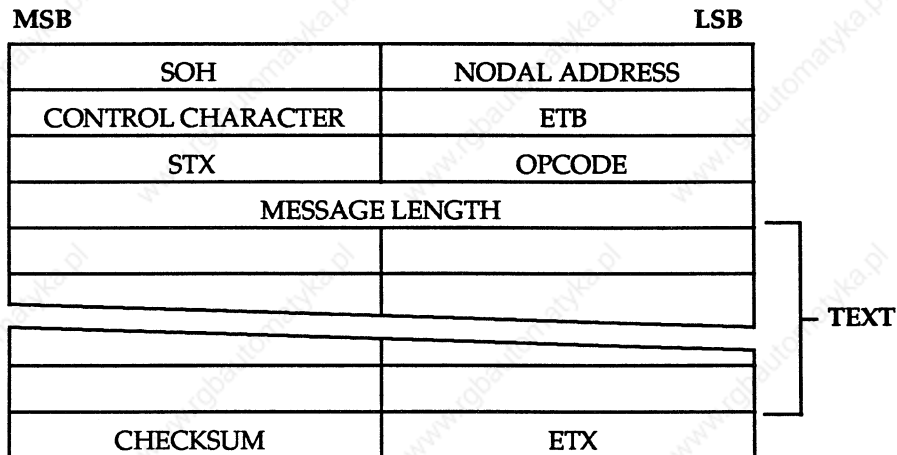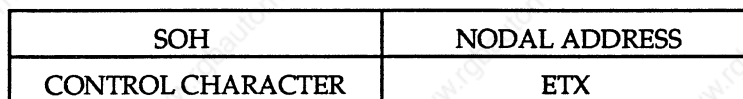
HEADER ONLY

FIGURE 37 - HEADER AND TEXT MESSAGE FORMAT

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ORDER OF TRANSMISSION

The most significant byte of the 16-bit word precedes the least significant byte. The words are transmitted in order from SOH/N.A. to Checksum/ETX.

MESSAGE TYPES

The ABC protocol includes two types of messages, supervisory and informational, which are identified by a control character. Table 22 lists the types of messages and identifying characters. Definitions of message types follow.

Command Information/Immediate Response - This information message is initiated by the host. The message requests the communication port to execute the command and respond with the results.

Command Information/Polled Response/ Acknowledgment Requested - This information message is initiated by the host. The message requests an immediate acknowledgment of the command reception. The results of the command execution are polled for at a later time through a poll command.

Command Information/Polled Response/No Acknowledge - This information message is initiated by the host. The message request is not acknowledged when the command is received. The results of the command execution are polled at a later time by a poll command. Nodal address 255 is used for a global nodal address to transmit to all devices on the network. It can only be used in conjunction with control character 130.

Response Information - This information message is in response to a host command or poll. This message is stored in the secondary station's buffer until it is overwritten during the execution of a subsequent command. As a result, the communication port may be repeatedly polled for retransmission of this message.

Poll - This command message from the host requests transmission or retransmission of the contents of the secondary station's transmit buffer. This command requires only the header portion be transmitted.

Acknowledge - This response from the secondary indicates a valid command was received. The acknowledge is only sent upon request by the host (command information/polled response message). This response requires only the header portion be transmitted.

Flag - A command by the secondary that signifies a change in predefined status bits within the secondary station. The text field contains the status information. This command requires both header and text to be transmitted.

TABLE 22 - ABC MESSAGE TYPE SUMMARY

HOST		SECONDARY	
CONTROL CHARACTER		CONTROL CHARACTER	
1	Command Information/ Immediate Response	129	Response Information
2	Command Information/ Polled Response/ Acknowledgment Requested	130	Acknowledge
130	Command Information/ Polled Response/No Acknowledge		
4	Poll	132	Flag

EXCHANGE PROCEDURES

The four basic methods of exchange available to the host and secondary devices are immediate response, polled response with acknowledge, polled response without acknowledge, and flag response.

With the polled response/acknowledge procedure, the host issues a command message, which includes an ACK request. If the secondary receives a valid command, it sends an acknowledge response, and executes the command. The response is held in the secondary's transmit buffer until it is polled for by the host (see Figure 38).

With the immediate response procedure, the host issues a command message, the secondary executes the command, and the secondary returns a result response (see Figure 39). Failsafe timeout delays within the host depend on the command issued. The host relinquishes line control while awaiting the response.

If the host issues a poll command before the secondary has finished the command execution, the host must wait for the secondary to respond with the result. Failsafe timeout delays within the host are short for the ACK response, but depend on the command issued for polled responses (see Figure 36).

With the polled response/no acknowledge procedure, the result is the same as a polled response/acknowledge procedure, except an acknowledge response is not returned.

The flag response is initiated by the secondary with a change in status of predefined control bits within the secondary station. There is no preceding command or subsequent acknowledgment by the host.
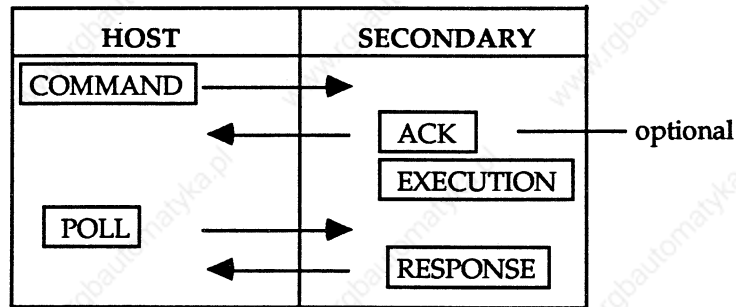
FIGURE 38 - POLLED RESPONSE DIAGRAM
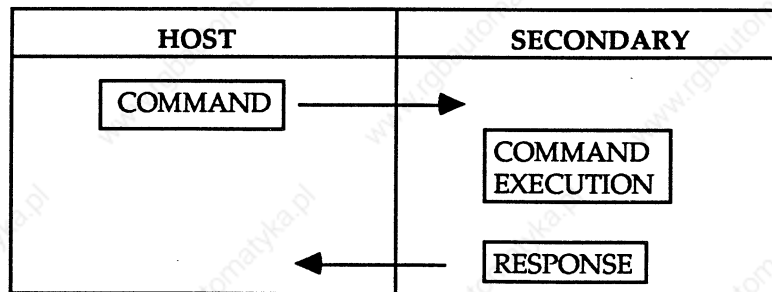
FIGURE 39 - IMMEDIATE RESPONSE DIAGRAM

MESSAGE RECEPTION TIMEOUT DELAYS

The intercharacter delay facilitates effective fault and abort detection. A delay of 10 character times or more between the reception of any two adjacent characters within a message results in an abort of the receive sequence.

To facilitate the use of software timers in the receiving stations, this 10 character timeout applies only to a receiver that is concentrating on the reception of the message. If a given receiver is distracted for x seconds to service an earlier message or another type of input, the abort timeout extends by x seconds. This allows the receiver the option of ignoring the software timer while servicing these other requests.

ERROR RECOVERY

Erroneous Secondary Receptions

Any errors generated during message reception results in no action by the secondary. The error situation is detected by the host through its timeout mechanisms. Retransmission is a host decision.

Host Reception of Erroneous Information Messages

The host has three options following the reception of an erroneous secondary response. The options are:

1. Retransmit the command.

2. Poll for a (re)transmission of the response.

3. Abort the exchange.

Host Reception of Erroneous Flag Responses

The host has two options following the reception of an erroneous flag response. The options are:

1. Poll for a (re)transmission of the response.

2. Ignore the message.

Host Reception of Erroneous Acknowledgments

The host has two options following the reception of an erroneous acknowledgment. The options are:

1. Retransmit the command.

2. Ignore the ACK (i.e., the host assumes that the erroneous acknowledgment should have been an ACK and not a flag response or an ACK from another station). This is a valid assumption in a point-to-point system with the flag mode disabled.

---

620 MEMORY WORD ORGANIZATION

Each memory word contains 24 bits. Figure 40 shows memory word organization.
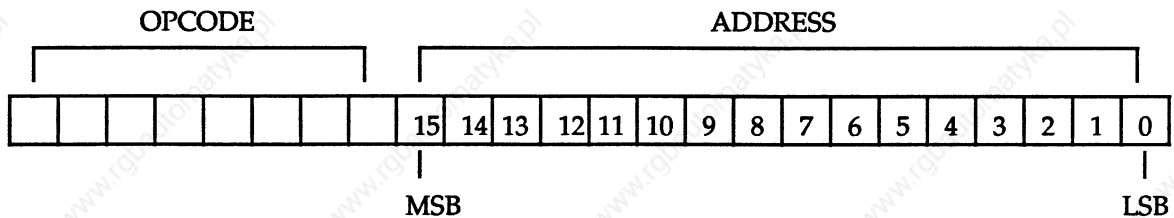
FIGURE 40 - 620 PROGRAM MEMORY WORD ORGANIZATION

CONTROL PROCESSOR MODULE CONFIGURATION THROUGH THE COMMUNICATION PORT OR 620-0048/0052 DATA COLLECTION MODULES

The 620-11/14/16 Control Processor Module and I/O System can be configured through the commun-ication port or a resident 620-0048/0052 Data Collection Module (DCM) as well as the 623-6100/6150 Loader/Terminal (L/T).

The Write I/O Configuration or Write Processor Control Configuration instructions within the Honeywell ABC Protocol are used for this purpose. If these commands are used for configuration, the following procedures apply:

1. There is a flag location in the System Status Table that the LCS uses to request new I/O or processor configuration if either configuration is invalid. This invalid condition can be a result of configuration data that has not been sent to the newly powered CPM, failure of battery backup in a powered-down processor, or some other error. This flag, called "I/O Configuration Request," is located in the System Status Table at address 2047 and is asserted with the value 170 (AA Hex). (See System Status Table in Appendix III.)

2. If the communication port or a 620-0048/0052 DCM is the primary configuration device, provisions must be made in the user's application to periodically monitor the I/O Configuration Request flag. This is done by using a Read N System Status Registers command. For more information, see Reading The Configuration With The Communication Port Or 620-0048/0052 in this Appendix.

The flag also should be checked at the completion of an on-line modification to an operating system to ensure that the Logic Controller received valid configuration data.

3. The assertion of I/O Configuration Request signifies that either or both the I/O configuration and the Control Processor Configuration are invalid. To determine which configuration must be reloaded, the user may elect to upload the I/O Configuration Table and the Control Processor Configuration Table—using a Read N System Status Registers command—in order to compare against an archival copy of configuration data. The user may also download both configurations without checking.

4. In either case, it is the responsibility of the configuring device to negate the I/O Configuration Request when reconfiguration is complete. This is done by writing the value 85 (55 Hex) to location 2047 in the System Status Table using a Write N System Status Registers command.

NOTE
Remember, this procedure should be used when the reconfiguration process is fully completed. If both I/O and Control Processor Module (CPM) configurations are done, or if I/O configuration is done in multiple steps, all operations must be finished before the I/O Configuration Request is negated.

Figure 41 illustrates an example of the correct procedures.
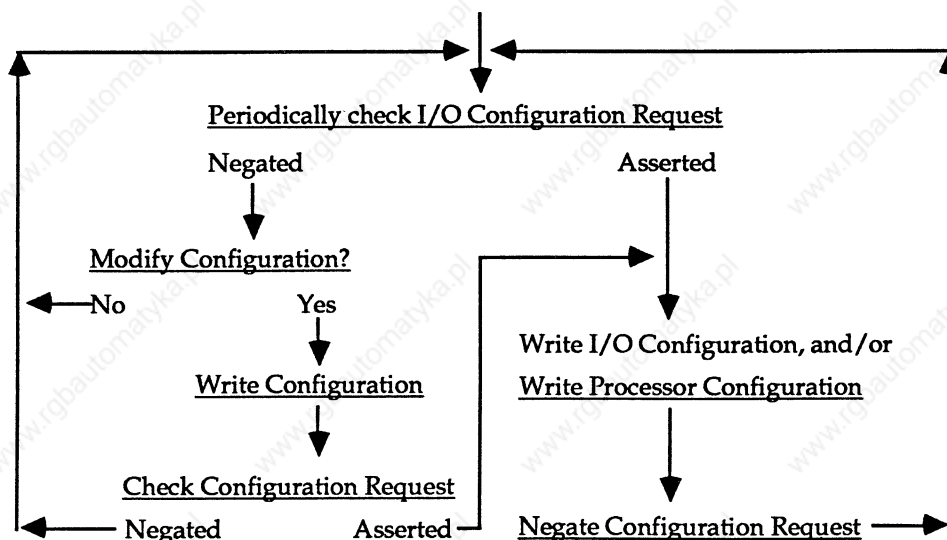
FIGURE 41 - EXAMPLE PROCEDURE FOR CONFIGURING THROUGH THE COMMUNICATION PORT OR CIM

READING THE CONFIGURATION
THROUGH THE COMMUNICATION PORT
OR 620-0048/0052 DATA COLLECTION MODULES

The I/O and CPM configuration data for the 620-11/14/16 LCSs resides in the System Status Table. (See Appendix III of this manual.) The user has access to this information through the Read N System Status Registers command. Following is a list of the locations of the various items within the Status Table that are associated with Logic Controller configuration.

0004　System Error (1 byte)

　　　　Bit 7 = Not used
　　　　Bit 6 = 1 = CPM configuration invalid
　　　　Bit 5 = 1 = Attempt to RUN without I/O
　　　　　　　　　configuration
　　　　Bit 4 = 1 = Attempt to RUN with low battery
　　　　Bits 3, 2, 1, 0 = Not used


```
        7       4   3       0
1904 | SLOT 1  | SLOT 0  |   ▲
     |         |         |   |
     |         |         |  Local
     |         |         |   I/O
1913 | SLOT 19 | SLOT 18 |   ▼
1914 | SLOT 21 | SLOT 20 |   ▲
     |         |         |   |
     |         |         |  Future
     |         |         |   I/O
2041 | SLOT 275| SLOT 274|   ▼
```

Bits 7, 6, 5, 4, 3, 2, 1, 0 = 0000 = 0-point
　　　　　　4,　　　　　0001 = 8=point
　　　　　　　　　　　　0010 = 16=point
　　　　　　　　　　　　0011 = 32-point
　　　　　　　　　　　　0100 = invalid
　　　　　　　　　　　　0101 = invalid
　　　　　　　　　　　　0110 = invalid
　　　　　　　　　　　　0111 = SLM (slot 7 only)
　　　　　　　　　　　　1xxx = invalid
　　　　　　　　　　　　　　n/a

NOTE

Slots 0 through 19 are the only slots presently applicable for configuration in the 620-11/14/16 Logic Controller System. Slots 20 through 275 are reserved for future expansion and are defaulted by the CPM to 0-point slots at power-up. However, these bytes are included in the CPM's diagnostic checksum of the I/O Configuration Table and any corruption of data in this area will cause the CPM to request a reconfiguration. (See the Control Processor Module Configuration Through the Communication Port or 620-0048/0052 Data Collection Modules section in this Appendix for more information.)

2042　Control Processor Module Configuration
　　　　(1 byte)

　　　　Bits 7, 6 = Not used
　　　　Bit 5 = Scan Loss Timer = 0 = disabled
　　　　　　　　　　　　　　　　1 = enabled
　　　　Bit 4 = Data Change Function = 0 = disabled
　　　　　　　　　　　　　　　　　1 = enabled
　　　　Bit 3 = Scan w/ Low Battery = 0 = disabled
　　　　　　　　　　　　　　　　　1 = enabled
　　　　Bit 2 = Output Status in
　　　　　　　Prgm/Disable Modes = 0 = freeze
　　　　　　　　　　　　　　　　1 = clear
　　　　Bit 1 = Force Function = 0 = disabled
　　　　　　　　　　　　　　1 = enabled
　　　　Bit 0 = RUN Mode Programming = 0 = disabled
　　　　　　　　　　　　　　　　　1 = enabled

2047　I/O Configuration Request (1 byte)

　　　　Data = 170 (AA Hex) = Control Processor
　　　　Module requests reconfiguration.
　　　　(See Control Processor Module Configuration
　　　　Through the Communication Port or 620-0048/0052 Data Collection Modules section
　　　　in this Appendix for more information).

WRITING TO THE SYSTEM STATUS TABLE THROUGH THE COMMUNICATION PORT OR 620-0048/0052 DATA COLLECTION MODULES

The following locations in the System Status Table apply to users exercising the Write N System Status Registers command.

2047   I/O Configuration Request (1 byte)

   Data = 85 (55 Hex) = Reconfiguration of the CPM is complete.

   (See CPM Configuration Through the Communication Port or 620-0048/0052 Data Collection Modules section in this Appendix for more information).

2493   Communication Port Configuration (3 bytes)
2492
2491

The built-in communication port may be configured through the port itself or a 620-0048/0052 Module by writing to these locations in the System Status Table.

See the Port Configuration Sequence Through the communication port and 620-0048/0052 Data Collection Modules section in this Appendix for full definitions of the configuration data.

2502   Top Flag Address (2 bytes)
2501

The communication port and 620-0048/0052 Modules monitor a block of 16 single-bit addresses for OFF-to-ON transitions. The user may write to System Status Registers 2501 (LSB) and 2502 (MSB) to define the most significant address of the flag area.

The address must be in the range:
$15 \leq Address \leq 4095$.

TABLE 23 - ASCII TO DECIMAL CONVERSION

	0	1	2	3	4	5	6	7	8	9
0	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT
1	LF	VT	FF	CR	SO	SI	DLE	DC1	DC2	DC3
2	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS
3	RS	US	SP	!	"	#	$	%	&	'
4	(	)	*	+	,	-	.	/	0	1
5	2	3	4	5	6	7	8	9	:	;
6	<	=	>	?	@	A	B	C	D	E
7	F	G	H	I	J	K	L	M	N	O
8	P	Q	R	S	T	U	V	W	X	Y
9	Z	[	\	]	^	_	'	a	b	c
10	d	e	f	g	h	i	j	k	l	m
11	n	o	p	q	r	s	t	u	v	w
12	x	y	z	{	:	}	~	DEL		

TABLE 24 - INSTRUCTION SET OPCODES FOR USE BY COMMUNICATION PORT

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21	20	19	18	17	16	15 - - - - - - - - - - - - - - - 0
Input Status Scan	8F	1	0	D	F	1	1	1	1	32767 Dec./7FFF Hex.
No Operation	FF	1	1	1	1	1	1	1	1	32767 Dec./7FFF Hex.
Bit Read	03	0	0	0	0	0	0	1	1	Address and Bit No. (14)
Normally Open Contact										
No Packed Down Branches	C8	1	1	D	F	1	0	0	0	Address
One Packed Down Branch	C9	1	1	D	F	1	0	0	1	Address
Two Packed Down Branches	CA	1	1	D	F	1	0	1	0	Address
Normally Closed Contact										
No Packed Down Branches	CC	1	1	D	F	1	1	0	0	Address
One Packed Down Branch	CD	1	1	D	F	1	1	0	1	Address
Two Packed Down Branches	CE	1	1	D	F	1	1	1	0	Address
Not	CB	1	1	0	0	1	0	1	1	Address
Transition ON Contact	43	0	1	D	F	0	0	1	1	Address (3)
Transition OFF Contact	4B	0	1	D	F	1	0	1	1	Address (3)
Branch (three internal instructions)										
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Double-Down Branch	C2	1	1	0	0	0	0	1	0	Not Used
Up Branch	C3	1	1	0	0	0	0	1	1	32767 Dec./7FFF Hex.
Output	C4	1	1	D	F	0	1	0	0	Address
Retentive Output	C5	1	1	D	F	0	1	0	1	Address
Latch Output	C6	1	1	D	F	0	1	1	0	Address
Unlatch Output	C7	1	1	D	F	0	1	1	1	Address
Bit Write	85	1	0	D	F	0	1	0	1	Address and Bit No. (14)
F. P. Constant in LS Register	9B	1	0	0	1	1	0	1	1	Address
F. P. Constant in MS Register	AB	1	0	1	0	1	0	1	1	Address
F. P. Bring In	A8	1	0	1	0	1	0	0	0	Address
F.P. Send Out	27	0	0	1	0	0	1	1	1	Address
Bring In	88	1	0	0	0	1	0	0	0	Address
Send Out	7	0	0	D	F	0	1	1	1	Address (7)
Constant	8B	1	0	0	0	1	0	1	1	Data
Indirect Bring In	89	1	0	0	0	1	0	0	1	Address
Indirect Send Out	06	0	0	0	0	0	1	1	0	Address
Pull from I/O	80	1	0	0	0	0	0	0	0	Registers (8) Address
Pull from Status Table	81	1	0	0	0	0	0	0	1	Registers (8) Offset (9)
Pull from Registers	82	1	0	0	0	0	0	1	0	Registers (8) Offset (9)
Push to I/O	84	1	0	0	0	0	1	0	0	Registers (8) Address
Push to Registers	86	1	0	0	0	0	1	1	0	Registers (8) Offset (9)
End Of Memory	30	0	0	1	1	0	0	0	0	32768 Dec./8000 Hex.
Not Skip and Retain	46	0	1	D	F	0	1	1	0	0 - 0, label
Not Skip and De-energize	47	0	1	D	F	0	1	1	1	0 - 0, label (5)
End of Skip	34	0	0	1	1	0	1	0	0	0 - 0, label
Jump	46	0	1	D	F	0	1	1	0	0 - 0, label (6)
Return to Beg. of Program	5	0	0	D	F	0	1	0	1	32767 Dec./7FFF Hex.
Delay	CF	1	1	0	0	1	1	1	1	Address

Notes begin at the end of the table.

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21	20	19	18	17	16	15 ---------------------- 0
On Delay Timer										
Word 1: (.01 sec.)	68	0	1	H	0	1	0	0	0	Address of elapsed time (5)
(.1 sec.)	69	0	1	H	0	1	0	0	1	Address of elapsed time (5)
(1 sec.)	6A	0	1	H	0	1	0	1	0	Address of elapsed time (5)
Word 2	C4	1	1	D	F	0	1	0	0	Output Address
Off Delay Timer										
Word 1: (.01 sec.)	60	0	1	H	0	0	0	0	0	Address of elapsed time (4)
(.1 sec.)	61	0	1	H	0	0	0	0	1	Address of elapsed time (4)
(1 sec.)	62	0	1	H	0	0	0	1	0	Address of elapsed time (4)
Word 2	C4	1	1	D	F	0	1	0	0	Output Address
Retentive On Delay Timer										
(.01 sec.)	4C	1	1	H	0	1	1	0	0	Address of elapsed time (4)
(.1 sec.)	6D	0	1	H	0	1	1	0	1	Address of elapsed time (4)
(1 sec.)	6E	0	1	H	0	1	1	1	0	Address of elapsed time (4)
Up/Down Counter	4F	0	1	H	H	1	1	1	1	Addr. - Accumulated Count (4)
Sequencer										
Sequencer Size	8A	1	0	0	0	1	0	1	0	Total # of Step (s) (10)
Step Number Address	8C	1	0	0	0	1	1	0	0	Address
Data Table Step 1	8B	1	0	0	0	1	0	1	1	Data
Control Output Address	07	0	0	0	0	0	1	1	1	Control Output Address
Load Sequencer	44	0	1	0	0	0	1	0	0	Address
Unload Sequencer	45	0	1	0	0	0	1	0	1	Address
Jump to Subroutine (JSR)										
Word 1	04	0	0	0	0	0	1	0	0	Address of zero (MAR)
Word 2	04	0	0	0	0	0	1	0	0	128, Label (11)
Subroutine (SUB)	24	0	0	1	0	0	1	0	0	128. Label (11)
Return to Subroutine (RTS)	14	0	0	0	1	0	1	0	0	128, Label (11)
BCD-BIN Conversion	0F	0	0	0	0	1	1	1	1	Address
BIN-BCD Conversion	1F	0	0	0	1	1	1	1	1	Address
F. P. to Integer Conversion	3F	0	0	1	1	1	1	1	1	Address
Integer to F. P. Conversion	2F	0	0	1	0	1	1	1	1	Address
AND	2C	0	0	1	0	1	1	0	0	Address
OR	2E	0	0	1	0	1	1	1	0	Address
Exclusive OR	3E	0	0	1	1	1	1	1	0	Address
Absolute Value	1C	0	0	0	1	1	1	0	0	Address
F. P. Square Root	2D	0	0	1	0	1	1	0	1	Address
Invert (1's Complement)	1D	0	0	0	1	1	1	0	0	Address
Negate (2's Complement)	1E	0	0	0	1	1	1	1	0	Address
Addition	0E	0	0	0	0	1	1	1	0	32767 Dec./7FFF Hex.
Subtraction	0D	0	0	0	0	1	1	0	1	32767 Dec./7FFF Hex.
Multiplication	0C	0	0	0	0	1	1	0	0	32767 Dec./7FFF Hex.
Division	0B	0	0	0	0	1	0	1	1	32767 Dec./7FFF Hex.
Equality Comparison	08	0	0	0	0	1	0	0	0	32767 Dec./7FFF Hex.
Less Than Comparison	09	0	0	0	0	1	0	0	1	32767 Dec./7FFF Hex.
Greater Than Comparison	0A	0	0	0	0	1	0	1	0	32767 Dec./7FFF Hex.
Test for Zero	8D	1	0	D	F	1	1	0	1	Address

Notes begin at the end of the table.

INSTRUCTION	HEX VALUE	BINARY VALUE								ADDRESSES AND ASSOCIATED DATA
		BITS								
		23	22	21	20	19	18	17	16	15 - - - - - - - - - - - - - 0
Matrix (Sequenced by operation)										
MOVE, INVERT										
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Zero
Operator	AE	1	0	1	0	1	1	1	0	Operator
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address
OR, AND, XOR										
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Operator
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address
SET 0, SET 1										
Set 0 Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Set 1 Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Operator (13)
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address
Compare										
Address/Bit Contact		Contact Opcode								Address
Down Branch	C1	1	1	0	0	0	0	0	1	Not Used
Enable Contact		Contact Opcode								Address
Size	88	1	0	0	0	1	0	0	0	Address
Source Matrix (Matrix A)	8E	1	0	0	0	1	1	1	0	Address
Reference Matrix (Matrix B)	9E	1	0	0	1	1	1	1	0	Address
Operator	AE	1	0	1	0	1	1	1	0	Operator (13) (12)
Destination Matrix (Matrix C)	BE	1	0	1	1	1	1	1	0	Address

Notes begin at the end of the table.

Table 24 Notes:

1. An F in bit 20 denotes a force bit that indicates if the force is ON or OFF. A D in bit 21 denotes a data bit that indicates the status of the force bit in the ON state. Note that a normally open contact has a power flow in the closed position while a normally closed contact has a power flow in the open position.

STATUS	BIT	
	20	21
1	FORCE	CLOSED
0	NO FORCE	OPEN

2. Bits 0-15 contains the hex value 7FFF (32767 Dec.) when not used by the instruction.

3. Bit 21 indicates the status of the instruction from the previous scan when the force (bit 20) is OFF. A "1" indicates that the instruction was ON from the previous scan.

4. An H in bit 21 is the time base history for timers and counters. A positive transition on bit 21 causes an increment of the count or time. A positive transition on bit 20 of the up/down counter causes a decrement of the count.

5. Bit 20 is a history bit that indicates the state of the element on the previous scan. If it is set to 1, then succeeding executions will be treated as a Skip and Retain.

6. A Jump to EOS has a label within the range of 8192 to 8447. An Indirect Jump to an EOS has a label of 8448. A Jump to a program line has a label of 8449.

7. Bits 20 and 21 indicate the forced state of the send out. Both bits are set to 1 when the instruction is forced. The forced send out will be treated as a No Operation (NOP) on succeeding scans.

8. Bits 13-15 contain a binary representation (x) where the value $x + 1$ is the number of registers to be used (0 = 1 register, 7 = 8 registers).

9. Bits 0-12 contain a binary representation of the address offset for both PUSH and PULL instructions.

    Status Table Address = Status Table Offset + 2048
    Register Address = Register Offset + 4096

    If Status Table Address ≤ 2047, then Status Table Offset = Status Table Address + 2048

    If Status Table Address > 2047 (max. value 4095) then Status Table Offset = Status Table Addr. - 2048

    Example:

2291	Instruction's Memory Word		
[PUL]	1000 0001	000 0 0000	1111 0011
1	opcode	register	offset

    offset = 243   Address: 243 + 2048 = 2291

10. Bits 0-15 contain a binary representation of the number of steps. Bits 11-15 contain zeros.

11. Bits 0-7 contain a binary representation of the label. Bits 8-15 contain a binary representation of 128 (80 Hex).

12. Operators are located in bits 0-15.

13.
OPERATOR	DECIMAL EQUIVALENT
MOVE	0
INVERT	2
OR	4
AND	6
XOR	8
SET 0, SET 1	10
COMPARE	12

Table 24 Notes (Continued):

14. Bit Read and Bit Write

Specifies one of eight bits in byte
specified by contents of bø

Ø - 7

Register Address*

b23   b16 b15   b13   ←12 bits→   bø

*Lowest 12 bits of Register Address

VECTOR

Register Data at
Address Specified

| MSB | LSB |

Byte Select Bit

0 - MSB
1 - LSB

For example:

```
       5001
For  —|BR|—          b₁₃ - b₁₅ . . . 001
        1
```
$b_{13} - b_{15} \ldots 001$

$b_{12} - b_1 \ldots 0011\ 1000\ 1001$

$b\text{ø} \ldots 1$

```
       5001
For  —|BR|—          b₁₅ - b₁₃ . . . 001
        1
```
$b_{15} - b_{13} \ldots 001$

$b_{12} - b_1 \ldots 0011\ 1000\ 1001$

$b\text{ø} \ldots \text{ø}$
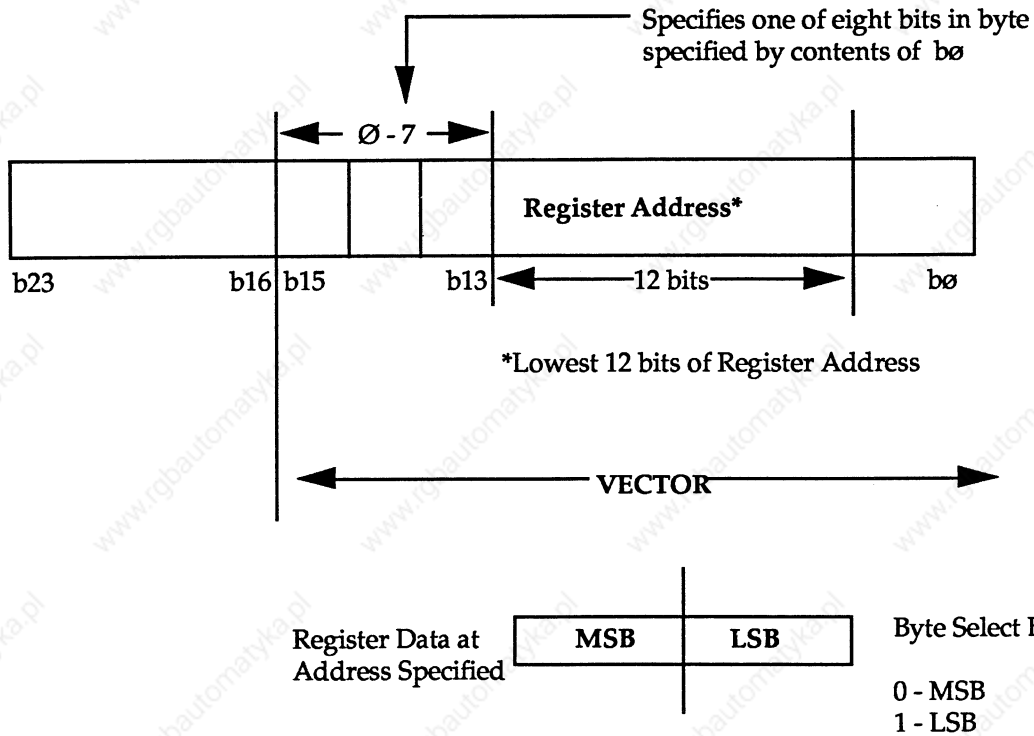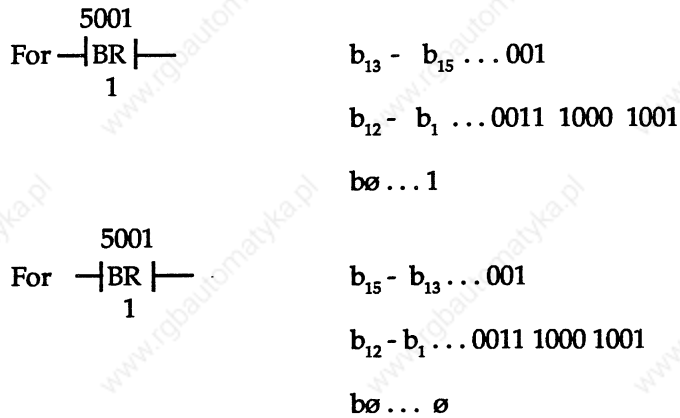
APPENDIX III

SYSTEM STATUS INFORMATION

The following is a list of 8-bit address registers and the system status information that they contain.

SYSTEM DIAGNOSTIC STATUS

2488	21845 = No ARMP in progress
2487	43690 = ARMP in progress
2470	Control Relay Size MSB (before usage of real I/O)
2469	LSB
2468	Real I/O Size MSB
2467	LSB
2466	Register Size MSB
2465	LSB
2432	Model # (BCD) (Except 620-10/15/20/30)
2431	Card Fault Address 1 MSB
2430	LSB
2429	Card Fault Address 2 MSB
2428	LSB
2427	Card Fault Address 3 MSB
2426	LSB
2425	Card Fault Address 4 MSB
2424	LSB
2423	Card Fault Address 5 MSB
2422	LSB
2421	Card Fault Address 6 MSB
2420	LSB
2419	Card Fault Address 7 MSB
2418	LSB
2417	Card Fault Address 8 MSB
2416	LSB
2415	Card Fault Count MSB
2414	LSB
2413	Scan Loss (Scan Loss = 0; Valid Scan = 128)
2412	Battery (Bad = 0; Good = 128)
2411	PM (Fail = 0; Pass = 128)
2408	Motherboard ID (Correct - 128)
2404	Option Card CIM or CNM (see NOTE 2)
2403	Option Card CIM or CNM (see NOTE 2)
2402	Option Card CIM or CNM (see NOTE 2)
2401	Option Card CIM or CNM (see NOTE 2)
2399	Control Network Status Bits, Option Card 1
2398	Control Network Status Bits, Option Card 2
2397	Control Network Status Bits, Option Card 3
2396	Control Network Status Bits, Option Card 4

2395	PC Checksum MSB
2394	LSB
2393	PC Checksum Error Flag MSB (0=no error, 1=error)
2392	LSB (not used)
2391	PC Initial Checksum Flag - System Use Only
2390	PC Initial Checksum Pass Flag (0=initial checksum calculation in progress) (1=initial checksum complete)
2318	Option Card Fault Bits 1, CIM/CNM
2317	Option Card Fault Bits 2, CIM/CNM
2316	Option Card Fault Bits 3, CIM/CNM
2315	Option Card Fault Bits 4, CIM/CNM

SYSTEM HARDWARE STATUS

2303	Processor Type: 0 = 620-10
	1 = 620-06, -11, -14, -15, -16
	2 = 620-20
	3 = 620-25, -35
2302	Revision Level (≥64 in the 620-11/14/16)
2299	Memory Size MSB
2298	LSB
2297	Memory Used MSB
2296	LSB
2295	Force Count MSB
2294	LSB
2293	0 MSB
2292	Baud Rate LSB
2291	0 MSB
2290	Scan Time LSB
2287	Software Request for Program MSB
2286	LSB
2284	Memory Type (EPROM = 128; Fail = 255)
2275	Option Card 1 ID
2274	Option Card 2 ID
2273	Option Card 3 ID
2272	Option Card 4 ID

SYSTEM IDENTIFICATION

2175	ASCII Bit Pattern for Program Date
2170	
2169	ASCII Bit Pattern for Programmer
2144	
2143	ASCII Bit Pattern for Program Title
2048	

For 620-11/14/16 Models:

2502	MSB	Top Address of Flag Bit Area
2501	LSB	

2499	System Status Table Size (Hex)
2498	Firmware Revision (Hex)
2497	Firmware Version (Hex)
2496 - 2491	Communication Port Configuration

2047   I/O Configuration Request
              85 - I/O is configured
              170 - Reconfiguration requested

2043   Ø
2042   Processor Control Configuration

2041 - 1904 I/O Configuration Table

0013	MSB	Executive ROM Check Code
0012	LSB	

0004   System Error Word

0003	MSB	0.01 Timebase Counter History for Last Scan
0002	LSB	

0001	MSB	0.01 Timebase Counter
	LSB	

NOTE
11111111 Component Not Present
00000001 CIM Present & Failed
10000001 CIM Present & Passed
00000010 CNM Present & Failed
10000010 CNM Present & Passed

The following 8- byte block is reserved for on-board communication port transaction records, <u>and applies only to the 620-11, 620-14, and 620-16.</u> The format varies depending on the protocol being used. Each count is comprised of two status table locations, which should be interpreted as a 16-bit word with a binary range of 0 - 65,535.

ABC PROTOCOL

2511 -	MSB	Receive Message Count
2510 -	LSB	

2509 -	MSB	Transmit Message Count
2508 -	LSB	

2507 -	MSB	Receive Error Count
2506 -	LSB	

2505 -	MSB	Invalid Message Count
2504 -	LSB	

MODBUS RTU

2507 -	MSB	Valid Message Count
2506 -	LSB	

2505 -	MSB	Event Count
2504 -	LSB	

Please note that in the case of word-wide registers, the least significant byte is located in the System Status Table byte with the lower address, the most significant in the higher address.

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