

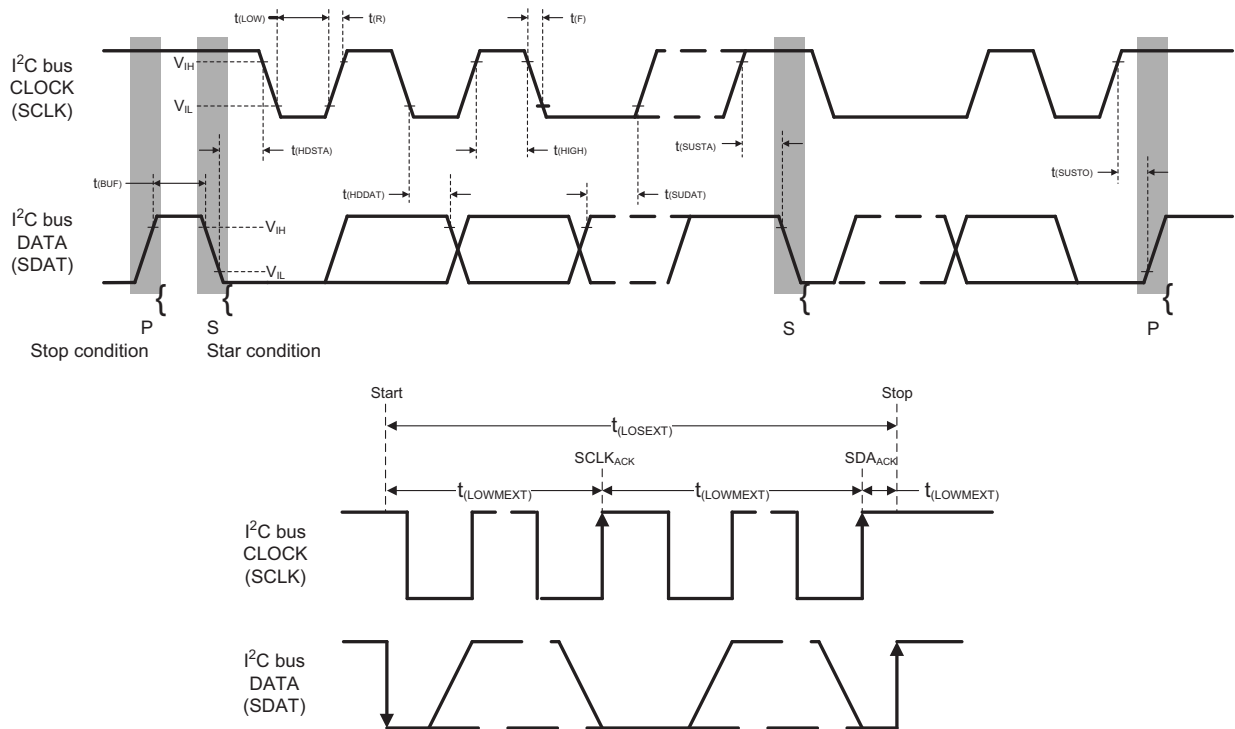


<b>BASIC CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)							
PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Supply voltage		$V_{DD}$	2.5	-	3.6	V	
Supply current	Excluded LED driving	$I_{DD}$	-	300	-	$\mu\text{A}$	
	Light condition = dark, $V_{DD} = 3.3\text{ V}$	$I_{DD}(\text{SD})$	-	0.2	-	$\mu\text{A}$	
I <sup>2</sup> C supply voltage		$V_{PULL\ UP}$	1.8	-	5.0	V	
ALS shut down	ALS disable, PS enable	$I_{ALSSD}$	-	200	-	$\mu\text{A}$	
PS shut down	ALS enable, PS disable	$I_{PSSD}$	-	260	-	$\mu\text{A}$	
I <sup>2</sup> C signal input	Logic high	$V_{DD} = 3.3\text{ V}$	$V_{IH}$	1.55	-	-	V
	Logic low		$V_{IL}$	-	-	0.4	
	Logic high	$V_{DD} = 2.6\text{ V}$	$V_{IH}$	1.4	-	-	V
	Logic low		$V_{IL}$	-	-	0.4	
Peak sensitivity wavelength of ALS		$\lambda_p$	-	550	-	nm	
Peak sensitivity wavelength of PS		$\lambda_p$	-	850	-	nm	
Full ALS counts	16-bit resolution		-	-	65 535	steps	
Full PS counts	12-bit / 16-bit resolution		-	-	4096 / 65 535	steps	
ALS sensing tolerance	White LED light source		-	-	$\pm 10$	%	
Detectable intensity	Minimum	IT = 800 ms, 1 step <sup>(1)(2)</sup>	-	0.004	-	lx	
	Maximum	IT = 50 ms, 65 535 step <sup>(1)(2)</sup>	-	4192	-		
ALS dark offset	IT = 50 ms, normal sensitivity <sup>(1)</sup>		0	-	3	steps	
PS detection range	Kodak gray card <sup>(3)</sup>		0	-	500	mm	
Operating temperature range		$T_{amb}$	-40	-	+105	$^{\circ}\text{C}$	
Cathode (sensor) voltage			2.5	-	3.6	V	
IRED driving current	<sup>(4)</sup>		-	-	200	mA	

**Notes**

- <sup>(1)</sup> Test condition:  $V_{DD} = 3.3\text{ V}$ , temperature:  $25\text{ }^{\circ}\text{C}$
- <sup>(2)</sup> Maximum detection range to ambient light can be determined by ALS refresh time adjustment. Refer to table "ALS Resolution and Maximum Detection Range"
- <sup>(3)</sup> Depending on external IRED
- <sup>(4)</sup> Based on IRED on / off duty ratio = 1/40, 1/80, 1/160, and 1/320

<b>I<sup>2</sup>C BUS TIMING CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	$\mu\text{s}$
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	$\mu\text{s}$
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	$\mu\text{s}$
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	$\mu\text{s}$
Data hold time	$t_{(HDDAT)}$	-	3450	-	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I <sup>2</sup> C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	$\mu\text{s}$
I <sup>2</sup> C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	$\mu\text{s}$
Clock / data fall time	$t_{(F)}$	-	300	-	300	ns
Clock / data rise time	$t_{(R)}$	-	1000	-	300	ns


 Fig. 1 - I<sup>2</sup>C Bus Timing Diagram