

*Advance Information*  
**32K x 8 Bit CMOS Static Random Access Memory**  
**Extended Temperature Range: -40 to 85°C**

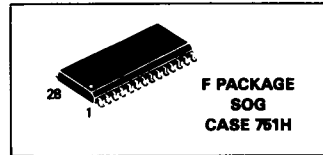
The MCM60L256A-C is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the cycle time is 100 ns. For long cycle times (>100 ns), the automatic power down (APD) circuitry will temporarily shut down various power consuming circuits, thereby reducing the active power consumption.

Chip enable ( $\bar{E}$ ) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When  $\bar{E}$  is a logic high, the part is placed in low power standby mode. The maximum standby current is 2  $\mu$ A ( $T_A=25^\circ\text{C}$ ). Chip enable also controls the data retention mode. Another control feature, output enable ( $\bar{G}$ ) allows access to the memory contents as fast as 50 ns. Thus the MCM60L256A-C is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

The MCM60L256A-C is offered in a 28 pin 330 mil gull-wing SO package.

- Single 5 V Supply,  $\pm 10\%$
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strokes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Output Enable and Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (Maximum Standby Current=2  $\mu$ A @ 25°C)
- Data Retention Supply Voltage=2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Time: MCM60L256A-C10=100 ns (Max)

**MCM60L256A-C**



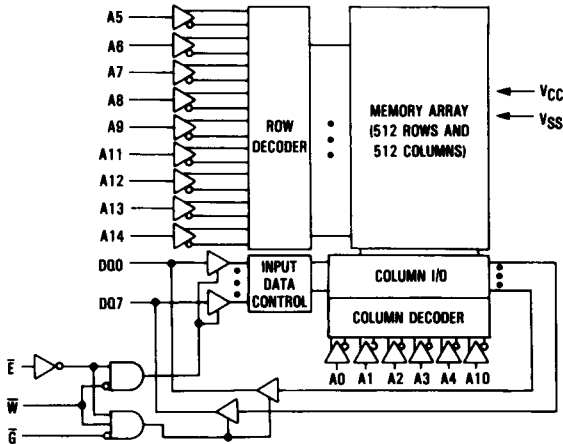
**PIN ASSIGNMENT**

A14	1	28	VCC
A12	2	27	W
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\bar{G}$
A2	8	21	A10
A1	9	20	$\bar{E}$
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
VSS	14	15	DQ3

**PIN NAMES**

A0-A14	Address
W	Write Enable
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
DQ0-DQ7	Data Input/Output
VCC	+5 V Power Supply
VSS	Ground

**BLOCK DIAGRAM**



This document contains information on a new product. Specifications and information herein are subject to change without notice.

**TRUTH TABLE**

$\bar{E}$	$\bar{G}$	$\bar{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	$I_{SB}$	High Z
L	H	H	Output Disabled	$I_{CC}$	High Z
L	L	H	Read	$I_{CC}$	$D_{out}$
L	X	L	Write	$I_{CC}$	$D_{in}$

X = don't care

**ABSOLUTE MAXIMUM RATINGS (See Note)**

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	-0.3 to +7.0	V
Voltage to Any Pin with Respect to $V_{SS}$	$V_{in}, V_{out}$	-0.5 to $V_{CC} + 0.5$	V
Power Dissipation ( $T_A = 25^\circ\text{C}$ )	SOG $P_D$	0.6	W
Operating Temperature	$T_A$	-40 to +85	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

**DC OPERATING CONDITIONS AND CHARACTERISTICS**

( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$ , Unless Otherwise Noted)

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3*	—	0.8	V

\* $V_{IL}$  (min) = -0.3 V dc;  $V_{IL}$  (min) = -3.0 V ac (pulse width  $\leq 50$  ns)

**DC CHARACTERISTICS**

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to $V_{CC}$ )	$I_{kg(I)}$	—	<0.01	$\pm 1.0$	$\mu\text{A}$
Output Leakage Current ( $\bar{E} = V_{IH}$ or $\bar{G} = V_{IH}$ or $\bar{W} = V_{IL}$ , $V_{out} = 0$ to $V_{CC}$ )	$I_{kg(O)}$	—	<0.01	$\pm 1.0$	$\mu\text{A}$
Operating Current (Read Cycle) ( $\bar{E} = V_{IL}$ , $\bar{W} = V_{IH}$ , Other Input = $V_{IH}/V_{IL}$ , $I_{out} = 0$ mA) $t_{AVQV} = 1\ \mu\text{s}$ $t_{AVQV} = 100$ ns	$I_{CCA1}$	—	10	15 70	mA
	$I_{CCA2}$	—	5	8 60	
Standby Current ( $\bar{E} = V_{IH}$ )	$I_{SB1}$	—	—	3.0	mA
Standby Current ( $\bar{E} \geq V_{CC} - 0.2\text{ V}$ , $V_{CC} = 2.0$ to $5.5\text{ V}$ ) ( $T_A = 25^\circ\text{C}$ )	$I_{SB2}$	—	2	100	$\mu\text{A}$
		—	—	2	
Output Low Voltage ( $I_{OL} = 4.0$ mA)	$V_{OL}$	—	—	0.4	V
Output High Voltage ( $I_{OH} = -1.0$ mA)	$V_{OH}$	2.4	—	—	V

Typical values are referenced to  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V}$

**CAPACITANCE (f = 1 MHz,  $T_A = 25^\circ\text{C}$ , Periodically Sampled Rather Than 100% Tested)**

Characteristic	Symbol	Min	Max	Unit
Input Capacitance ( $V_{in} = 0\text{ V}$ )	All Inputs Except DQ $C_{in}$	—	10	pF
I/O Capacitance ( $V_{I/O} = 0\text{ V}$ )	DQ $C_{I/O}$	—	10	pF

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

## AC OPERATING CONDITIONS AND CHARACTERISTICS

( $V_{CC} = 5.0 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 85^\circ\text{C}$ , Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V  
 Input Rise/Fall Time . . . . . 5 ns  
 Input Timing Measurement Reference Levels . . . . . 1.5 V

Output Timing Measurement Reference Levels . . . . . 0.8 and 2.2 V  
 Output Load . . . . . See Figure 1

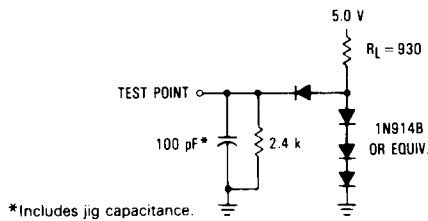
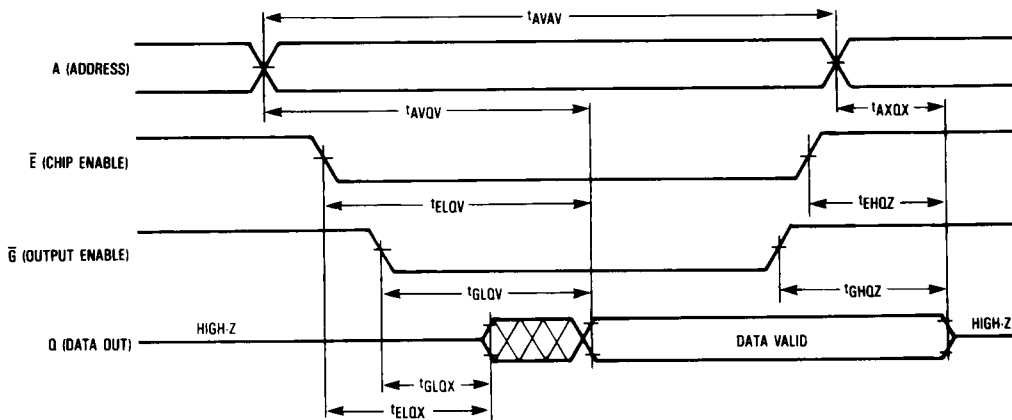
### READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Read Cycle Time	$t_{AVAV}$	$t_{RC}$	100	—	ns	—
Address Access Time	$t_{AVQV}$	$t_{AA}$	—	100	ns	—
$\bar{E}$ Access Time	$t_{ELQV}$	$t_{AC}$	—	100	ns	—
$\bar{G}$ Access Time	$t_{GLQV}$	$t_{OE}$	—	50	ns	—
Output Hold from Address Change	$t_{AXQX}$	$t_{OH}$	10	—	ns	—
Chip Enable to Output Low-Z	$t_{ELQX}$	$t_{CLZ}$	10	—	ns	2, 3
Output Enable to Output Low-Z	$t_{GLQX}$	$t_{OLZ}$	5	—	ns	2, 3
Chip Enable to Output High-Z	$t_{EHQZ}$	$t_{CHZ}$	0	35	ns	2, 3
Output Enable to Output High-Z	$t_{GHQZ}$	$t_{OHZ}$	0	35	ns	2, 3

#### NOTES:

- $\bar{W}$  is high at all times for read cycles.
- All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 100 mV transition from the previous steady state voltage.
- These parameters are periodically sampled and not 100% tested.

### READ CYCLE



\*Includes jig capacitance.

Figure 1. AC Test Load

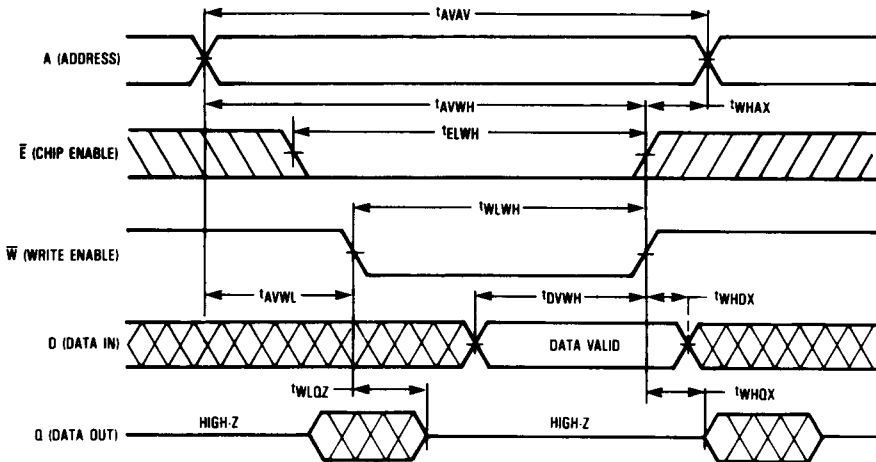
**WRITE CYCLE 1 AND 2 (See Note 1)**

Parameter	Symbol	Alt Symbol	Min	Max	Unit	Notes
Write Cycle Time	$t_{AVAV}$	$t_{WC}$	100	—	ns	—
Address Setup Time	$t_{AVWL}/t_{AVEL}$	$t_{AS}$	0	—	ns	—
Address Valid to End of Write	$t_{AVWH}/t_{AVEH}$	$t_{AW}$	80	—	ns	—
Write Pulse Width	$t_{WLWH}$	$t_{WP}$	60	—	ns	2
Data Valid to End of Write	$t_{DVWH}/t_{DVEH}$	$t_{DW}$	35	—	ns	—
Data Hold Time	$t_{WHDX}/t_{EHDX}$	$t_{DH}$	0	—	ns	—
Write Low to Output in High-Z	$t_{WLOZ}$	$t_{WHZ}$	0	25	ns	3, 4
Write High to Output Low-Z	$t_{WHQZ}$	$t_{WLZ}$	10	—	ns	3, 4
Write Recovery Time	$t_{WHAX}/t_{EHAX}$	$t_{WR}$	0	—	ns	5
Chip Enable to End of Write	$t_{ELWH}/t_{ELEH}$	$t_{CW}$	80	—	ns	—

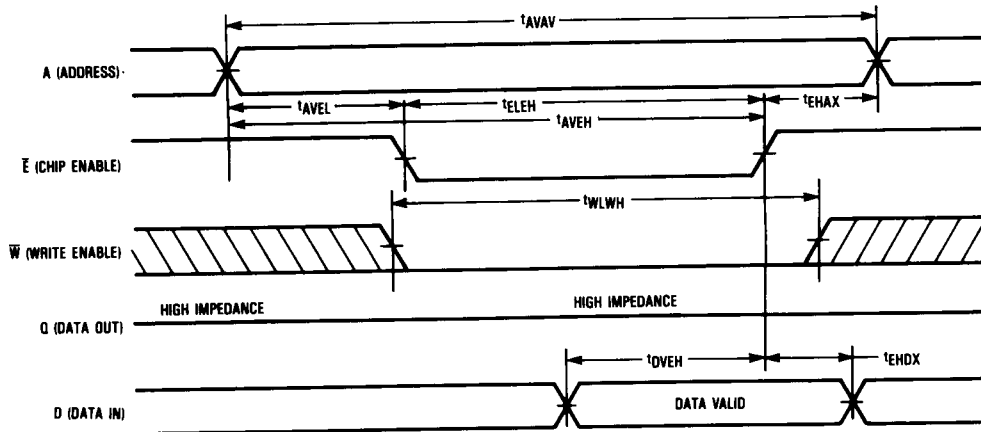
**NOTES:**

1. Outputs are in high impedance state if  $\bar{G}$  is high during Write Cycle.
2. A write occurs during the overlap ( $t_{\overline{WP}}$ ) of a low  $\bar{E}$  and a low  $\bar{W}$ . If  $\bar{W}$  goes low prior to  $\bar{E}$  low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 100 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5.  $t_{\overline{WR}}$  is measured from the earlier of  $\bar{E}$  or  $\bar{W}$  going high to the end of write cycle.

**WRITE CYCLE 1 ( $\bar{W}$  CONTROLLED)**



### WRITE CYCLE 2 ( $\bar{E}$ Controlled)



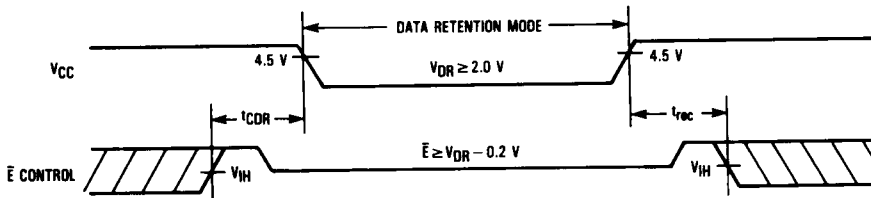
### DATA RETENTION CHARACTERISTICS ( $T_A = -40$ to $85^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
V <sub>CC</sub> for Data Retention ( $\bar{E} \geq V_{CC} - 0.2$ V)	V <sub>DR</sub>	2.0	—	5.5	V
Data Retention Current ( $\bar{E} \geq V_{CC} - 0.2$ V)	I <sub>CCDR</sub>	V <sub>CC</sub> = 3.0 V	—	50	$\mu\text{A}$
		V <sub>CC</sub> = 5.5 V	—	100	
Chip Disable to Data Retention Time	t <sub>CDR</sub>	0	—	—	ns
Operation Recovery Time	t <sub>rec</sub>	t <sub>AVAV</sub> *	—	—	ns

\*t<sub>AVAV</sub> = Read Cycle Time

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### DATA RETENTION MODE



NOTE: If the V<sub>IH</sub> of  $\bar{E}$  is 2.4 V in operation, I<sub>SB1</sub> current flows during the period that the V<sub>CC</sub> voltage is decreasing from 4.5 V to 2.4 V.

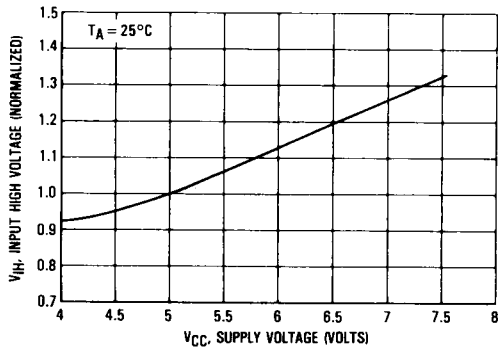


Figure 1. Input High Voltage versus Supply Voltage

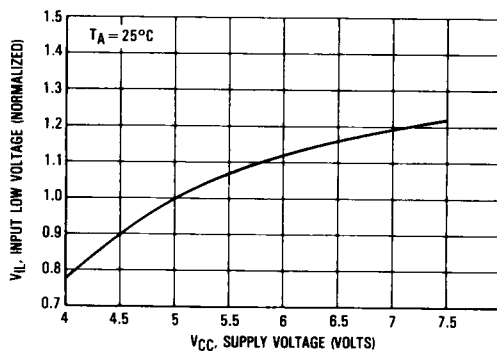


Figure 2. Input Low Voltage versus Supply Voltage

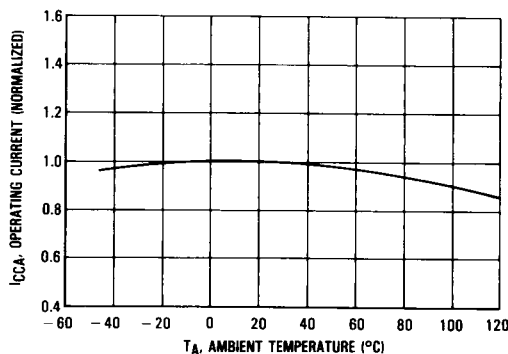


Figure 3. Operating Current versus Ambient Temperature

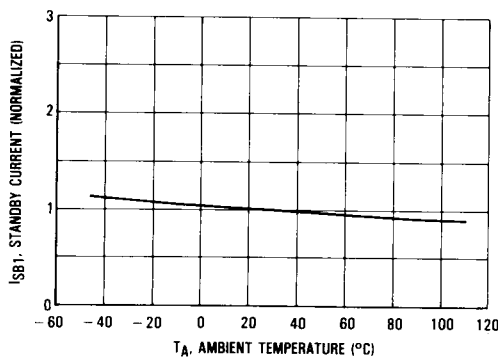


Figure 4. I<sub>SB1</sub> Standby Current versus Ambient Temperature

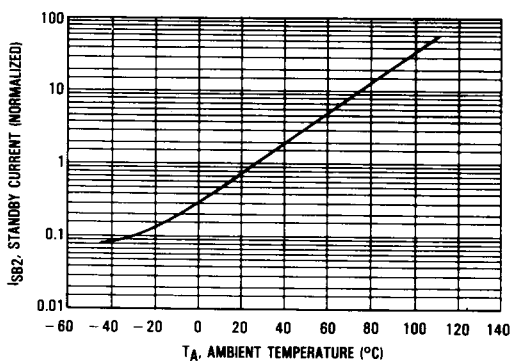


Figure 5. I<sub>SB2</sub> Standby Current versus Ambient Temperature

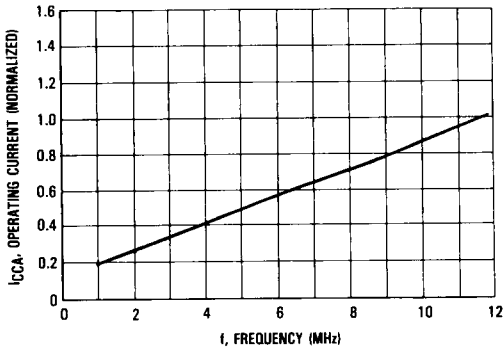


Figure 6. Low Power Operating Current versus Frequency (Read)

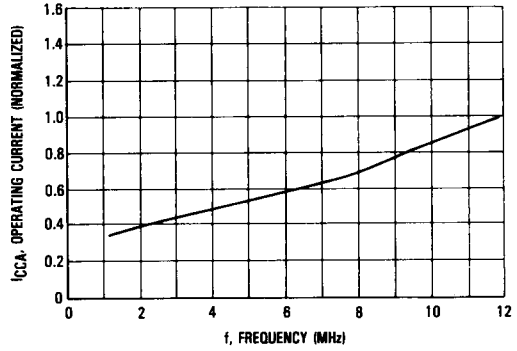


Figure 7. Operating Current versus Frequency (Write)

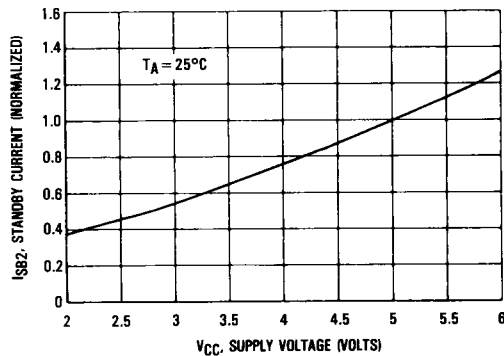


Figure 8. Low Power IBS2 Standby Current versus Supply Voltage

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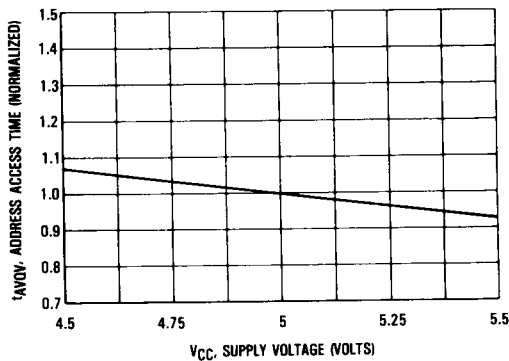


Figure 9. Access Time versus Supply Voltage

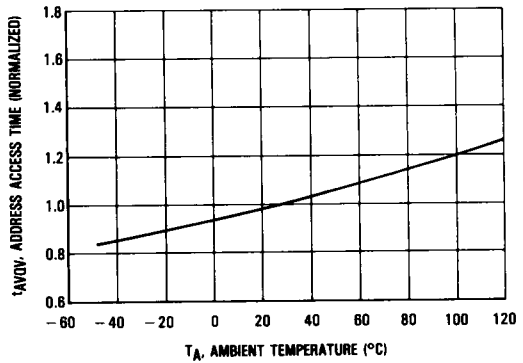
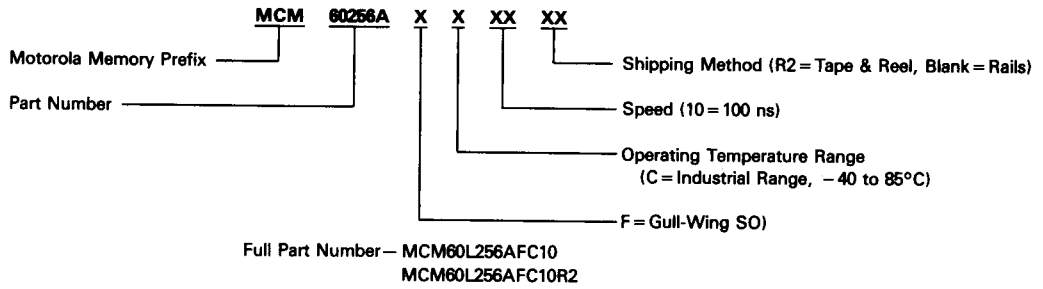


Figure 10. Access Time versus Ambient Temperature

**ORDERING INFORMATION**  
**(Order by Full Part Number)**



NOTE: For mechanical data, please see Chapter 10.