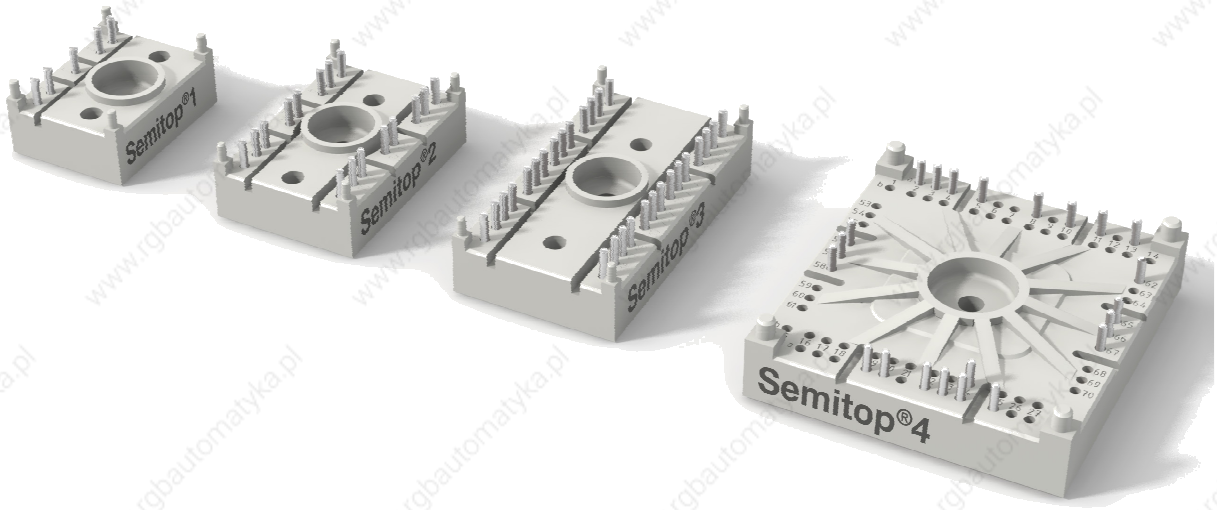
SEMITOP®

THE LOW AND MEDIUM POWER MODULE FOR HIGH INTEGRATED APPLICATIONS



Version 2
January 2008

Marco Di Lella - Riccardo Ramin

SEMITOP® TECHNICAL INFORMATION

1 Introduction

Great thermal management performance, high reliability and easy mounting were the design goals reached with the SEMITOP® family when it was introduced in the market in the late 90's. Nowadays SEMITOP® family confirms to be the best alternative solution for all the applications where performance, reliability, integration and costs are a must.

1.1 The SEMITOP® concept

SEMITOP® are base plate less modules, that means they are made by direct soldering of the silicon chips and the power terminals on a ceramic substrate. The ceramic substrate is packaged with a plastic housing and the whole assembly is then pressed and fixed to the heatsink by a single mounting screw.
The SEMITOP® pressure technology and the single mounting screw guarantee:

- the lowest Rthjs
- a mechanical stress free design

which allow to get:

- a SUPERIOR Power Cycle Capability
- an extremely HIGH Reliability

1.2 Features

- One screw
- Base plate less design
- Rugged pins for PCB solder assembly
- High insulation degree (2,5kV AC 1min / 3kV DC 1s)
- Only 12 mm height
- Complete product line covering a continuous current from 20A to 200A in 600V and from 8A to 100A in 1200V

1.3 Customer Advantages and Benefits

- One screw mounting for an Easy, Fast and Reliable assembly
- Modules for automatic PCB soldering
- UL recognized
- The best possible thermal resistance:
  - up to 30% lower compared isolated discrete TOs
  - up to 18% lower compared to IMS substrates
- Integration lead to compact design, space savings, mounting cost saving

With only 12mm height, SEMITOP® is a *compact isolated power module* for *PCB soldering* offering a wide platform integrating several chip technologies as well as several circuit topologies such as CIB (up to 100A/600V and 50A/1200V), 6-pack (up to 200A/600V and 100A/1200V), Input Bridge Rectifier, AC switches, double PFC topologies or Single leg for Multilevel Inverters.

A complex circuit can be quickly assembled by just *one mounting screw* to the heatsink and then automatically soldered to the PCB. Standard FR4 PCB material as well as lead free solder materials are suitable for the assembly.

The single central mounting screw provides an even pressure distribution which guarantees low thermal resistance resulting in low junction temperature and high reliability.
The reliability performances are confirmed by an extensive qualification program consisting in 17 different qualification and reliability tests performed for more than 10000h.

1.4 New technologies: Multi Level Inverter

SEMIKRON further expands the SEMITOP® family enlarging the application product range by introducing a ***new product family to implement multilevel inverter applications for DC/AC conversion.***

Multilevel inverter topology is more and more consolidating in the UPS applications also in the medium-low power ratings (5-40 kVA).
Multilevel is a pretty easy concept: inverter works by the series connection of IGBT modules in order to work with voltage ratings much higher than the IGBT reverse blocking voltages. The concept was first introduced for high voltage and high power converter applications to allow also the use of standard IGBTs for tens of thousand voltage rating applications.
Multilevel inverter is a simple application to improve the efficiency in the DC/AC conversion. The converter allows to get an output waveform very close to the sinusoidal one with an extremely reduced harmonic content. This gives two advantages:

- switching frequency can be reduced compared to a typical two level application and therefore silicon losses can be reduced as well;
- reduction of output filter resulting in overall dimensions and costs reduction.

A typical three-phase inverter implemented with half-bridge topology (figure 1a) allows to get an output voltage waveform that can switch between two voltage levels only. The topology in figure 1b allows to get an output voltage waveform that switch through three voltage levels and therefore this topology is known as three level inverter.

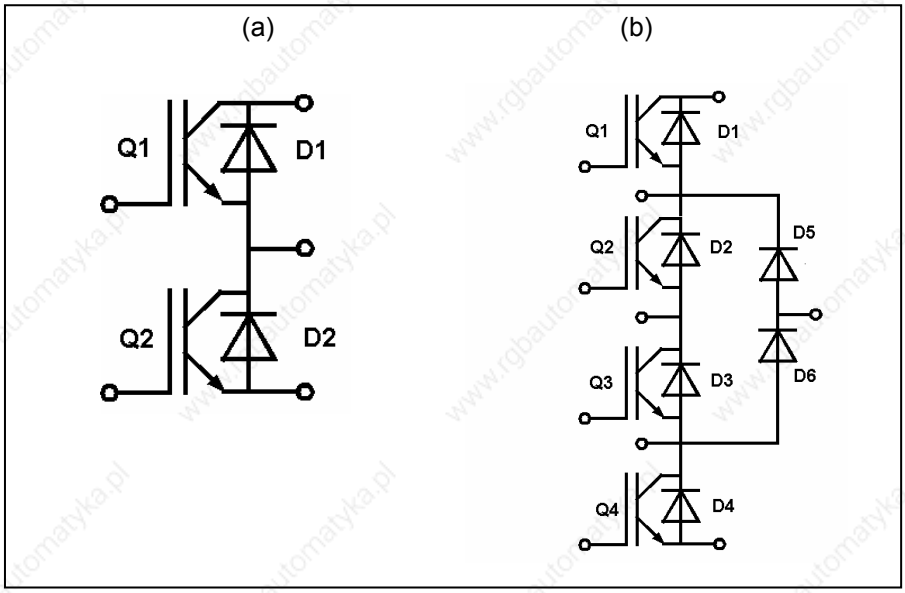


Fig 1.1 - Typical Leg for a 2 Level inverter (2L) and a 3 Level inverter (3L)

Three phase two level inverter PWM generation algorithms can be extended also to multilevel inverters. The algorithms with triangular carrier give the best benefits for harmonic distortion reduction, that means a three level inverter needs a carrier and a reference too.
In this case the number of triangular carriers is equal to L-1, being L the number of voltage levels . Therefore, **for a three phase three level inverter two triangular carriers and one sinusoidal reference are needed.**

Three alternative PWM strategies with differing phase relationships can be used for three level inverter:

1 Alternative phase opposition disposition (APOD), where carriers in adjacent bands are phase shifted by 180°
2 Phase opposition disposition (POD), where the carriers above the reference zero point are out of phase with those below zero by 180°
3 Phase disposition (PD), where all carriers are in phase across all bands

PD strategy is typically used because it allows to have the minimum harmonic distortion for the line-to-line output voltage.

Three level inverter apparently shows a major circuit complexity compared to a two level inverter, but **the resulting technical and economical advantages recommend to use it**.
Therefore two standard modules will be compared for the same application and the same boundary conditions as described on table 1.

S = 20 kVA M = 1 i_{pk} = 40,8 A	cos (φ) = 0,85 $V_{ll,rms}$ = 400V T_s = 80°C	f_{sw} = 20 kHz $I_{out,rms}$ = 29 A

	IGBT Blocking Voltage	Ic @ Ts=80°C	Vce,sat typ @ 50A chip level	Eon+Eoff @ Ic=50A,Rg=33Ω	IGBT Rthj,s
SK 30 MLI 066	600V	31A	1,65 V	4,2mJ @ Vcc=300V, Tj= 150°C	1,8 [K/W]
SK 60 GB 128	1200V	44A	1,9 V	12,5mJ @Vcc=600V, Tj=125°C	0,6 [K/W]

Table 1 – Simulation's working conditions and main IGBT parameters

Three level multilevel inverter integrates IGBT with lower reverse blocking voltage, 600V instead of 1200V. Typically 600V chips are faster and thinner than 1200V chips. Therefore **silicon in a three level inverter has lower switching losses and lower forward voltage drop.**

As summarized in table 2, **total losses per single arm of three level inverter are lower than 47%** compared to the ones of the two level inverter. Q2 and Q3 (fig. 1.1b) switching losses might be neglected. D1 and D4 diodes carry a very low current value as the current of Q1 commutes to D5, the current of Q4 commutes to D6 while the current of Q2 commutes to Q3. Clamp diodes carry the whole load current.

SK 30 MLI 066	
IGBT: total losses per arm	118 W
Neutral clamp diode total losses (D5/D6)	28 W
Total losses per arm	146 W

SK 60 GB 128	
IGBT: total losses per arm	176,1 W
Diodes total losses	53 W
Total losses per arm	229 W

Table 2 – Losses analysis: 3L Inverter vs 2L inverter

Figure 1.2 shows the overall losses trend as a function of the switching frequency for a single inverter leg (3L vs 2L). The UPS applications in the range of 20KVA, work with switching frequencies above the audible human range to reduce the noise pollution. **In this switching frequency range, the total leg losses for a 3L inverter are drastically reduced compared to the 2L inverter.**
Moreover in a 3L inverter, the output voltage waveform is really close to a sinusoidal wave, therefore the 3L inverter needs very small output filters (fig. 1.3)
Stresses on the 3L IGBTs and diodes are therefore reduced increasing the long term reliability and the application overall efficiency.

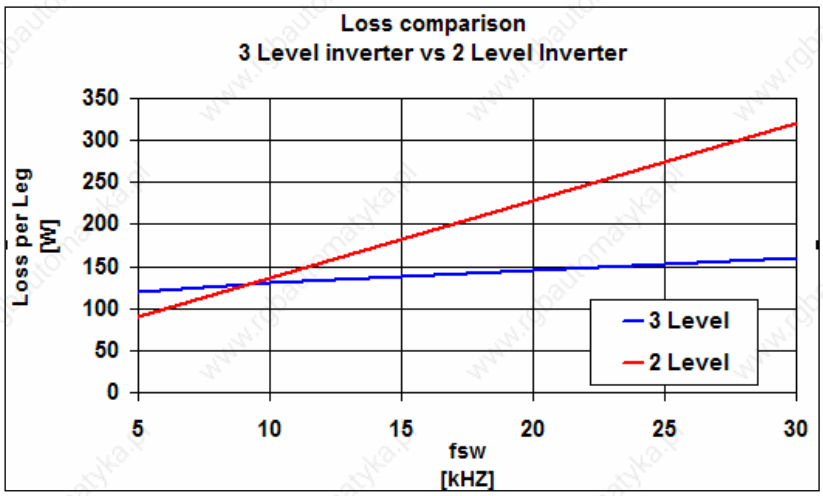


Fig 1.2 – Comparison between total losses per arm vs frequency

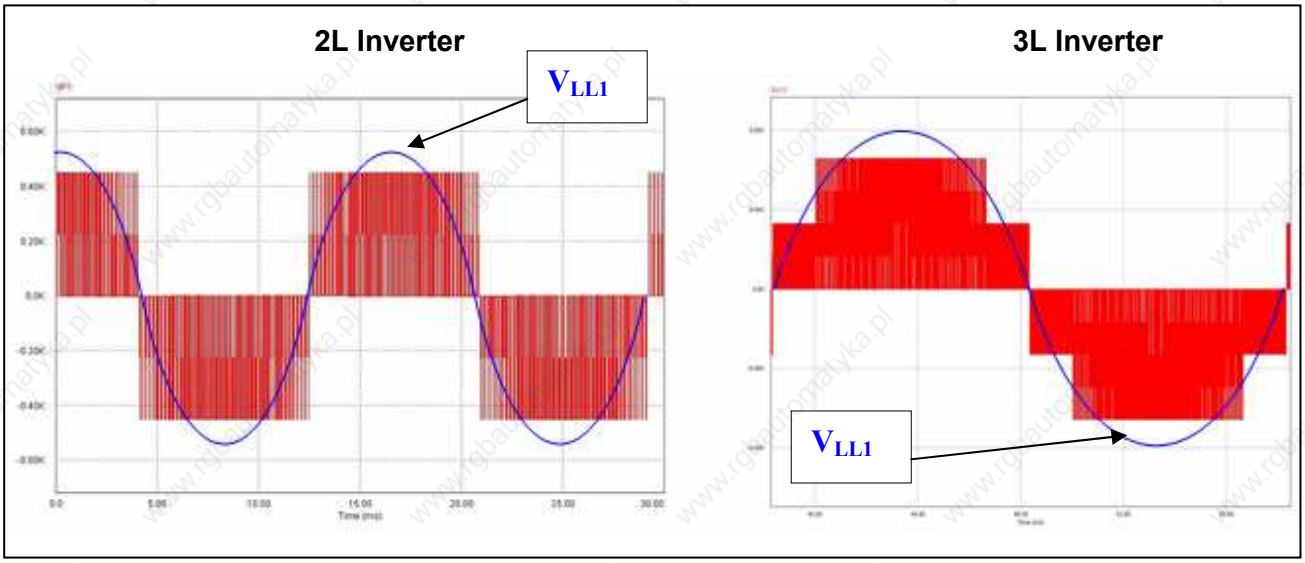


Fig 1.3 – Comparison between line-to-line output voltage for a 2L and 3L inverter

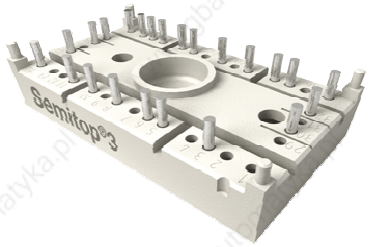
From economical perspective, in this specific analysis, the cost for a 3L inverter leg, integrating 600V silicon, is 27% cheaper than a 2L inverter leg integrating 1200V silicon.
The real benefit for a 3L inverter is the application can work with reduced stresses on the power switches due to the lower losses and the output voltage is switching through three voltage levels. Therefore the output voltage is close to a sinusoidal waveform with a reduced harmonic contents and this lead to use smaller output filters. Reduced overall losses lead to need smaller heatsink.
Smaller heastink and smaller output filter permit to reduce the overall UPS dimensions further reducing the overall costs.
Therefore using a 3L level standard SEMITOP® module UPS applications can benefit electrical, thermal efficiency maximization reducing the time to market but especially reducing the overall UPS costs.

The below table summarizes the comparison between a 3L and 2L inverter ("+":better; "-":worst; "o":no difference)

	3L	2L
Driver	-	+
PWM Algorithms	-	+
DC link	o	o
Output filters	++	-
THD	++	-
Current ripple losses	++	-
IGBT voltage	**600V**	**1200V**
Losses (switching/conduction)	++	- -

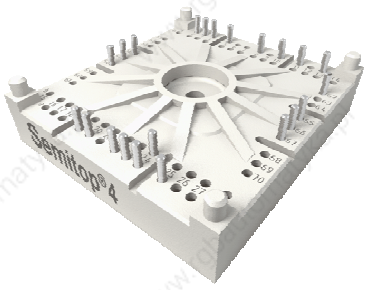
Table 3 – 3L Inverter vs 2L inverter overall comparison

SEMIKRON offers an arm of Multi Level Inverter in SEMITOP® 3 and SEMITOP®4 housing.
In the following the product portfolio for an arm of three-level inverter:



Module type	$I_{c,nom}$ [A]	$E_{on}+E_{off}$ [mJ]	$R_{th,j-s}$ [K/W]	Inverter power [kVA]*
SK 20 MLI 066	20	1,5	2,1	**22,5**
SK 30 MLI 066	30	1,7	1,8	**27,5**
SK 50 MLI 066	50	3,5	1,3	**39**

* Simulation conditions: cos(φ)=0,85;T_s = 80°C; m =1 ;f_{sw}=20kHz



Module type	$I_{c,nom}$ [A]	$E_{on}+E_{off}$ [mJ]	$R_{th,j-s}$ [K/W]	Inverter power [kVA]*
SK 75 MLI 066 T	75	3,7	0,75	**52**
SK 100 MLI 066 T	100	6,7	0,65	**60**
SK 150 MLI 066 T	150	7,3	0,55	**85**

* Simulation conditions: cos(φ)=0,85;T_s = 80°C; m =1 ;f_{sw}=20kHz

for a current rating up to 150A !

Fig. 1.4 – Multi Level Inverter SEMITOP® product portfolio

By using only three modules, it is possible to obtain a complete multi level inverter topology.
Pinout has been designed to reduce the connection lengths and to obtain a low stray inductance design.

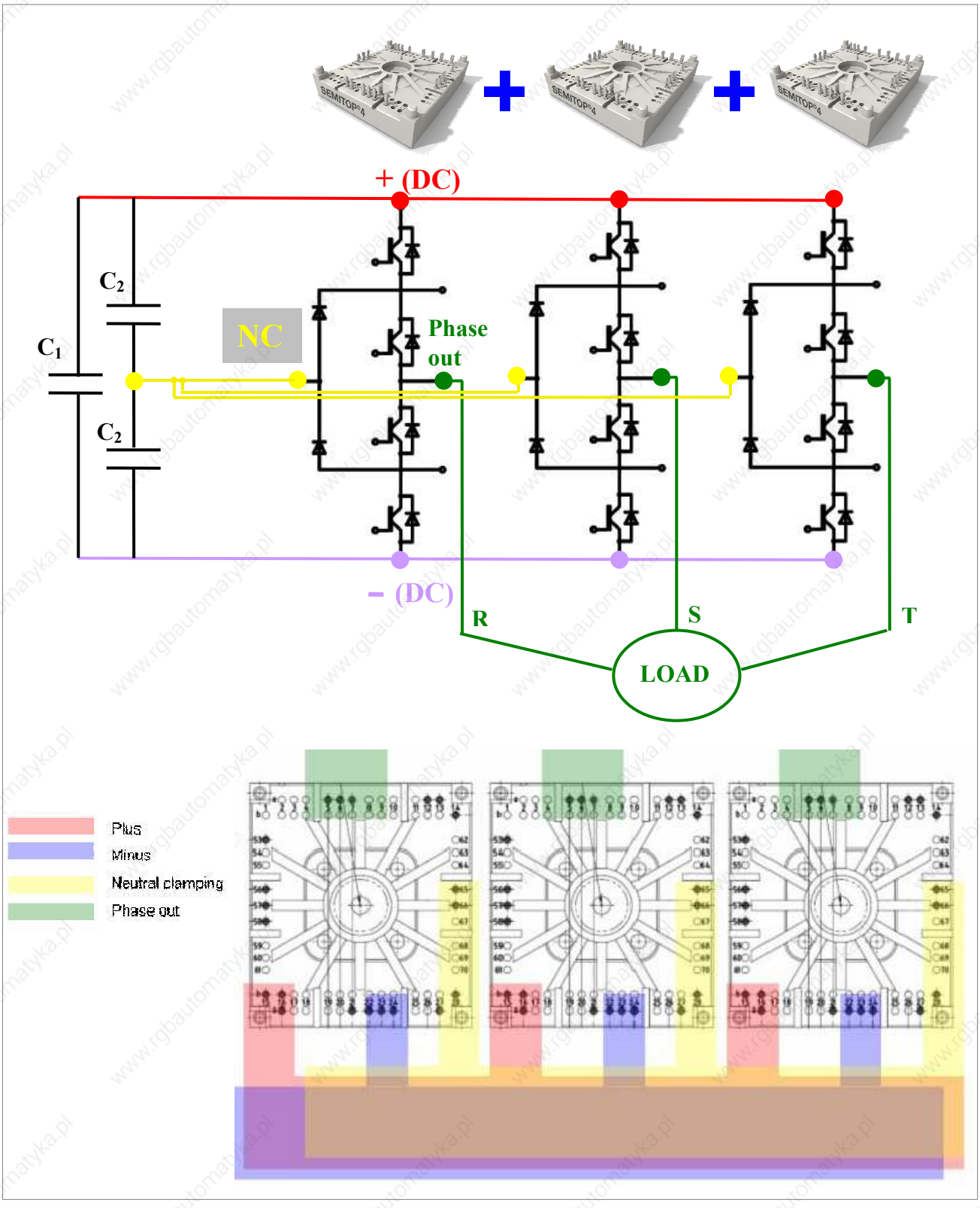


Fig. 1.5 – Connection example to assembly a complete three-phase three-level inverter

All datasheets are already available in Internet site and are complete with diagrams.

2 SEMITOP® Technical Details

The SEMITOP® range is offered in four different mechanical sizes and three different product lines: IGBT, DIODE & THYRISTOR and Low voltage MOS.
The whole SEMITOP® family is based on the same design concept and it is produced on the same production lines .
The different mechanical sizes can be mixed in the same application since the SEMITOP® platform is fully compatible.

2.1 Mechanical Construction

SEMITOP® construction is quite simple. The silicon chips are soldered to the ceramic substrate, and they are connected to the terminals by bonding wires. After pin soldering, assembly of DCB and housing is realized and then completely filled with Silicon Gel.

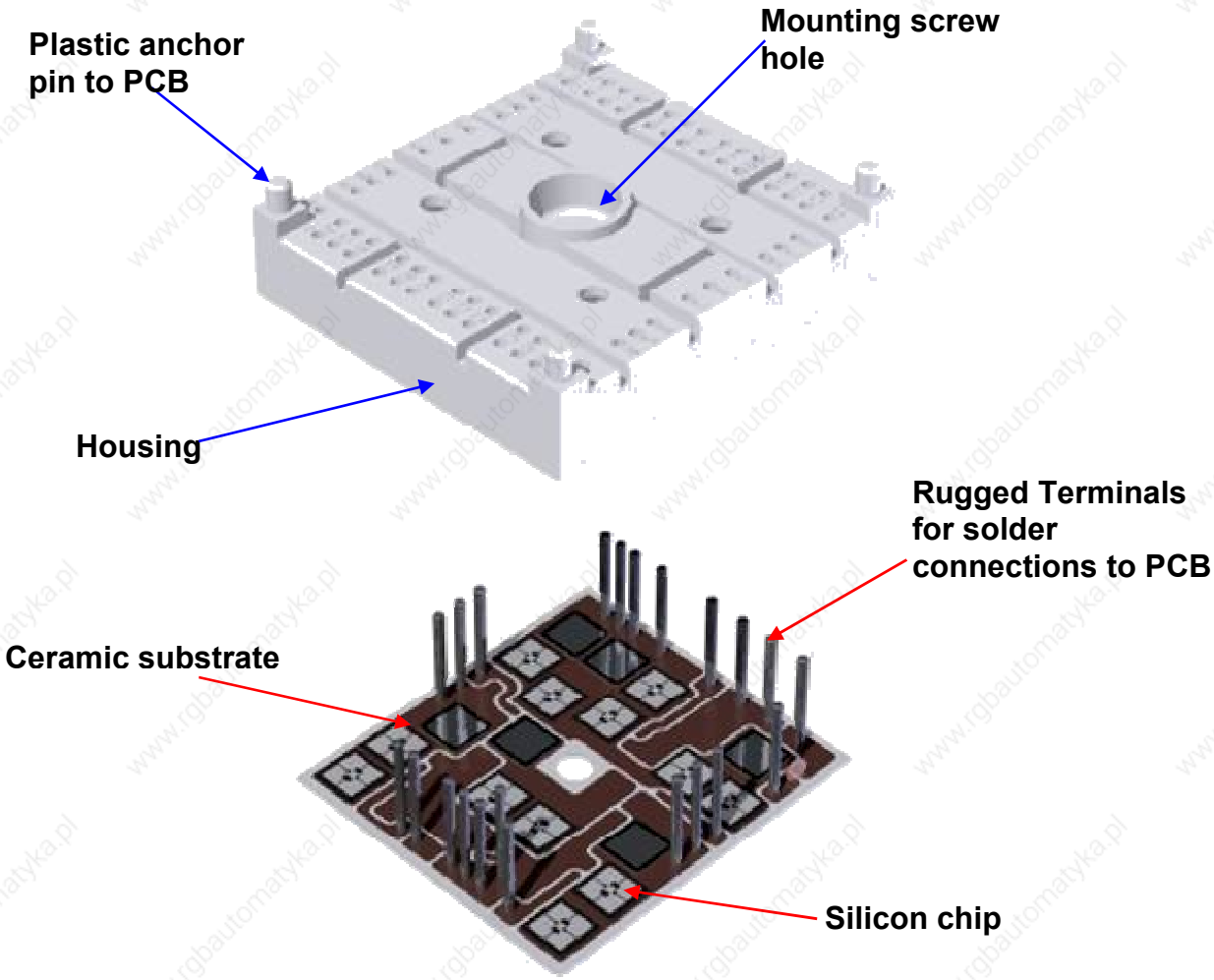


Fig 2.1- SEMITOP® Mechanical Construction

2.1.1 Tolerance system

The SEMITOP® family has been designed according tolerances defined by ISO 2768 m.
The value of tolerance depends on the value of the nominal dimension.
For a defined "working grade", greater is the nominal dimension, greater is the corresponding tolerance.

Tolerance class		Permissible deviations for basic size range							
Designation	Description	from 0,5* up to 3	over 3 up to 6	over 6 up to 30	over 30 up to 120	over 120 up to 400	over 400 up to 1000	over 1000 up to 2000	over 2000 up to 4000
f	fine	± 0,05	± 0,05	± 0,1	± 0,15	± 0,2	± 0,3	± 0,5	--
m	medium	± 0,1	± 0,1	± 0,2	± 0,3	± 0,5	± 0,8	± 1,2	± 2
c	coarse	± 0,2	± 0,3	± 0,5	± 0,8	± 1,2	± 2	± 3	± 4
v	very coarse	--	± 0,5	± 1	± 1,5	± 2,5	± 4	± 6	± 8
* For nominal size below 0,5 mm, the deviation shall be indicated adjacent to the relevant nominal size(s).									

Table 4 – Permissible deviations for linear dimensions except for broken edges

Following the values of tolerance from ISO 2768 m, according to the different dimensional ranges, SEMITOP tolerances are:

from 0.5 to 3 mm:	±0.1
from 3 to 6 mm:	±0.1
from 6 to 30 mm:	±0.2
from 30 to 120 mm:	±0.3

Quotes for all SEMITOP® in the datasheets are according to the above mentioned tolerance system:

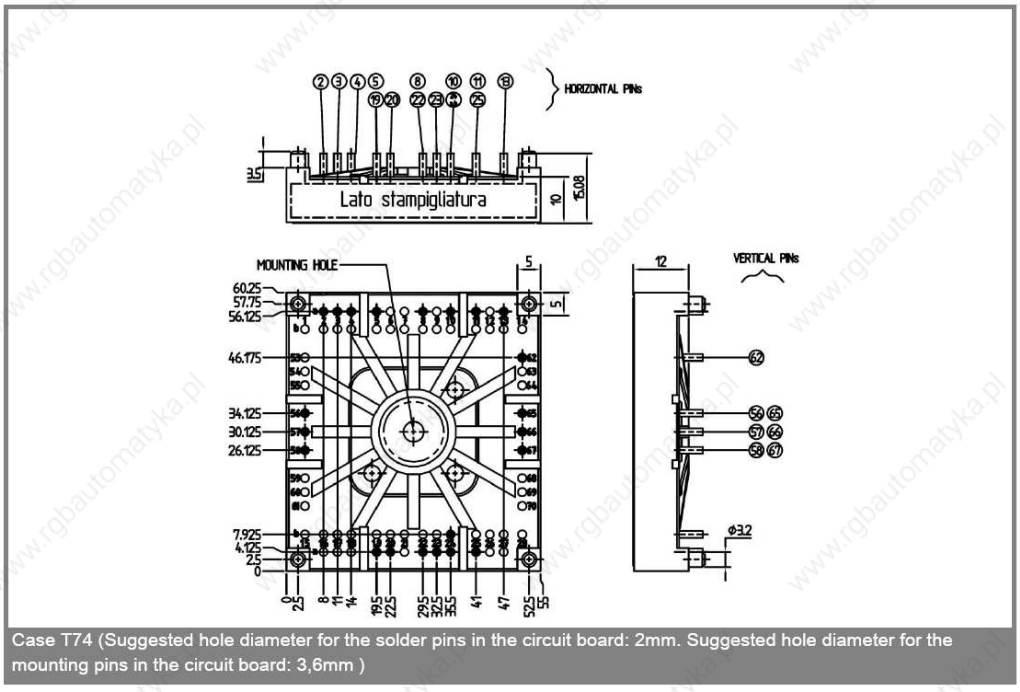
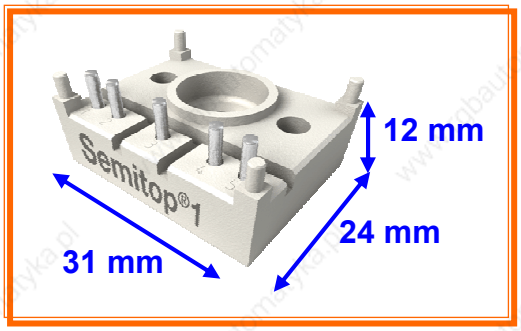
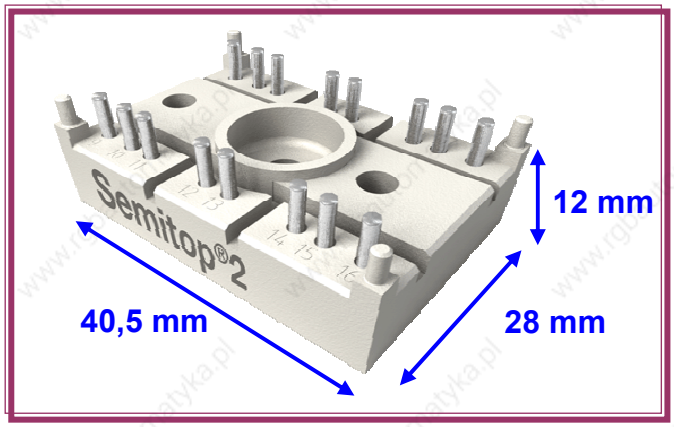


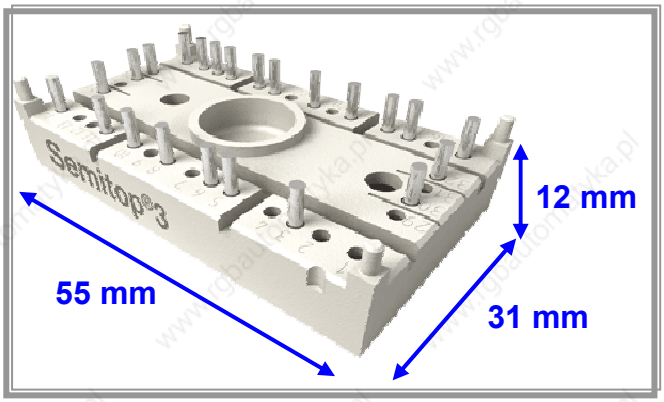
Fig. 2.2 – Example of quoting in SEMITOP datasheets

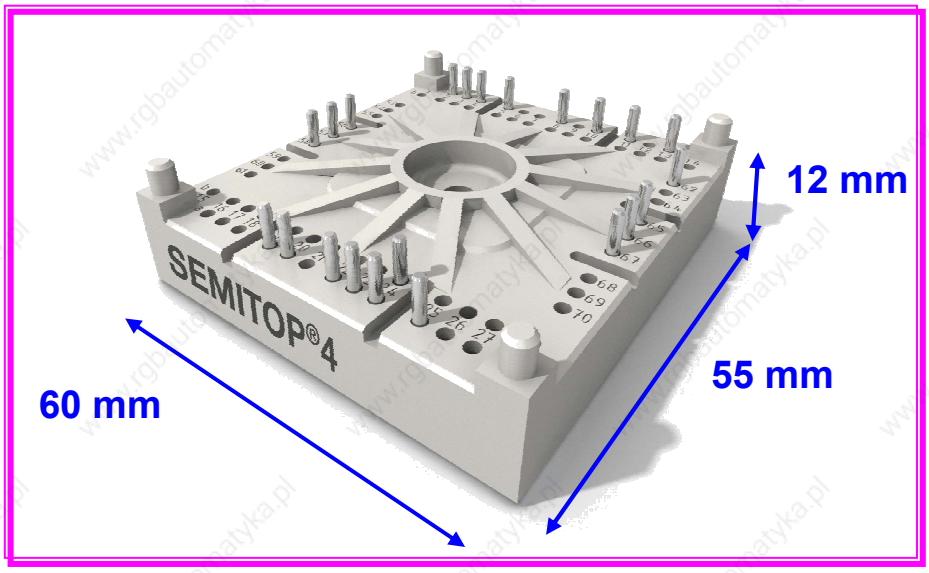
2.2 Product portfolio

SEMIKRON expands the SEMITOP® family and increases the power range with the introduction of SEMITOP® 4.
The following pictures show the overall dimensions of SEMITOP® modules:









…..up to 40 kVA

SEMITOP®4 increases the power capability of SEMITOP® family up to 25kW motor power, over three times the existing SEMITOP®3 package.

Three main topologies are integrated in SEMITOP®4 housing:

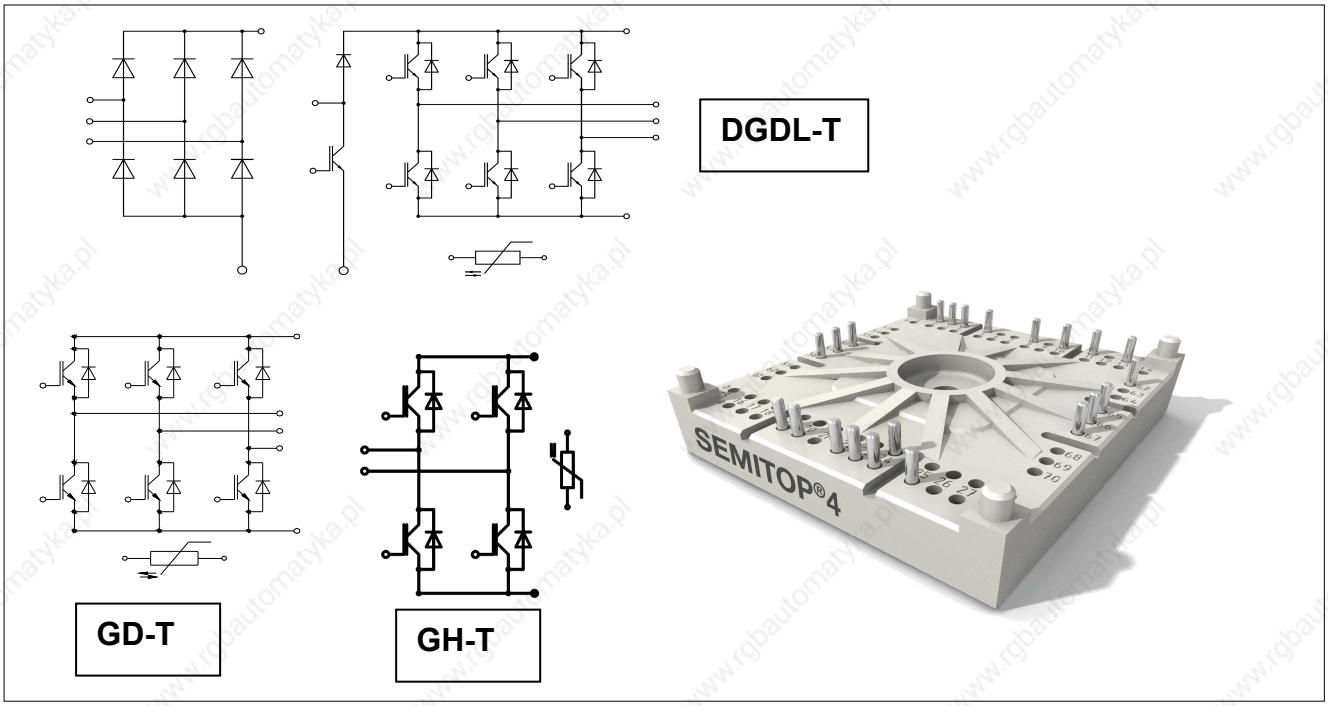


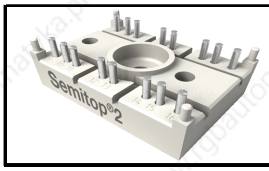
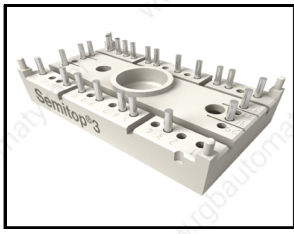
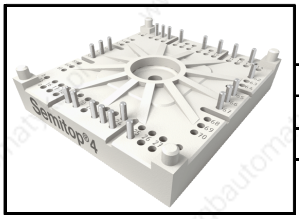
Fig. 2.3 - SEMITOP 4 topologies

Due to the introduction of this new module, the product portfolio of SEMITOP® modules increases in current and power range.
In the following an overview of the most running products divided for topologies:

- CIB modules
- Inverter modules
- Thyristor/diode modules
- Bridge rectifiers modules

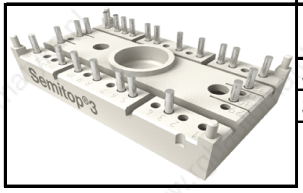
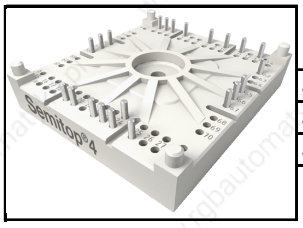
MODULES - CIB

600 V

	Type	I_{CMAX} @25°C [A]	$V_{CE(sat)}$ typ. @25°C [V]	Eon+Eoff typ. @125°C [mJ]	$R_{th(j-s)}$ [k/W]	Case	Motor power* [kW]
	SK 8 BGD 065 E	12	2	0,34	2,6	SEMITOP 2	1,5
	SK 9 DGD 065 ET	20	2	0,34	2,6	SEMITOP 3	1,5
	SK 20 DGD 065 ET	26	2	1,06	1,7	SEMITOP 3	3
	SK 25 DGD 065 ET	30	1,8	1,35	1,4	SEMITOP 3	3
	SK 10 DGDL 065 ET	17	2	0,31	2	SEMITOP 3	2,2
	SK 15 DGDL 065 ET	19	2	0,52	1,9	SEMITOP 3	2,5
	SK 20 DGDL 065 ET	24	2	1,08	1,7	SEMITOP 3	3
	SK 30 DGDL 066 ET	35	1,45	2,01	1,8	SEMITOP 3	5
	SK 50 DGDL 066 T	69	1,45	3,1	0,95	SEMITOP 4	7,5
	SK 75 DGDL 066 T	81	1,45	5,7	0,75	SEMITOP 4	10
	SK 100 DGDL 066 T	106	1,45	6,9	0,65	SEMITOP 4	12,5

***Motor power at Ts=80°C,fsw=12kHz, Vcc=310V,Vout=190V,fout=50Hz overload=150% for 60s**

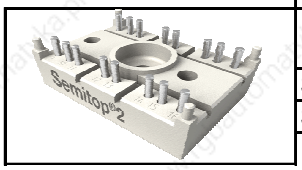
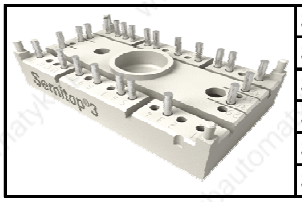
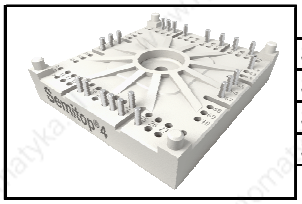
1200 V

	Type	I_{CMAX} @25°C [A]	$V_{CE(sat)}$ typ. @25°C [V]	Eon+Eoff typ. @125°C [mJ]	$R_{th(j-s)}$ [k/W]	Case	Motor power* [kW]
	SK 10 DGDL 126 ET	15	1,7	2	2	SEMITOP 3	3
	SK 15 DGDL 126 ET	22	1,7	3,8	1,6	SEMITOP 3	4
	SK 25 DGDL 126 T	41	1,7	6,5	0,9	SEMITOP 4	5,5
	SK 35 DGDL 126 T	52	1,7	8,6	0,75	SEMITOP 4	7,5
	SK 50 DGDL 126 T	68	1,7	12,5	0,6	SEMITOP 4	12,5

***Motor power at Ts=80°C,fsw=12kHz,Vcc=600V,Vout=400V, fout=50Hz, overload=150% for 60s**

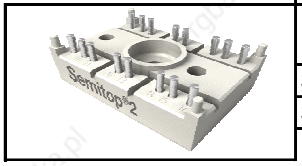
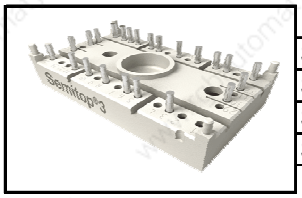
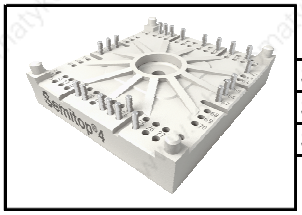
MODULES - IGBT

600 V

	Type	I_{CMAX} @25°C [A]	$V_{CE(sat)}$ typ. @25°C [V]	Eon+Eoff typ. @125°C [mJ]	$R_{th(j-s)}$ [k/W]	Case	Motor power* [kW]
	SK 9 GD 065	11	2	0,34	2,6	SEMITOP 2	0,75
	SK 20 GD 065	24	2	1,04	1,7	SEMITOP 2	5,5
	SK 10 GD 065ET	17	2	0,31	2	SEMITOP 3	2,2
	SK 15 GD 065 ET	20	2	0,52	1,9	SEMITOP 3	2,5
	SK 20 GD 065 ET	26	2,1	1,04	1,7	SEMITOP 3	3
	SK 25 GD 065 ET	30	1,8	1,35	1,4	SEMITOP 3	4
	SK 35 GD 065 ET	45	2	1,9	1	SEMITOP 3	5
	SK 50 GD 066 ET	51	1,45	3,1	1,3	SEMITOP 3	7,5
	SK 75 GD 066 T	83	1,45	5,7	0,75	SEMITOP 4	10
	SK 100 GD 066 T	105	1,45	6,9	0,65	SEMITOP 4	15
	SK 150 GD 066 T	151	1,45	11,4	0,55	SEMITOP 4	17,5
	SK 200 GD 066 T	174	1,45	13,8	0,45	SEMITOP 4	20

***Motor power at Ts=80°C,fsw=12kHz, Vcc=310V,Vout=190V, fout=50Hz overload=150% for 60s**

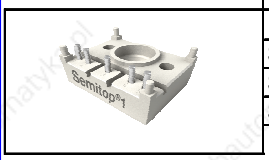
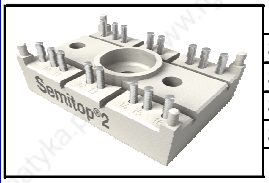
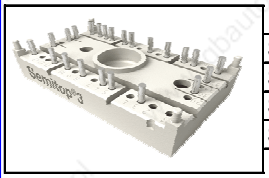
1200 V

	Type	I_{CMAX} @25°C [A]	$V_{CE(sat)}$ typ. @25°C [V]	Eon+Eoff typ. @125°C [mJ]	$R_{th(j-s)}$ [k/W]	Case	Motor power* [kW]
	SK 8 GD 126	15	1,7	1,9	2	SEMITOP 2	2,5
	SK 15 GD 126	22	1,7	3,56	1,6	SEMITOP 2	4
	SK 10 GD 126 ET	15	1,7	2	2	SEMITOP 3	3
	SK 15 GD 126 ET	22	1,7	3,56	1,6	SEMITOP 3	4
	SK 25 GD 126 ET	32	1,7	6,4	1,2	SEMITOP 3	5
	SK 35 GD 126 ET	40	1,7	8,9	1,05	SEMITOP 3	5,5
	SK 50 GD 126 T	68	1,7	12,1	0,6	SEMITOP 4	10
	SK 75 GD 126 T	88	1,7	16,7	0,5	SEMITOP 4	15
	SK 100 GD 126 T	114	1,7	26,1	0,4	SEMITOP 4	20

***Motor power at Ts=80°C,fsw=12kHz,Vcc=600V,Vout=400V, fout=50Hz, overload=150% for 60s**

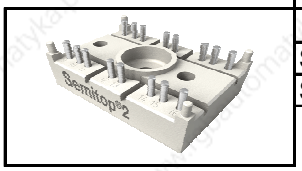
* : Customers need to check in the details their own conditions

MODULES - Thyristor/Diode

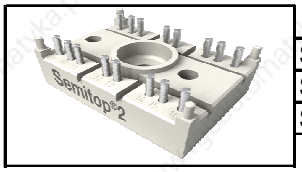
	Type	V_{RRM} [V]	I_{RMS} [A]	I_{TSM} @25°C [A]	$V_{T(TO)}$ typ. @25°C [V]	rT @125°C [mΩ]	$R_{th(j-s)}$ [k/W]	Case	Motor power* [kW]
	SK 25 KQ	800-1600	20	390	1,1	20	1,7	SEMITOP 1	14
	SK 45 KQ	800-1600	33	720	1	10	1,2	SEMITOP 1	20
	SK 70 KQ	800-1600	72	1000	1	6	0,8	SEMITOP 1	22
	SK 100 KQ	800-1600	101	1500	0,9	4,5	0,6	SEMITOP 2	30
	SK 120 KQ	800-1600	134	2000	0,9	3,5	0,45	SEMITOP 2	40
	SK 25 WT	800-1600	20	390	1,1	20	1,7	SEMITOP 2	14
	SK 45 WT	800-1600	33	720	1	10	1,2	SEMITOP 2	20
	SK 25 UT	800-1600	20	390	1,1	20	1,7	SEMITOP 3	14
	SK 45 UT	800-1600	33	720	1	10	1,2	SEMITOP 3	20
	SK 70 WT	800-1600	72	1000	1	6	0,8	SEMITOP 3	22
	SK 100 WT	800-1600	101	1500	0,9	4,5	0,6	SEMITOP 3	30

***Motor power at Ts=80°C,Vin=400V, overload=150% for 60s, Tjmax=125°C**

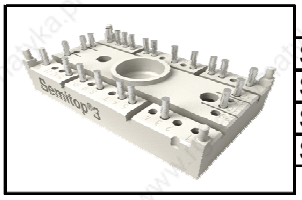
Bridge rectifiers SEMITOP

	Type	V_{RRM} [V]	I_D T_h=80°C [A]	Case	Motor power* [kW]	
	SK 50 B	800-1600	51	SEMITOP 2	7	
	SK 70 B	800-1600	68	SEMITOP 2	10	

***Motor power at Ts=80°C,Vin=230V, overload=150% for 60s, Tjmax=125°C**

	SK 55 D	800-1600	55	SEMITOP 2	12,5
	SK 70 D	800-1200	70	SEMITOP 2	15
	SK 95 D	800-1600	95	SEMITOP 2	22,5

***Motor power at Ts=80°C,Vin=400V, overload=150% for 60s, Tjmax=125°C**

	SK 40 DH	800-1600	42	SEMITOP 3	5,5	firing angle=0°
	SK 70 DH	800-1600	68	SEMITOP 3	11	firing angle=0°
	SK 40 DT	800-1600	42	SEMITOP 3	5,5	firing angle=0°
	SK 70 DT	800-1600	68	SEMITOP 3	11	firing angle=0°

***Motor power at Ts=80°C,Vin=400V, overload=150% for 60s, Tjmax=100°C**

*: indications valid at Ts=80°C and oveload factor=1.5 for 60s. Customers need to check in the details their own conditions

2.3 Chip technologies

- IGBT technologies:

Voltage / Technology	600 V	1200 V	
Standard	063	123	
Fast	065	125	
Trench 3	066	126	(fast chip technology)
Hyperfast	067		
SPT		128	
Trench 4		12T4	New Trench4 technology

- MosFet trench technologies: 55V, 75V, 100V,150V,200V
- CoolMos: 600V

2.4 Type designation system

①	②	③	④	⑤	⑥	⑦
SK	30	DGDL	06	6	E	T

① SK = SEMIKRON product

② Type current [A]: approximately module current at Ts=80°C

③ Circuit topology description

④ Voltage grade:

- Thyristor/diode: V_{RRM} [V]/10;
- IGBT: V_{CE} [V]/100 ;
- MOS: V_{DS}[V] / 10

⑤ Optional: chip generation

3 = Standard NPT IGBT technology
5 = Ultrafast NPT IGBT technology
6 = Fast Trench 3 IGBT technology
7 = Hyperfast IGBT technology
8 = SPT IGBT technology
T4 = Trench 4 IGBT technology

⑥/⑦ Optional: extras (e.g. F: fast diode; T: temp sensor; E: open emitter; I: current sensor)

3 Chip technologies and optimised operation frequency

Maximum allowable current, applied voltage and power dissipation define the maximum ratings for a device. These absolute maximum ratings have not to be exceeded if long life and reliability are to be attained. Ratings depend from material used, structure, design, mount and type of process. Therefore the close correlation between electrical properties and different ratings defines the electrical operating bounds of different devices, according to the following picture:

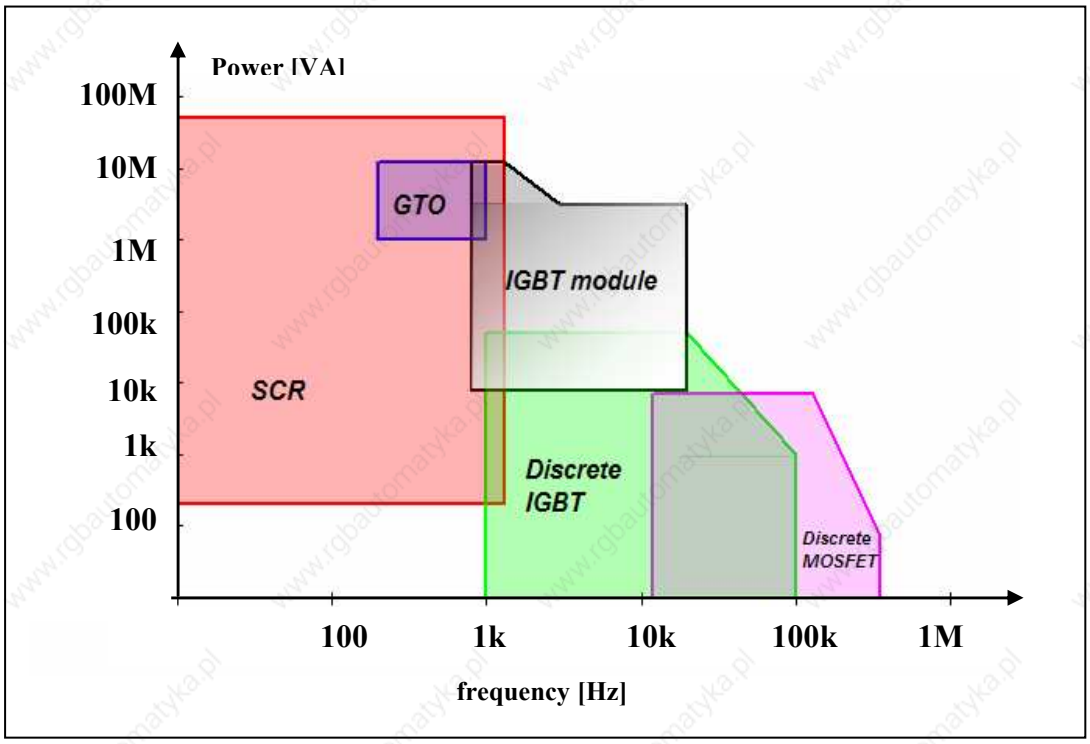


Fig. 3.1 – Frequency range application for different modules

The general trend is the higher I-V ratings the slower the possible switching frequency, hence increased junction temperature.
High frequency low-power applications is dominated by MosFets or trench-gate IGBTs, high-power low-frequency switching applications are dominated by thyristor.
The IGBT combines both the voltage controlled properties of MosFet both the main features of bipolar transistors.
The IGBT is suitable for numerous applications in power electronics, especially in pulse-width modulated servo and three-phases drives; it can also be used for UPS applications and other power applications requiring high switch repetition rates.

3.1 600V IGBT technology characteristics

Different 600V reverse voltage IGBTs chip technologies are integrated in SEMITOP® modules. In the following a comparison in terms of main IGBT parameters:

Parameter / Series	063	065	066	067
V_{CEsat} @ 25 °C	2,1	2,2	1,5	2,7
typ. Eon per 30A	1,11	0,98	0,98	0,91
typ. Eoff per 30A	1,2	0,95	1,1	0,68
Relative chips size at rated current	100	100	60 40% Higher Rthjs	100
pos. Temp. Coeff of V_{CEsat}	Yes	Yes	Yes	Yes
Gate Charge per 100 A, -8 V ... +15 V	140	140	167	140

Table 5 – Comparison between 600V IGBT technologies

066 series allows to obtain the same current rating with a smaller chip size compared to the other technologies but it means an higher $R_{th(j-s)}$. 067 series exhibits a drastically reduced E_{off} .
Comparison of different technologies behaviour has been investigated calculating energy losses on a typical industrial application.
A dependency of the power losses from the frequency switching for the different 600V chip technologies was obtained as the following picture shows:

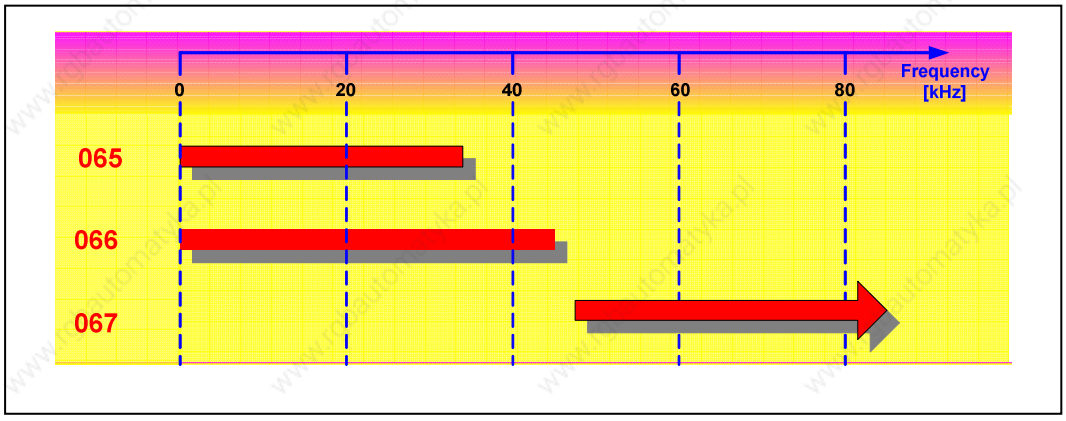


Fig. 3.2 – Frequency range application for 600V chip technologies

Future trend will be to replace the existing 063 and 065 modules with the equivalent 066 modules.
For 50kHZ upwards, 067 series is the most performing technology also due to the drastically reduced E_{off} and therefore is suitable for high frequency applications.

3.2 1200V IGBT technology characteristics

In the following picture, a comparison between the different 1200V IGBT technologies:

Parameter	Standard 123 series	Ultrafast 125 series	SPT 128 series	Unit
V_{CEsat} @ 25°C	2.5	3.3	1.9	V
E_{ON} +E_{OFF} per 100A	28	15	21	mJ
Relative chip size at rated current	100	100	100	%
pos. temp. coeff. of V_{CEsat}	YES	YES	YES	-
Q_G* [nC] / 100A	850	1000	1000	nC
Q_G* [nC] / 100 mm²	530	620	620	nC

* measured @ V_{GE} from -8V to 15V

Table 6 – Comparison between 1200V IGBT technologies

According to the power losses calculation for a typical industrial application, in the picture an overview of the frequency range application for the different 1200V chip technologies:

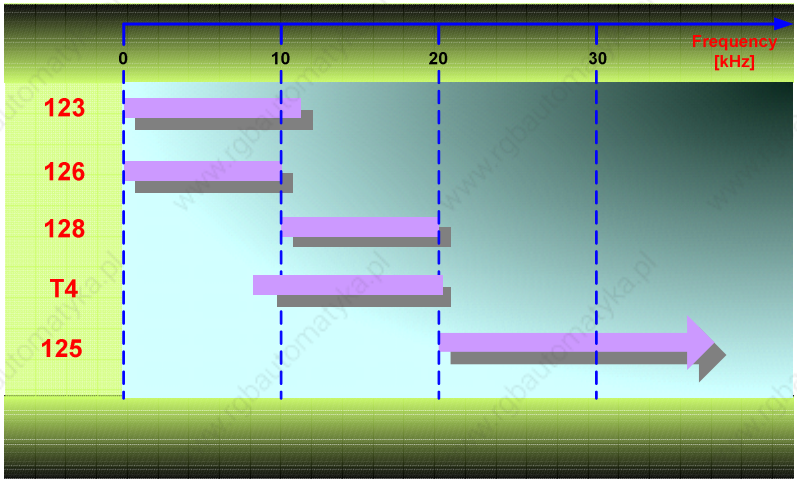


Fig. 3.3 – 1200V IGBT frequency range application

3.3 NEW TRENCH 4 IGBT technology

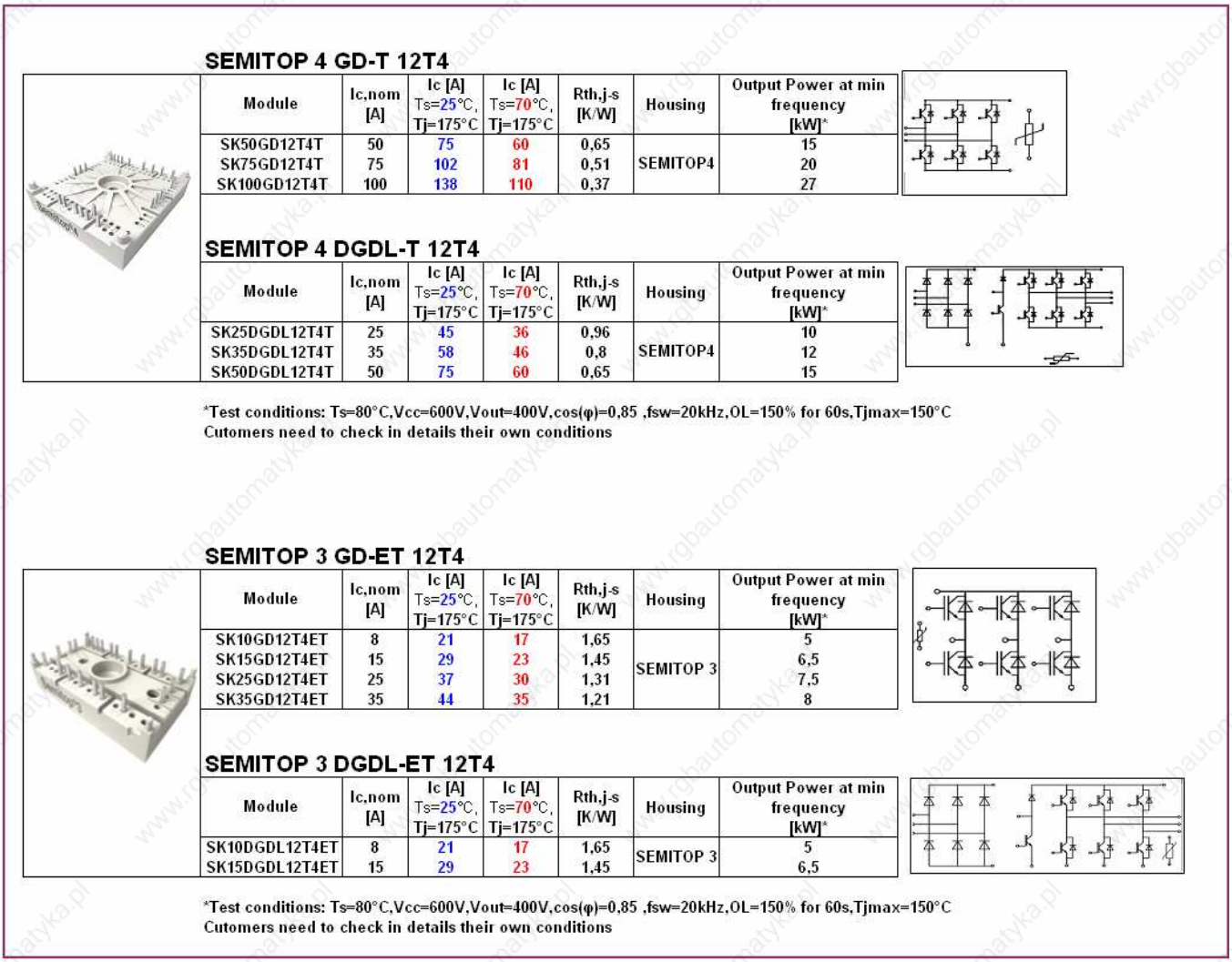
New TRENCH4 IGBT technology enables an operation at higher junction temperature up to 175°C. This offers margin in driver application for overload condition. In low output frequency operating conditions, the current can exceed two times the nominal current up to several milliseconds. The IGBT4 can provide a repetitive overload current capability of three times the nominal chip current. In more and more applications the operating DC link reaches 850-900V. IGBT4 is a 1200V rated chip with a reverse blocking voltage up to 150V.

The following table summarizes the main IGBT4 benefits:

Criteria	IGBT4
Maximum junction temperature	175°C
Repetitive overload current I_{CRM}	3 x $I_{c,nom}$
Reverse voltage margin to 1200V	150V

Table 7 – Main IGBT4 properties

Together with the IGBT4 chip, SEMIKRON introduces CAL4 diodes for junction temperature operation up to 175°C and with a current density increase up to 20%.
SEMITOP® modules will integrate IGBT4 with CAL4 chip in SEMITOP® housings to extend the product portfolio.
Two main topologies are planned be implemented, to obtain the product portfolio shown in the picture:



SEMITOP 4 GD-T 12T4

Module	Ic,nom [A]	Ic [A] Ts=25°C, Tj=175°C	Ic [A] Ts=70°C, Tj=175°C	Rth,j-s [K/W]	Housing	Output Power at min frequency [kW]*
SK50GD12T4T	50	75	60	0,65	SEMITOP4	15
SK75GD12T4T	75	102	81	0,51		20
SK100GD12T4T	100	138	110	0,37		27

SEMITOP 4 DGDL-T 12T4

Module	Ic,nom [A]	Ic [A] Ts=25°C, Tj=175°C	Ic [A] Ts=70°C, Tj=175°C	Rth,j-s [K/W]	Housing	Output Power at min frequency [kW]*
SK25DGDL12T4T	25	45	36	0,96	SEMITOP4	10
SK35DGDL12T4T	35	58	46	0,8		12
SK50DGDL12T4T	50	75	60	0,65		15

*Test conditions: Ts=80°C,Vcc=600V,Vout=400V,cos(φ)=0,85 ,fsw=20kHz,OL=150% for 60s,Tjmax=150°C
Cutomers need to check in details their own conditions

SEMITOP 3 GD-ET 12T4

Module	Ic,nom [A]	Ic [A] Ts=25°C, Tj=175°C	Ic [A] Ts=70°C, Tj=175°C	Rth,j-s [K/W]	Housing	Output Power at min frequency [kW]*
SK10GD12T4ET	8	21	17	1,65	SEMITOP 3	5
SK15GD12T4ET	15	29	23	1,45		6,5
SK25GD12T4ET	25	37	30	1,31		7,5
SK35GD12T4ET	35	44	35	1,21		8

SEMITOP 3 DGDL-ET 12T4

Module	Ic,nom [A]	Ic [A] Ts=25°C, Tj=175°C	Ic [A] Ts=70°C, Tj=175°C	Rth,j-s [K/W]	Housing	Output Power at min frequency [kW]*
SK10DGDL12T4ET	8	21	17	1,65	SEMITOP 3	5
SK15DGDL12T4ET	15	29	23	1,45		6,5

*Test conditions: Ts=80°C,Vcc=600V,Vout=400V,cos(φ)=0,85 ,fsw=20kHz,OL=150% for 60s,Tjmax=150°C
Cutomers need to check in details their own conditions

Fig. 3.4 – SEMITOP product portfolio with IGBT4 chip

A comparison between the present 1200V IGBT technologies has been performed, for the same nominal chip current (50A).

	IGBT 4	IGBT 3	Unit
$V_{CE,sat}$ @ 125°C, chip level	2,2	2,0	V
$E_{on}+E_{off}$ (50A,15Ω)	10,8	12,5	mJ
$T_{j,max}$	175	150	°C
Relative chip area	87	100	%
$R_{th,j-s}$	0,65	0,6	K/W

Table 8 – Comparison 1200V IGBTs

Due to the reduced chip area, IGBT4 has a bigger current density and maximum junction temperature is 175°C instead of 150°C.

New SEMITOP® T4 modules will also integrate the newest SEMIKRON diode generation: CAL4 diodes in order to reach the operating junction temperature of 175°C.
CAL diodes 4th generation are Controlled Axial Lifetime chips with an increased current density up to 20%.
A comparison among the present diode technologies has been performed, for the same diode nominal current (50A)

	CAL I4	CAL HD	CAL I3	Unit
$V_{CE,sat}$ @ 125°C, chip level	2,0	1,6	1,8	V
E_{rr} (50A,15Ω)	0,9	3,75	2	mJ
$T_{j,max}$	175	150	150	°C
Relative chip area	62	66	100	%
$R_{th,j-s}$	1,1	1	0,7	K/W

Table 9 – Comparison 1200V CAL4 diodes

3.4 Operating areas for IGBT

3.4.1 Safe operating area (SOA)

Safe operating area is defined as the voltage and current conditions over which the chip can operate without self-damage during switching-on. This curve is not present in datasheet but can be provided on request.
SOA curve is a graph that exhibits dependence of collector current from collector-emitter voltage by considering different short duration conditions and junction temperature of the device.
The safe operating area is the area under the considered curve.
In the following an example of SOA curve for module SK10DGDL126ET:

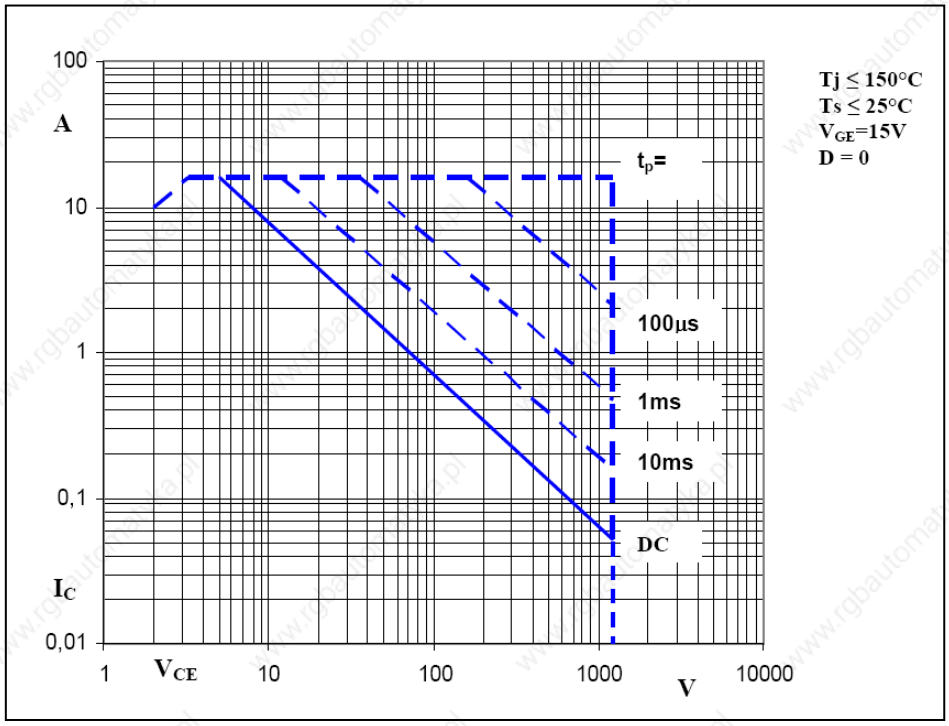


Fig. 3.5 – Safe Operating Area (SOA) diagram

3.4.2 Reverse Bias Safe operating area (RBSOA)

Reverse Bias Safe operating area is the SOA curve when the device is during turn-off state.
This curve is also not present in datasheet but it can be provided on request.
Maximum V_{CES} has not to be exceeded during turn-off. Due to the internal stray inductance, collector-emitter voltage to terminals is less than the collector-emitter voltage at chip level. This it the reason the curve is cut in the upper right corner respect to the curve at chip level.
In the following an example of RBSOA curve for modules SK10DGDL126ET:

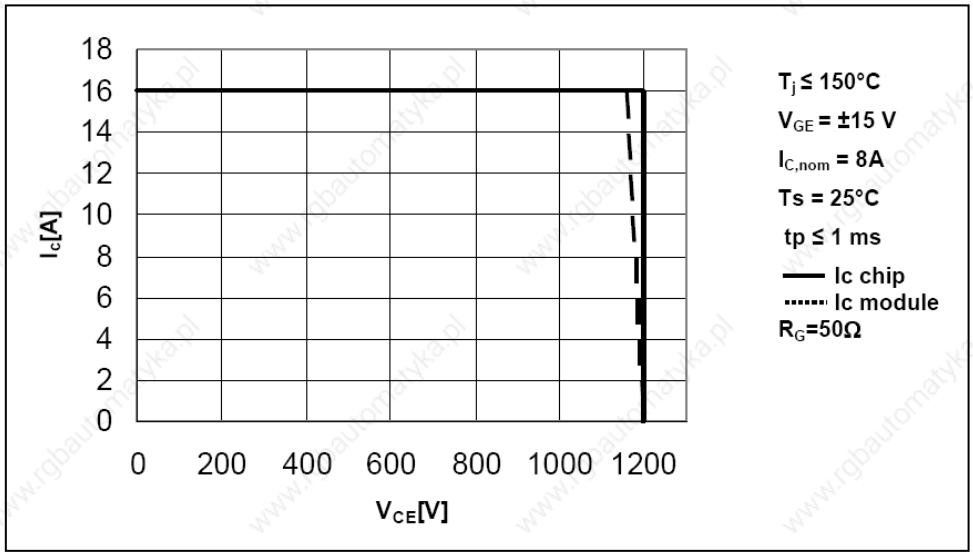


Fig. 3.6 – Reverse Bias Safe Operating Area (RBSOA) diagram

3.4.3 Short Circuit Safe operating area (SCSOA)

This is the SOA curve at short circuit condition. The diagram shows the limit for safe control of a short circuit. The curve is not present in the datasheets but it can be provided on request.

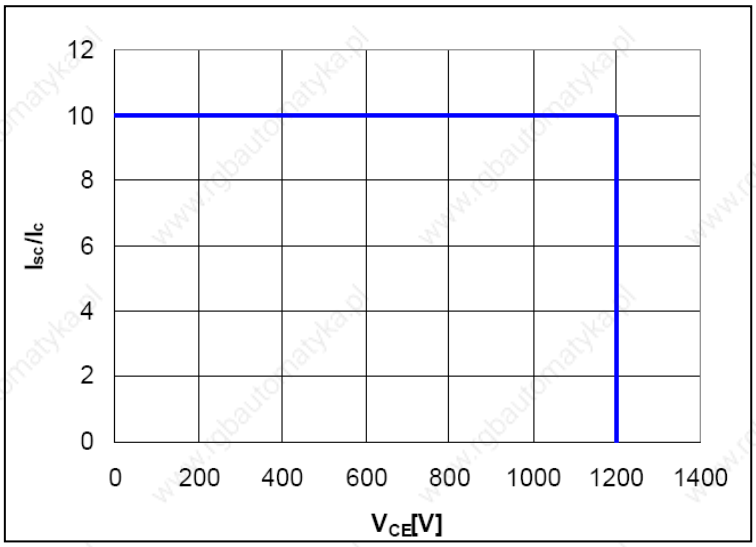


Fig. 3.6 – Short Circuit Safe Operating Area (SCSOA) diagram

The picture shows SCSOA curve for moduel SK10DGDL126ET.
The following boundary conditions have to be fulfilled to guarantee safe operation:

1) the short circuit has to be detected and turned off within max 10μs
2) the time between two short circuits has to be at least 1second
3) the IGBT must not be subjected to more than 1000 short circuits during its total operation time

4 SEMITOP® technology

When SEMIKRON introduced in the low power, low cost market SEMITOP® family, SEMIKRON offered an alternative solution to classical discrete components (so called TOs).

SEMITOP® modules are actually made by direct soldering of the silicon chips (IGBT, Mosfet, Diodes, Thyristors) and the power terminals on a ceramic substrate, typically aluminium oxide Al_2O_3 or aluminium nitrate AlN covered by a thin copper layer (see Fig.4.1).
The ceramic substrate is directly placed on the heatsink using only a thermal conductive material (typically Thermal Grease). Such a silicon material should fill all air gaps at the interface between the module and the heat sink.
The housing is the basic part of SKiiP® technology in SEMITOP® modules.
The housing has to guarantee that the ceramic substrate is evenly set on the heatsink in order to perform an homogenous heat exchange between module and the heatsink.
The SEMITOP® plastic housing has to evenly pressure the substrate surface through the only screw required for the mounting.

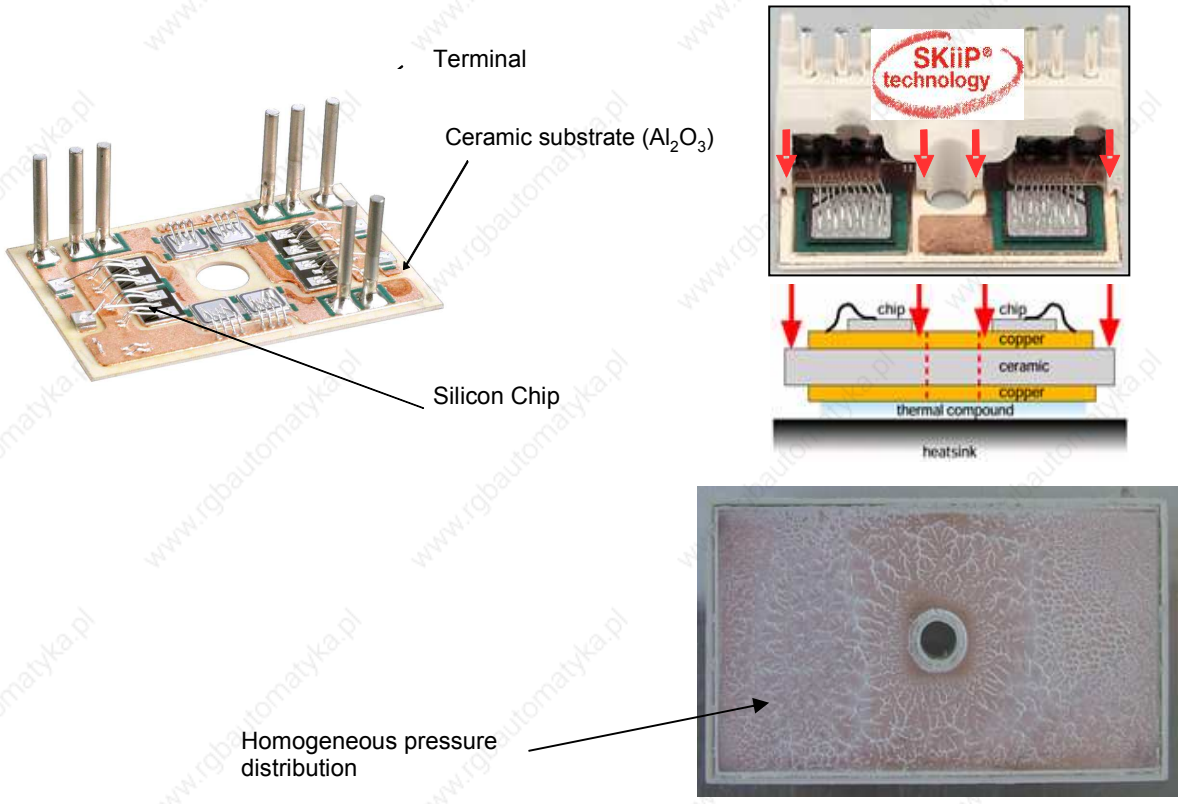


Fig. 4.1 – SEMITOP structure and concept of SkiiP Technology

The pressure concept allows to obtain the following advantages:

- Lower thermal resistance, lower chip temperature, no hot spots
- No stress on the bonding connections
- High thermal and power cycling capability, that means long term reliability

4.1 Technical comparison with dicrete components (TO devices)

SEMITOP® are baseplate free modules while **TO devices are module with baseplate** (see Fig. 4.2)

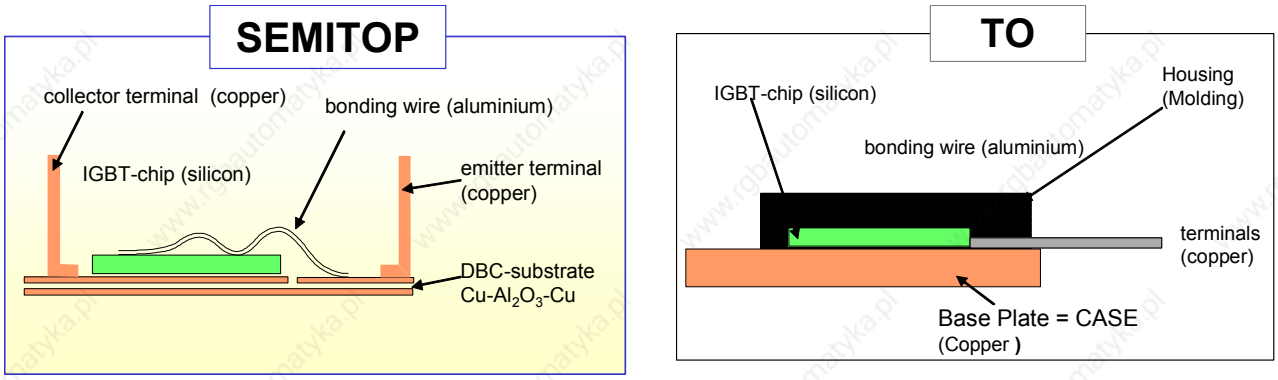


Fig. 4.2 – Difference in the structure between SEMITOP modules and TO devices

Dice are placed on a DCB substrate in SEMITOP® modules. DCB substrate is made of a **top side copper layer in direct contact with the chip, a ceramic layer that ensures insulation and a back side copper layer that goes in contact with the heatsink.** In this manner the whole module is in direct contact with the heatsink through the DCB substrate.
TO modules have dice in direct contact with a copper layer. No further copper and ceramic layers are present. TO modules are not isolated. They need a further insulation foil to be placed on a heatsink.
This difference affects the thermal resistance paths for the two modules as the following picture shows:

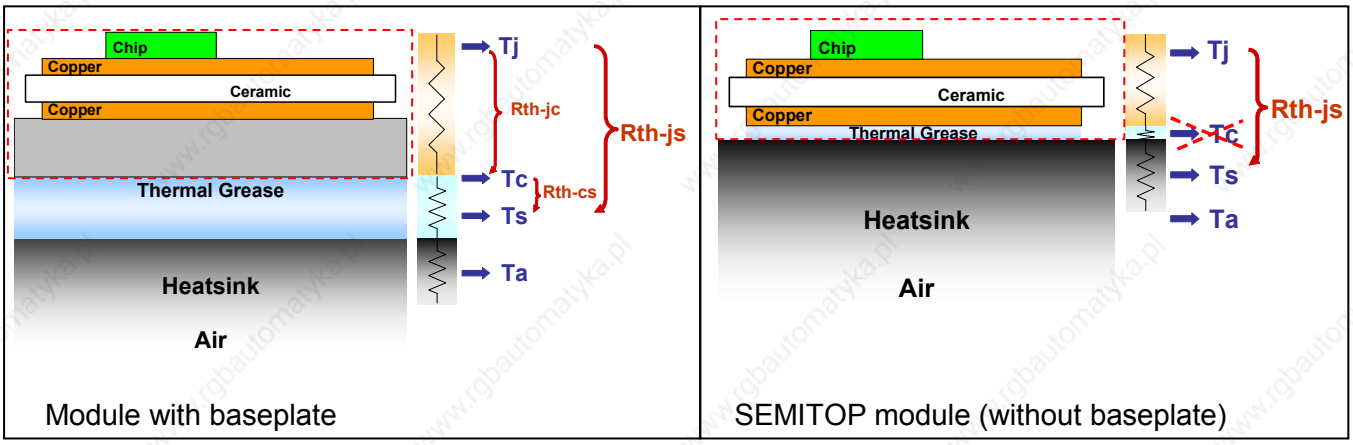
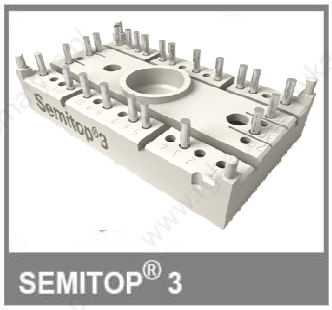


Fig. 4.3 – Thermal resistance paths for a baseplate and a baseplate less module

By using SEMITOP module, junction-case thermal resistance path is avoided and there is a direct thermal path between chip junction and heatsink. With a module with baseplate, there are two paths to consider: junction-case and case-sink thermal ones.
This difference means that SEMITOP current characterization is based on **heatsink temperature**, while TO current characterization refers to **case temperature.**
*The **maximum allowable DC current** for **TO**s is referred to the **case temperature**. SEMITOP module doesn't have the base plate, therefore the maximum allowable DC current for **SEMITOP** is referred to the **heatsink temperature**.*
Attention has to be put on comparing TOs and SEMITOP in order to avoid misleading evaluations.

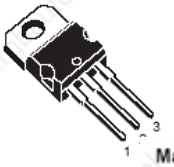
The following figure puts in evidence the current values for a SEMITOP and TO device with the same silicon chip inside but referred to **two different measuring points:**

SK 20 DGDL 065 ET



Absolute Maximum Ratings		T_s= 25°C, unless otherwise specified	
Symbol	Conditions	Values	Units
IGBT - Inverter, Chopper			
V_{CES}		600	V
I_C	T_s = 25 (80) °C	24 (17)	A
I_{CM}	T_s = 25 (80) °C, tp ≤ 1 ms	48 (34)	A
V_{GES}		±20	V
T_j		-40 ... +150	°C
Diode - Inverter, Chopper			
I_F	T_s = 25 (80) °C	25 (18)	A
$I_{FM} = -I_C$		50 (36)	A
T_j		-40 ... +150	°C

Ic @ Ts = T heatsink



Type	V_{CE}	I_C	$V_{CE(sat)}$	T_j	Package	Ordering Code
SGP20N60	600V	20A	2.4V	150°C	TO-220AB	Q67040-S4509
SGB20N60					TO-263AB	Q67041-A4712
SGW20N60					TO-247AC	Q67040-S4236

Ic @ Tc = T case

Maximum Ratings			
Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	600	V
DC collector current	I_C		A
T_C = 25°C		40	
T_C = 100°C		20	

Fig. 4.4 – Current characterization in TO and SEMITOP datasheets

TO characterization does not consider the isolation and at first sight TO device seems to be more performing than SEMITOP.

To assembly different TO's on the same heatsink, users need to guarantee **isolation** between the different parts by means of:

1. **Plastic foil**
2. **Isolated metal substrate (IMS)**
3. **Isolated TO**

1. Insulation by plastic foil

The following picture shows the typical isolation by plastic foil:

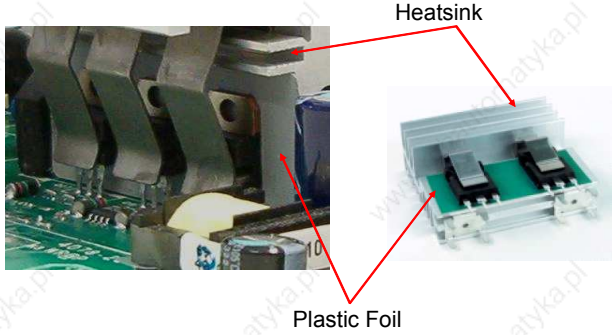


Fig. 4.5 – TO device isolation by plastic foil in a typical application

Comparing the thermal resistance for a same chip mounted on a SEMITOP module and on a TO device, **SEMITOP presents a thermal resistance value lower up to 50% compared to TO devices.**

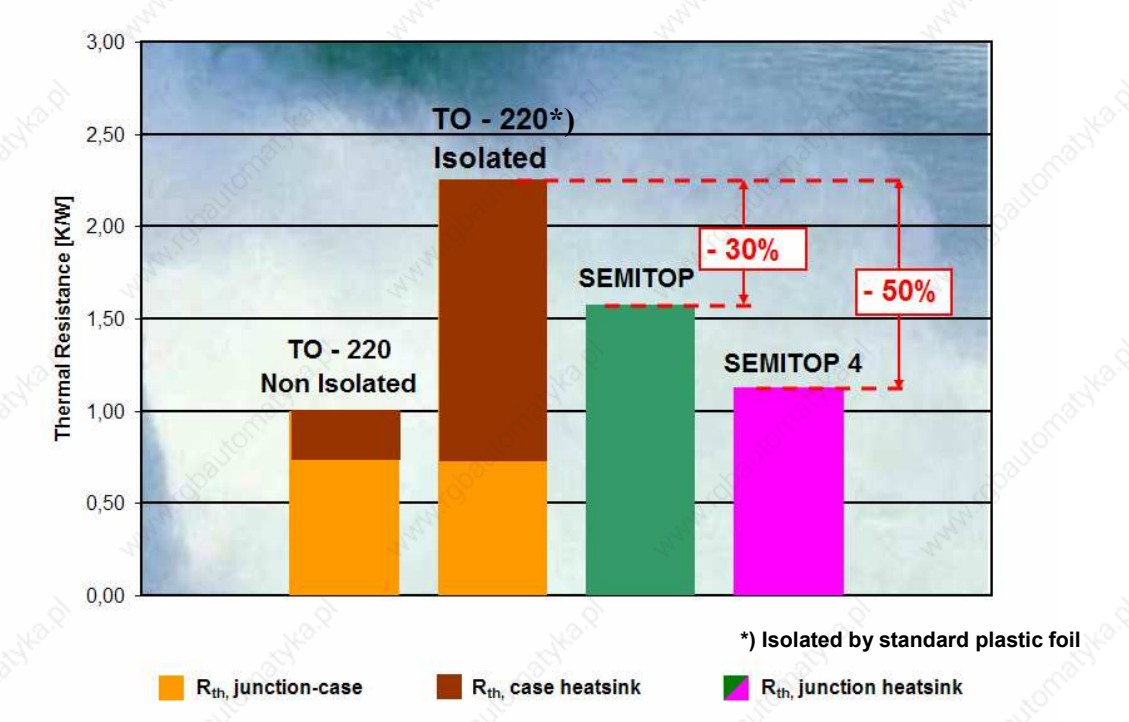


Fig. 4.6 – Rth values comparison between TO devices and SEMITOP

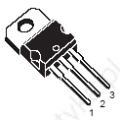
If the current calculation is now referred to the heatsink, that means TO device is now isolated, the new current values are as follow:

SK 20 DGDL 065 ET

SEMITOP® 3

Absolute Maximum Ratings — T_s = 25°C, unless otherwise specified

Symbol	Conditions	Values	Units
IGBT - Inverter, Chopper			
			V
Ic (Ts =80C) =		**17A**	A
			A
V_{GES}		±20	V
T_j		-40 ... +150	°C
Diode - Inverter, Chopper			
I_F	T_s = 25 (80) °C	25 (18)	A
$I_{FM} = -I_{CM}$	T_s = 25 (80) °C, tp ≤ 1 ms	50 (36)	A
T_j		-40 ... +150	°C



Type	V_{CE}	I_C	$V_{CE(sat)}$	T_j	Package	Ordering Code
SGP20N60	600V	20A	2.4V	150°C	TO-220AB	Q67040-S4509
SGB20N60					TO-263AB	Q67041-A4712
SGW20N60					TO-247AC	Q67040-S4236

....ximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CE}	600	V
DC collector current	I_C		A
Ic (Ts =80C, with plastic foil) =		**14A**	

Fig. 4.7 – Current values calculated at the same point (Ts)

Referring to the same characterization point, SEMITOP is more performing compared to isolated TO by plastic foil.

2. IMS insulation

In the following figure the structure of IMS insulation and a typical application:

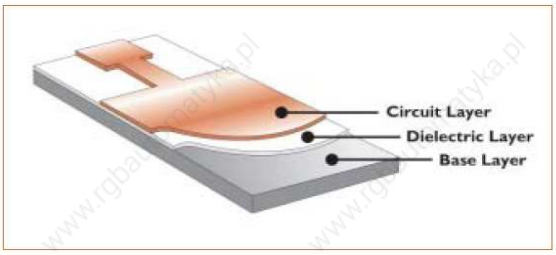


Figure 3: Thermal Clad IMS comprises a circuit layer, a thermally enhanced dielectric layer and a metal substrate.

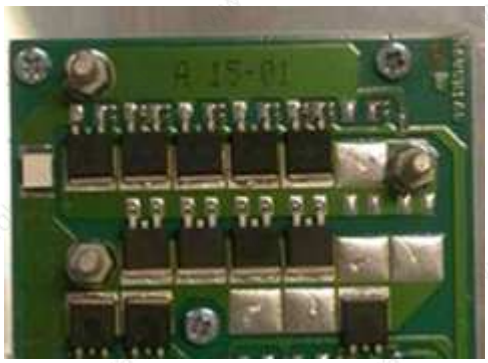


Fig. 4.8 - IMS insulation system

Thermal resistance of TO devices has been measured for different IMS material and temperature cycling test has been performed in order to obtain reliability and performance comparison.
Comparison was made with the same silicon chip inside.
Here the test results:

Temperature cycles TCs between -40°C….+125°C

SEMIKRON qualification program > 100 TCs

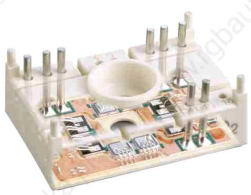
IMS type	Rthjh after 40 TCs	ΔRthjh
Thermal E	21.3K/W	+665%

DELAMINATION

IMS type	Rthjh after 50 TCs	ΔRthjh
25FR	10,24K/W	+ 318%

IMS type	Rthjh Before TCs	Rthjh After 100 TCs	ΔRthjh
MP09006	3,20 K/w	3,85 K/w	+ 20%

SEMITOP	Rthjh after 100 TCs	ΔRthjh
Al_2O_3 DCB	2.30K/W	+/- 0,4 %



The test puts in evidence that only one IMS material passed the test according to SEMIRKON qualification program. The thermal resistance of a TO device isolated with MP09006 IMS material is still higher than the thermal resistance of SEMITOP and its cost is comparable to the cost of a TO device.
TO's with other IMS material showed delamination effects, due to the huge difference between the CTE (coefficient of thermal expansion) of the different materials and did not complete the test.
Due to SKiiP technology, in SEMITOP modules there are not rigid large area connections between materials with different CTE. **Different materials are contacted by a pressure structure**. Any mechanical stress is adsorbed by the structure itself. **That means high reliability**.

The following figure shows the influence of the different CTEs in baseplate modules and in baseplate free modules:

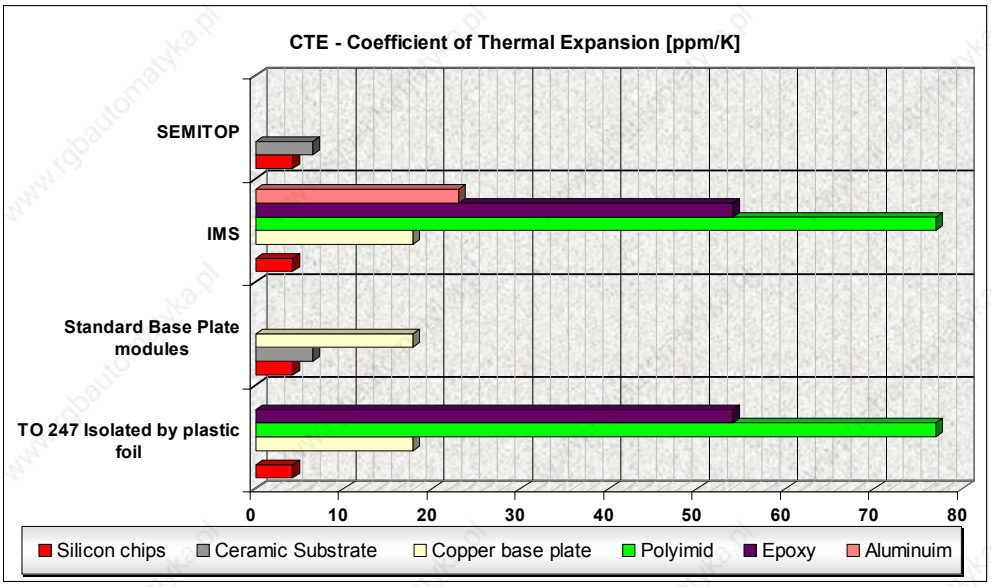


Fig. 4.9 – CTE of material for different modules

The huge difference between the CTE leads to mechanical stresses reducing reliability of the module.

3. ISOLATED TO

Even compared to the latest isolated TOs generations, SEMITOP are able to perform better thermal resistance values.

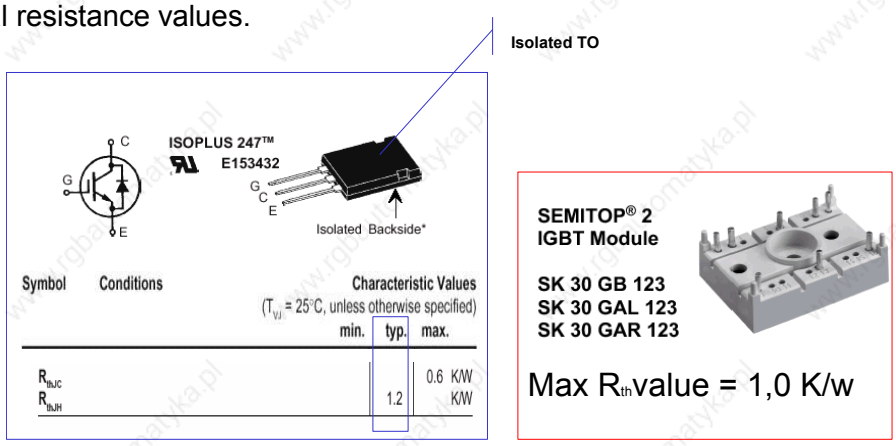


Fig. 4.10 – SEMITOP vs Isolated TO

Compared to TO devices, main SEMITOP® features are:

- **Allow a higher integration level in the various applications;**
- **Ensure a high insulation degree without using any further insulation material;**
- **Offer a highly reliable product:**
- **Better thermal resistance up to 30% lower for SEMITOP®1,2,3 and up to 50% lower for SEMITOP®4**
- **A very high power cycle capability, which means a high reliability;**
- **An integrated solution where the stray parameters (inductance and capacitance) are controlled and lower then discrete solutions.**

If we compare the **components costs**, SEMITOP will be expansive than TO, but we have to consider the application cost that could be substantially reduced using the integrated solution.

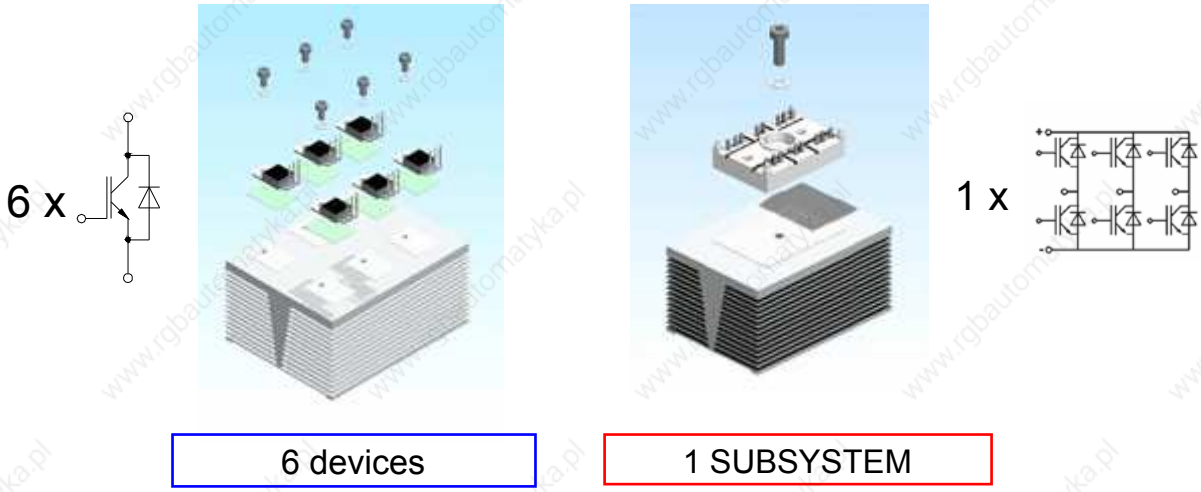


Fig. 4.11 – Assembling steps for TO devices and SEMITOP module for costs comparison

In order to have a significant analysis it has to be considered how the devices are assembled.
To realize a three phase inverter where the TO contains the FWD in the best case, we need **6 TOs**, **6 screws**,**6 washers** and **6 pcs of insulation material**.
With SEMITOP we can easily assembly, in **ONE step and with ONE mounting screw**, the **complete inverter** to the heatsink.
More over SEMITOP® is a complete subsystem 100% tested.

Other costs have to be taken in account like:

- **Mounting costs**
  - Time (less mounting steps)
  - Materials (less part to assembly, e.g. screws)
  - Reduced heatsink treatments (only one hole per module)
- **No isolation material required**
- **Reduced overall dimensions (smaller PCB, smaller heatsink)**

One of the other **benefits** of **SEMITOP is its cost effectiveness.**

4.2 Definition and Measurement of Rth

The maximum junction temperature T_j under static and dynamic load conditions is very important for the power system layout, because it is a key factor for the lifetime of a power system.
The SEMITOP® pressure contact technology connects the DCB substrate thermally to the heatsink; the case temperature T_c cannot be measured directly by a hole through the heatsink that allows the access to the module base.
Therefore only **the thermal resistance junction to sink R_{thj-s} is a measurable parameter** .

4.2.1 Test set up

The following picture shows the measure system for thermal resistance:

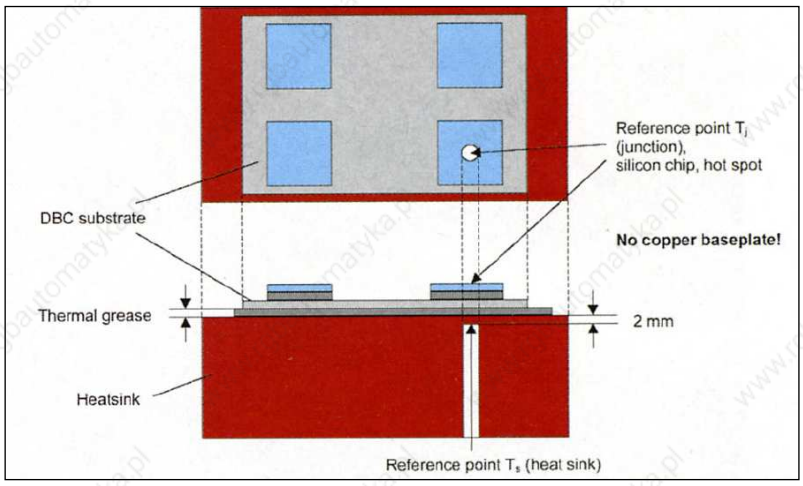


Fig. 4.12 – System set up for R_{th} measurement

The reference point T_s is shifted to a position of 2mm underneath the module inside the heatsink. The distance of 2mm ensures that parasitic effects resulting from heatsink parameters (size, thermal conductivity etc.) are minimised and the disturbance induced by the thermocouple itself is negligible.
At position of hotspot, the heatsink will be drilled towards the bottom of the module to 2mm below the module DBC base (hole diameter of Ø 2.5mm). A thermocouple can be introduced into this hole measuring the reference point Ts.
This method is independent from the DBC layout and results in constant thermal resistance values for the same chip sizes and packaging technology.

4.2.2 Principle of Rth measurement

For modules without a baseplate it is not possible to measure the thermal resistance $R_{th(j-c)}$ and $R_{th(c-s)}$ separately as the baseplate does not exist. The thermal resistance $R_{th(j-s)}$ is evaluated from the virtual junction temperature Tj.

The following physical coherency is used: when operating with a small measurement current, bipolar semiconductor devices show a linear dependence of the voltage drop from the virtual junction temperature.

The module is operated at a constant load current until thermal equilibrium is reached after 60 seconds. After reaching thermal equilibrium, the load current is switched off and a small current of 100mA is applied to the module.

The thermal resistance $R_{th,j-s}$ describes the distribution of temperatures in a system as the reaction to an impressed power P according to the following equation:

$$R_{th,j-s} = \frac{T_j - T_s}{P} \qquad \text{[EQ.1]}$$

The thermal resistance is in general due to the contribute of two terms, resulting in the following equation:

$$R_{th,j-s} = R_{th,j-c} + R_{th,j-s} \qquad \text{[EQ.2]}$$

Since SEMITOP is an **insulated module, the contribute due to the baseplate $R_{th,j-c}$ is null**.
The following picture shows the difference between a module with baseplate and a baseplate free module and the relative contributes of Rth paths:

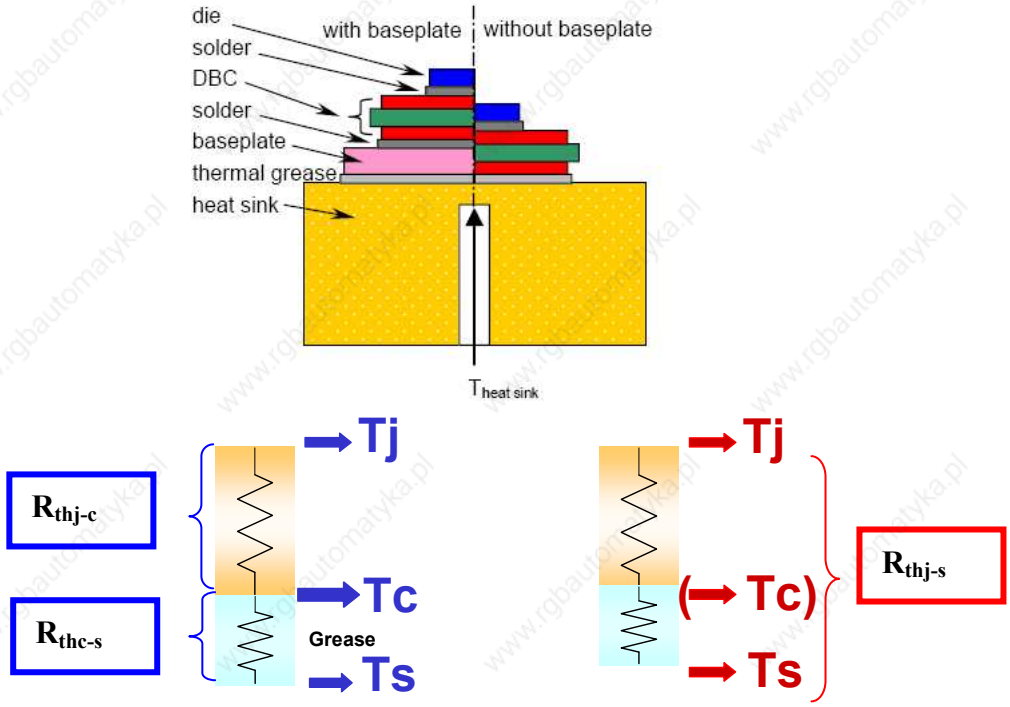


Fig. 4.13 – Different thermal paths in a **base plate module** and in a **baseplate free module**

4.2.3 Transient Thermal impedance Zth

Transient thermal impedance relates the junction temperature rise to a fixed dissipated power.
According to EQ.1, by applying to the chip a step of fixed power value to dissipate and mantaining the heatsink temperature to a fixed value, by measuring the junction temperature variation in the time,it is possible to measure the thermal resistance rise during time until it reaches the steady state value $R_{th,j-s}$.
For a given multilayer structure such as silicon chip, DCB and heatsink, thermal behaviour can be modeled by using an electrical analogy as shown in the following picture:

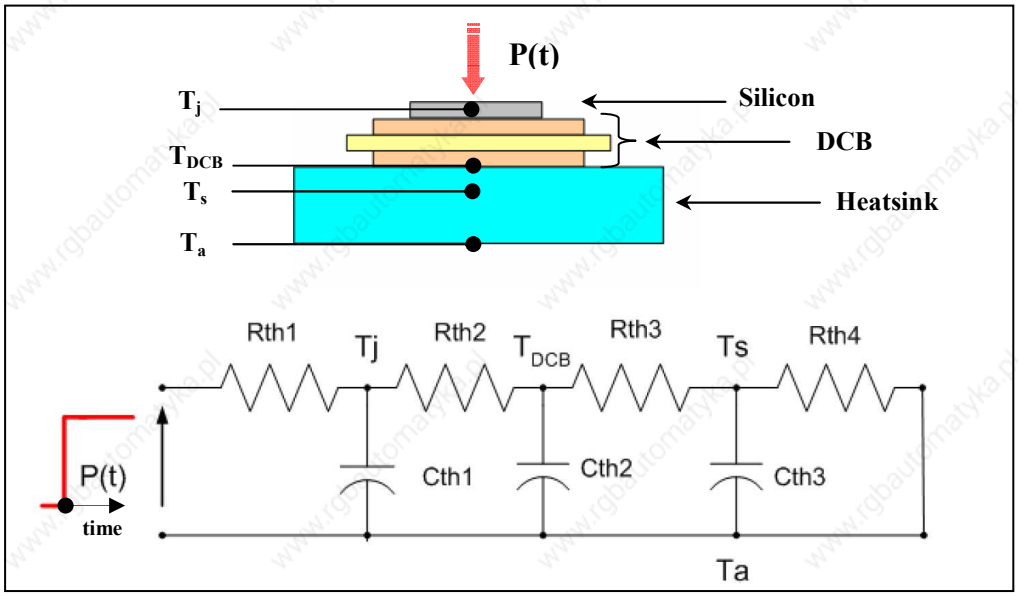


Fig. 4.14 – Multilayer thermal structure and thermal equivalent circuit

$R_{th,i}$ [unit measure K/W] and $C_{th,i}$ [unit measure J/K] are the thermal resistance and the heat capacity values respectively for each path.

Based on measurements, a mathematical thermal model is derived, resulting in the following equation:

$$Z_{th,j-s} = \sum_{i=1}^{4} R_{th,i} \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right) \qquad \text{[EQ.3]}$$

The resultant equivalent electrical model for thermal transient impedance calculation is the following:

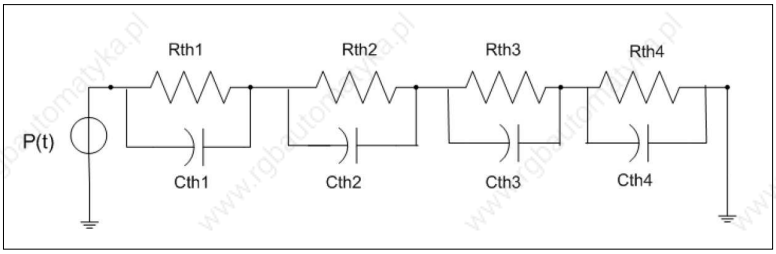


Fig. 4.15 – Thermal model for thermal impedance calculation

In the following picture an example of transient thermal profile obtained by using the EQ.3 for the IGBT and diode integrated in the module SK35GD126ET:

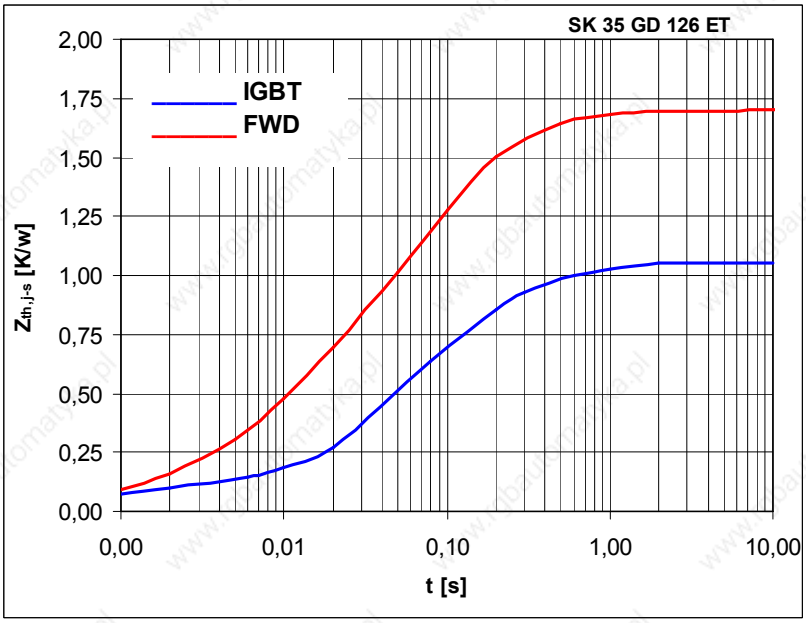


Fig. 4.16 – Example of thermal impedance profile

Thermal impedance profiles for SEMITOP® modules can be supplied on request.

4.3 Specification of the integrated temperature sensor

4.3.1 Electrical characteristic

A standard KG3B-35-5 temperature sensor with NTC (Negative Temperature Coefficient) characteristic is available on some SEMITOP® modules. **The temperature sensor is a resistor soldered on a separate DCB close to the IGBT and diode and reflects the actual heatsink temperature.**
The nominal resistance value at 25°C is 5 kΩ ± 5%.
The temperature-dependent resistance of the NTC sensor is described by the following equation:

$$R_2 = R_1 \cdot e^{\left[B\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right]} \qquad \text{[EQ.4]}$$

where
R_2 : resistance at absolute temperature T_2 [K]
R_1 : resistance at absolute temperature T_1 [K]
B : B-value [K] ($B_{25/85}$ = 3420 K)

The typical NTC characteristic is shown in the figure:

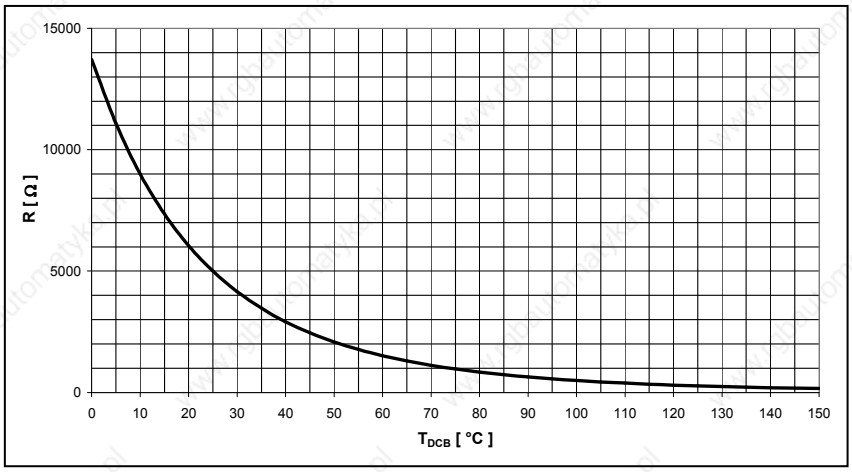


Fig. 4.17 – Typical NTC sensor characteristic

4.3.2 Electrical isolation

Inside the SEMITOP® the temperature sensor is mounted close to the IGBT – and diode dice onto the same substrate. The minimum distance between the copper conductors is ≥ 0.71 mm.

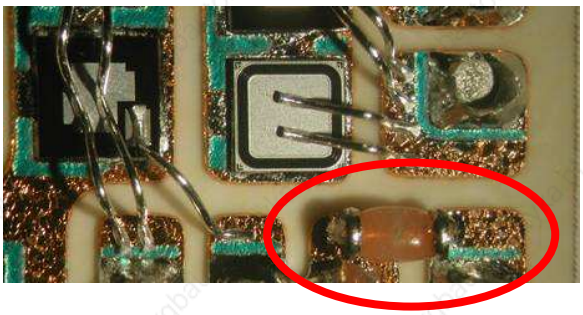


Fig. 4.18 – Position of NTC temperature sensor on DCB substrate

Since the SEMITOP® module is filled with silicon gel for isolation purposes, the requirements for the specified isolation voltage (AC 2.5 kV for 1 min, AC 3 kV for 1 sec) are met and 100% tested.

During short circuit failure and therewith electrical overstress, the bond wires could melt off and so produce an arc with high energy plasma. In this case the direction of plasma expansion is not predictable; the temperature sensor might be touched by plasma and exposed to a high voltage level.
The safety grade “Safe electrical isolation” according to EN 50178 can be achieved by different additional means, described there in detail.

Fig. 4.19 – Sketch of high energy plasma caused by melted off bond wire

SEMITOP® Mounting instructions

ESD protection

IGBT and MOS circuits in SEMITOP® modules are sensitive to electrostatic charges. All SEMITOP® modules are ESD protected during transport, storage and mounting process with an ESD cover.
During the handling and assembly of the modules use a conductive grounded wristlet and working place.

Heat sink specification

The mounting area on the heatsink must be clean and free of grease and particles.
The mechanical specifications for the heat sink are (See Figure 1):

- Flatness: 50 µm per 100 mm
- Roughness Rz : 6,3 µm
- Machined without overlaps

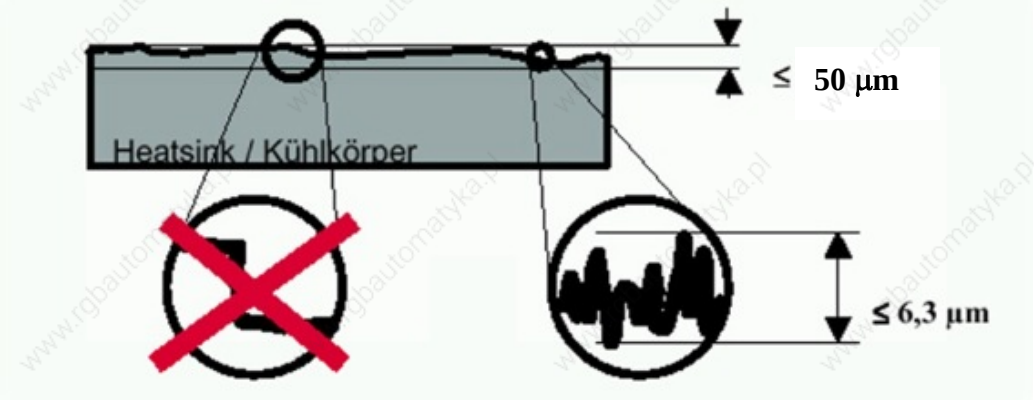


Figure 1 – Heatsink specifications

Mounting surface

- The mounting surface of SEMITOP module must be free from grease and particles.
- Fingerprints or on the bottom side do not affect the thermal behaviour.
- Due to the manufacturing process, the bottom side of the SEMITOP may exhibit scratches, holes or similar marks.
- Discoloration on the bottom side do not affect the thermal behaviour
- The following figures (Figure 2 and Figure 3) define surface characteristics, which do not affect the thermal behaviour.

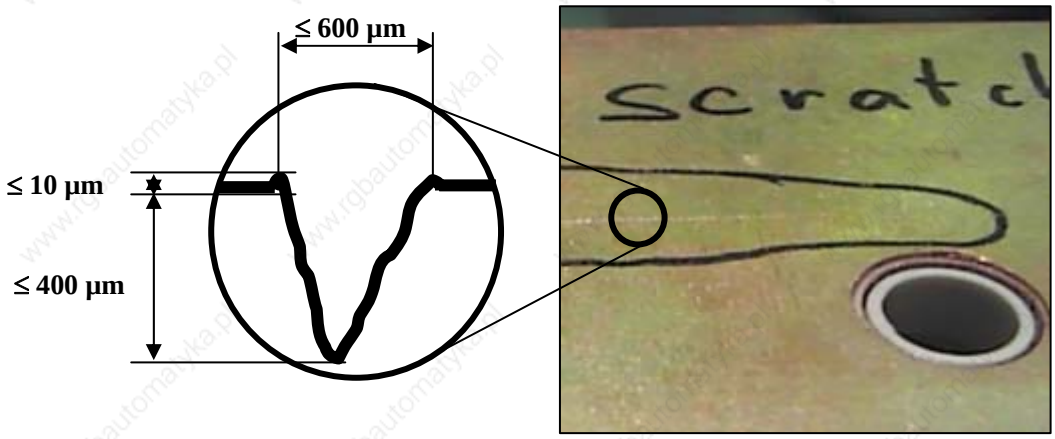


Figure 2 - Scratches on the SEMITOP bottom surface

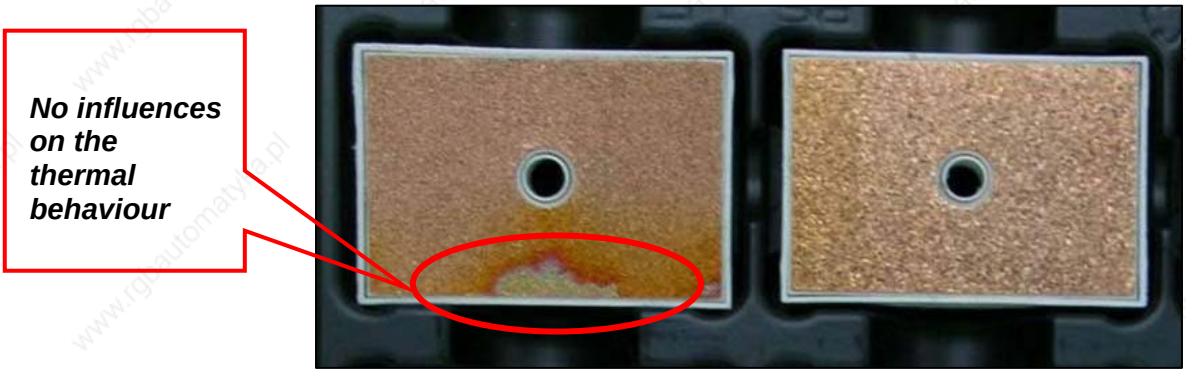


Figure 3 – Discoloration on SEMITOP bottom surface

Assembling Steps

SEMITOP® modules could be assembled by either starting soldering the modules to the PCB (Figure 4) and then fix the subsystem PCB+SEMITOP® to heat sink, or fixing SEMITOP® to the heat sink (Figure 5) and then solder to the PCB.

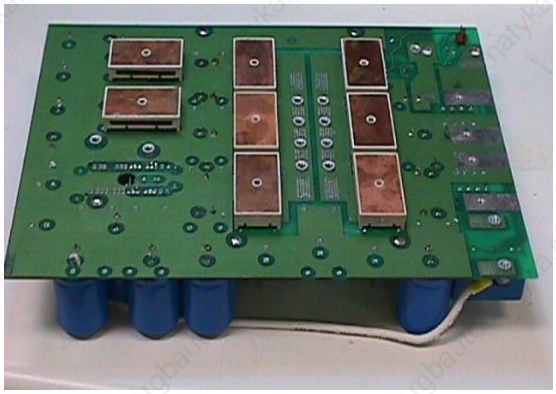


Figure 4 – PCB Assembly

Figure 5 – Heatsink assembly

To avoid any damage to the SEMITOP® modules, it is important to respect important operative conditions during the main assembling steps such as the application of thermal grease, the soldering process and the assembly to the heat sink.

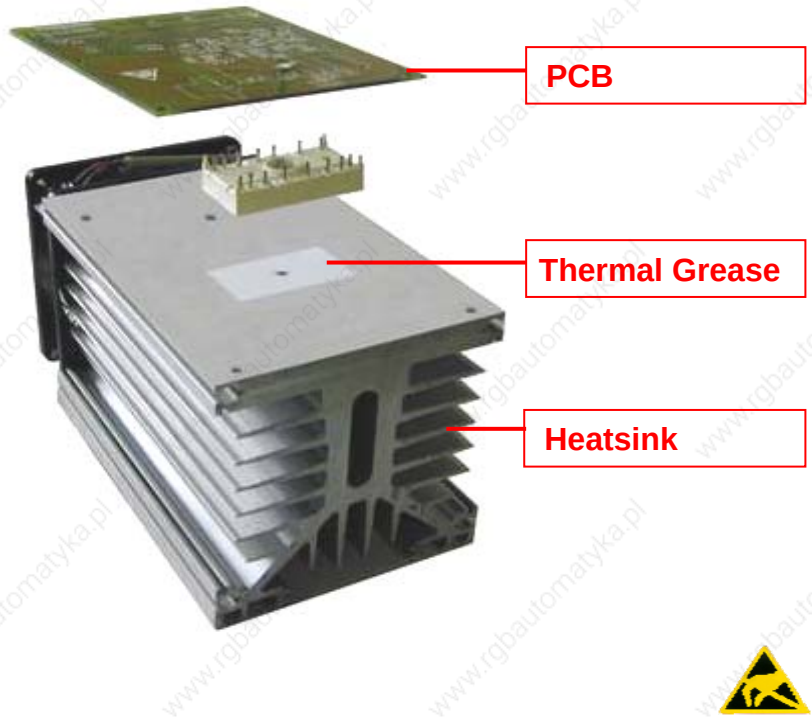


Figure 6 – Assembling steps

Thermal grease application

To avoid air gaps at the interface between the module and the heat sink a thermal grease must be applied.
The function of the grease is to flow according to the shape of the interface, allowing a metal-to-metal contact where it is possible, and filling the remaining gaps.
Recommended thermal grease material is Wacker-Chemie P 12.

SEMIKRON recommends a hard rubber roller or a screen print for an even distribution of the grease.

The thickness of the applied grease layer should be:

Module	Thermal Grease Thickness
SEMITOP® 1	20 – 25 µm (Wacker P12)
SEMITOP® 2	30 – 35 µm (Wacker P12)
SEMITOP® 3	50 – 55 µm (Wacker P12)
SEMITOP® 4	40 – 45 µm (Wacker P12)

The thickness of the applied grease can be checked by a measuring gauge (e.g. Fa. ELCOMETER Instruments GmbH, Himmlingstr. 18, 73434 Aalen, Tel. +49-7366-919283: Sechseck-Kamm 5 - 150 µm).

Assembly on heat sink
After applying the recommended thickness of thermal grease on the heat sink, tighten the screw with the corresponding mounting torque:

Module	Screw	Washer	Maximum Mounting Torque
SEMITOP® 1	DIN 912-M-4x16	DIN 6798 Form A + DIN 125	1,5 Nm +0/-10%
SEMITOP® 2	DIN 912-M-4x16	DIN 6798 Form A + DIN 125	2,0 Nm +0/-10%
SEMITOP® 3	DIN 912-M-4x16	DIN 6798 Form A + DIN 125	2,5 Nm +0/-10%
SEMITOP® 4	DIN 912-M-4x16	DIN 6798 Form A + DIN 7349	2,6 Nm +/- 5%

SEMIKRON recommends:

- a torque wrench with automatic control;
- the above recommended screws and washers;
- tighten the screws only once. After the mounting do not re-tighten the screws to the nominal mounting torque value.
  Due to relaxation of the housing and flow of thermal paste, the loosening torque is lower than the mounting torque. However, the construction of the housing, the washers and the adhesion of the thermal paste still ensure sufficient thermal coupling of the module to the heat sink.
- Do not exceed the mounting torque because a further increase of the maximum mounting torque will not improve the thermal contact but could only damage the module.

Connecting SEMITOP® – PCB

Use plastic anchor pins in each corner on the top of the SEMITOP® for mechanical connection between PCB and SEMITOP®.
To avoid mechanical stress to the soldering pins, the PCB has to be additionally supported (e.g. using spacers).
Suggested hole diameter for the soldering pins and the mounting pins in the PCB is 2mm.

Soldering on PCB

SEMITOP® modules could be soldered to the PCB using the most common soldering process:

- Hand iron;
- Wave soldering process.

Independent of the soldering process used to solder SEMITOP® modules to the PCB, SEMIKRON recommends a thorough evaluation of the solder joints to ensure an optimal connection between SEMITOP® and the PCB.
Figure 7 shows a profile of a good soldered joint. Notice that the solder forms a concave meniscus between pin and pad. This is an example of a properly formed meniscus and it is a result of good wetting during the soldering process.

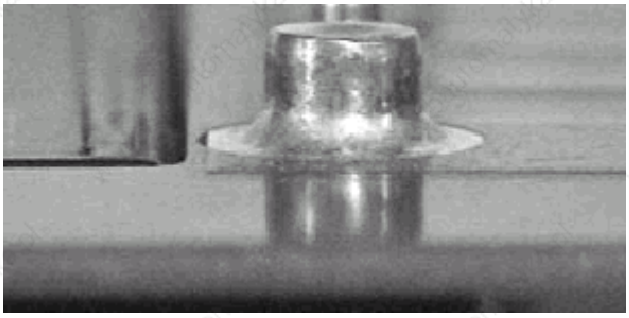


Figure 7 - Good soldered joint profile

In both Figure 7 and Figure 8 it can also be seen that the soldering covers a good deal of the surface area of the pin and of the pad. This is also evidence of good wetting. Notice that the soldering joint has a smooth surface with a silver colour. This is the result of good immobilization of the joint during cooling as well as good cleaning of the board prior to soldering. All soldering connections should exhibit similar characteristics regardless whether they are soldered by hand iron or wave soldering process.

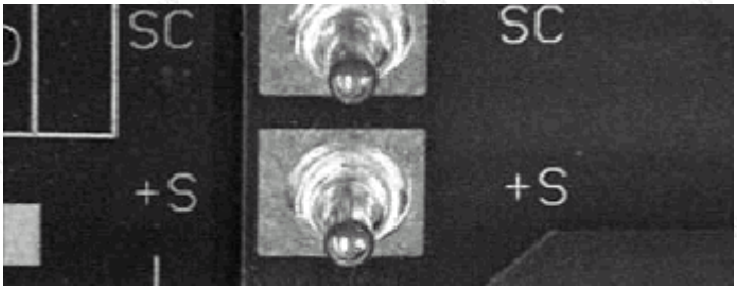


Figure 8 - Details

The time required to create a robust connection depend on several parameters:

a) PCB thickness: When increasing the PCB thickness, the heat dissipation capability of the PCB itself will be the higher, and thus it will require a longer soldering time.

b) Copper wire area: Pins require large copper wire to minimize resistive power losses during the current flowing.
Since copper has a good heat transmission coefficient, the size of these copper wires directly affects the soldering time necessary to heat the PCB pad.

c) Hand iron power: power, tip size and working temperature of the hand iron affect the soldering time. These parameters have to be adjusted in order to keep the maximum temperature within the specified limit.

SEMIKRON recommends that the soldering joints should be thoroughly checked to ensure a high quality soldering joint. If necessary, different parameters should be adjusted in order to optimise the process.

Hand Soldering
SEMIKRON recommends to not exceed the maximum temperature of 260°C for a soldering time of 10seconds.

Wave Soldering Profile
SEMIKRON recommends:

- do not exceed the maximum wave soldering profile of figure 9;
- the maximum preheating temperature has to be kept under or equal to the maximum storage temperature (125°C);
- do not exceed the maximum preheating time of 100seconds;
- during the soldering phase, do not exceed the maximum soldering time of 10 seconds at the maximum temperature of 260°.

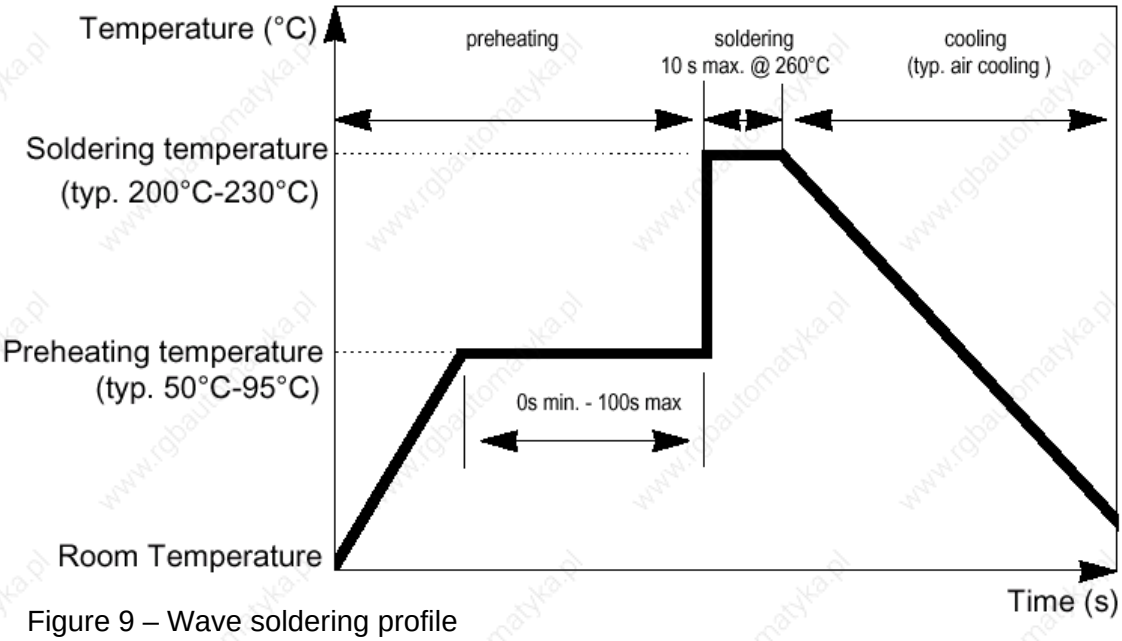


Figure 9 – Wave soldering profile

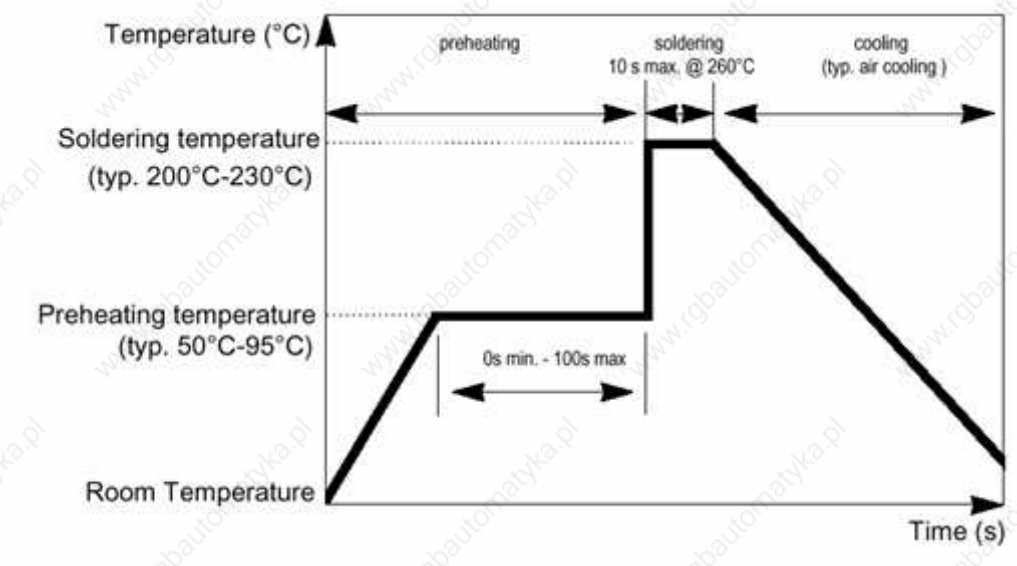


Fig 5.11 – Wave soldering profile

SEMITOP modules could be soldered by a **deep soldering process**; the important is to avoid to exceed the maximum soldering conditions stated in the previous items.

The final connection of power cables to the PCB is made by the use of PCB power connectors. These connectors are designed to be soldered on the PCB. The connection between the PCB power connector and the power terminal of SEMITOP module is through the PCB copper power track. In the following figure some examples of **power terminals for PCB soldering**:

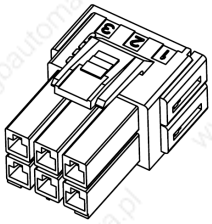
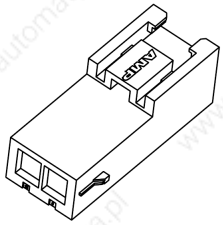
Power connector	Manufacturer	Power connector	Manufacturer
	**Erni**		**Tyco AMP**
			
	**Phoenix Contact**		**Weidmüller**

Fig. 5.12 – Example of PCB power connectors

5.6.2 PCB starter kit

Many designers are considering to use SEMITOP® modules as alternative to IPMs modules due to their flexibility for driver choose.
An application note for a low cost driver design for SEMITOP 3 modules has been implemented: (refer to the following link for details: http://www.semikron.com/internet/webcms/objects/pdf/low_cost_driver_for_semitop_inverter.pdf)
In the picture a detail of the PCB with integrated SEMITOP®3 module that can be supplied on request.

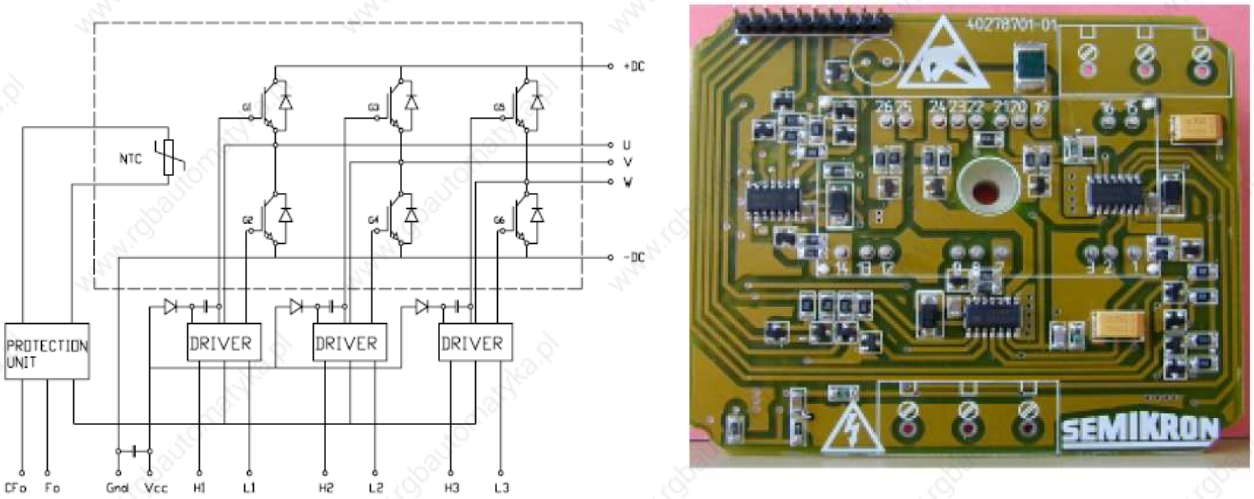


Fig. 5.13 – Example of SEMITOP®3 module with low cost driver integrated

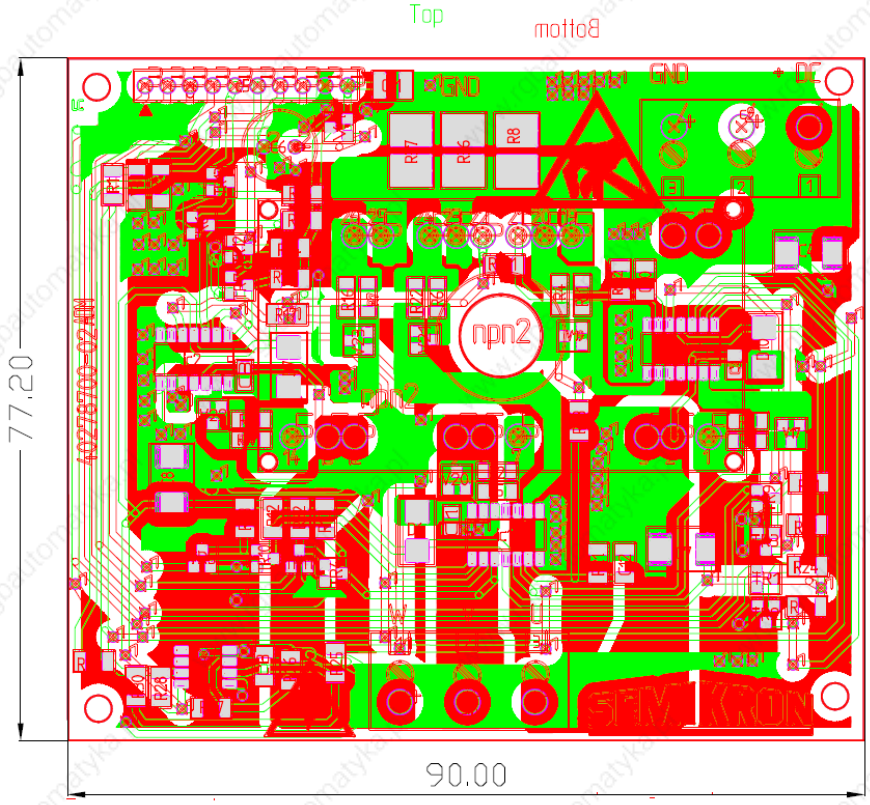


Fig. 5.14 – SEMITOP®3 PCB outline dimensions

Suggested hole diameter in the PCB for pin solders and plastic mounting pins is 2mm.

With the introduction of SEMITOP®4 modules, two PCBs demo board were developed for two specific topologies:

- Demo PCB board for GD topology
- Demo PCB board for DGDL topology

In the following pictures, outline dimensions and schematic are shown,

1. PCB for GD topology SEMITOP4 housing

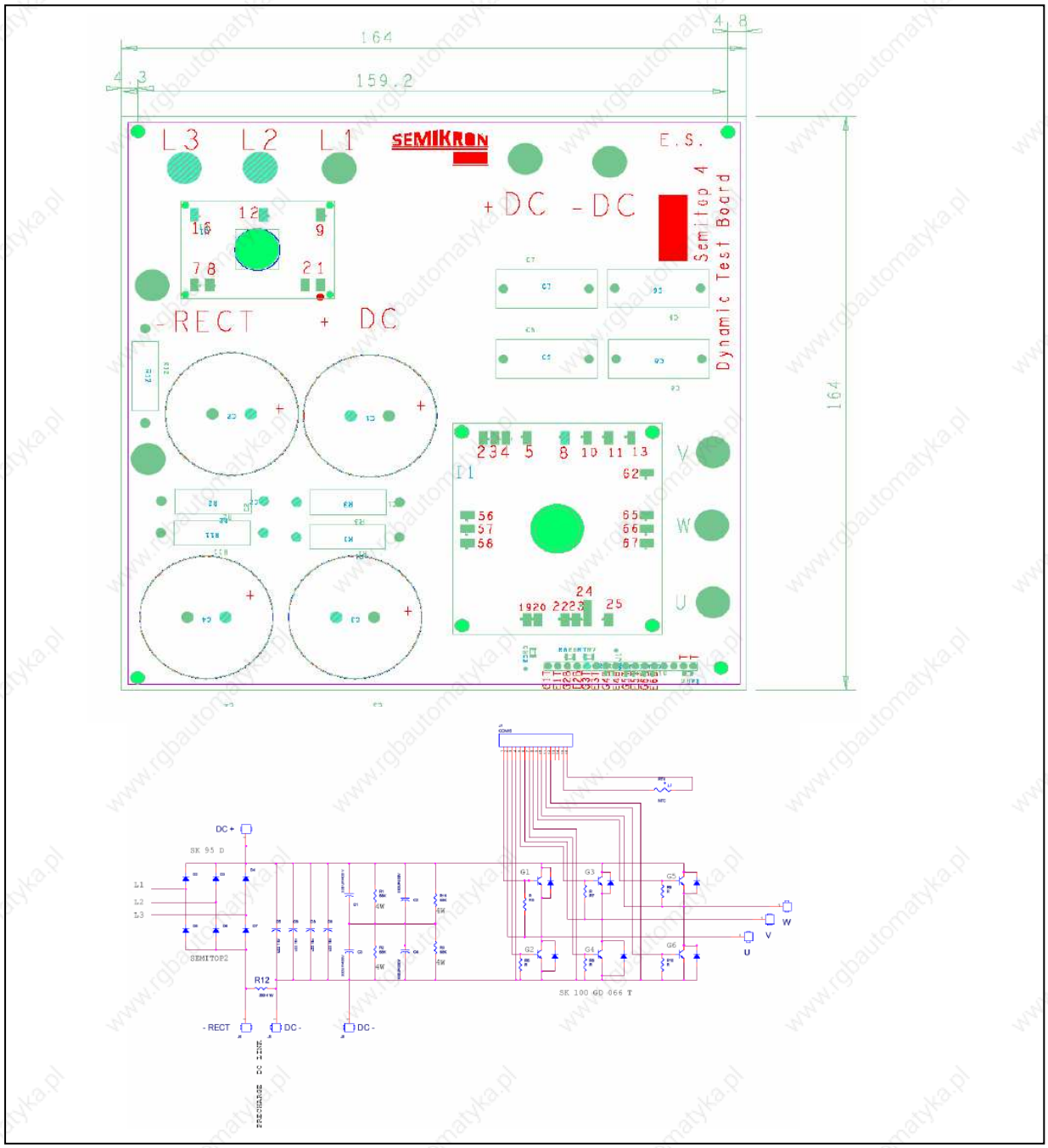


Fig. 5.15 – Demo PCB for GD topology: outer dimensions and schematic

2. PCB for DGDL topology SEMITOP4 housing

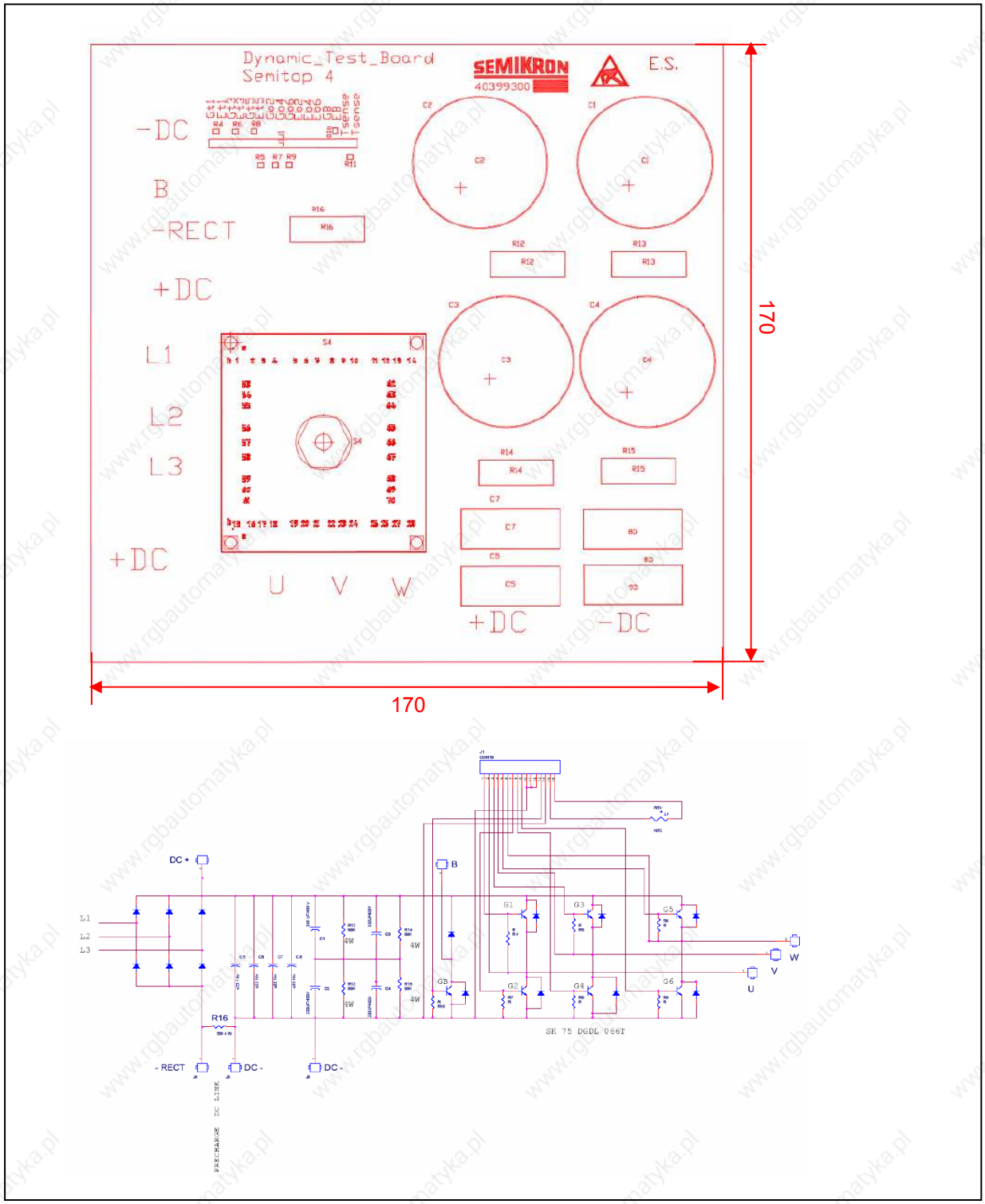


Fig. 5.16 – Demo PCB for DGDL topology: outer dimensions and schematic

These PCBs are intended only for testing purpose and not for mass production.
These demo boards are intended for dynamic test and therefore they are a low stray inductance design. The boards allow as well the use of capacitors and resistor for DC link precharge circuit.

Recommendation: 4 electrolytic capacitors 330uF 400V
4 resistors 68kW/4W, 1 resistor 330W/4W

Suggested hole diameter for the solder pins in the circuit board is 2mm. Suggested hole diameter for the mounting pins in the circuit board is 3,6mm.

Both demo PCB boards are available on request.
Components such as connectors, SMDs etc., are not included in the shipment.

5.7 ESD protection

IGBT and MOS circuits in SEMITOP® modules are sensitive to electrostatic charges. All SEMITOP® modules are ESD protected during transport, storage and mounting process with an ESD cover.
During the handling and assembly of the modules use a conductive grounded wristlet and working place.

6 Technology clarifications

6.1 Pin current capability

The maximum SEMITOP Pin current capability is defined by the boundary conditions of different applications (operating conditions, heatsink temperature, cooling conditions) and cannot be given as one common value (formerly 30A).
The current through the pin depends on the power losses and on the cross section area of the terminals. The solder point is cooled by pin and terminals.
Increasing the cross section area of the SEMITOP connection terminals (i.e using bigger connectors, larger copper strips, wider PCB wires) the maximum allowable DC pin current will be increased.
A SEMITOP3, soldered on a standard FR4 PCB with 105μm copper thickness, was assembled on an P16/120 heatsink without cooling.

The pin temperature rise, at PCB contact, was measured as function of:

- the PCB track width;
- the DC current.

The following measurement of the temperature rise on one pin as function of the DC current had been performed:

a: 1 (one) pin soldered on 4mm width single layer PCB track;

b: 1 (one) pin soldered on 4mm width double layer PCB track;

c: 1 (one) pin soldered on 10mm width double layer PCB track.

The experimental results are shown in the figure:

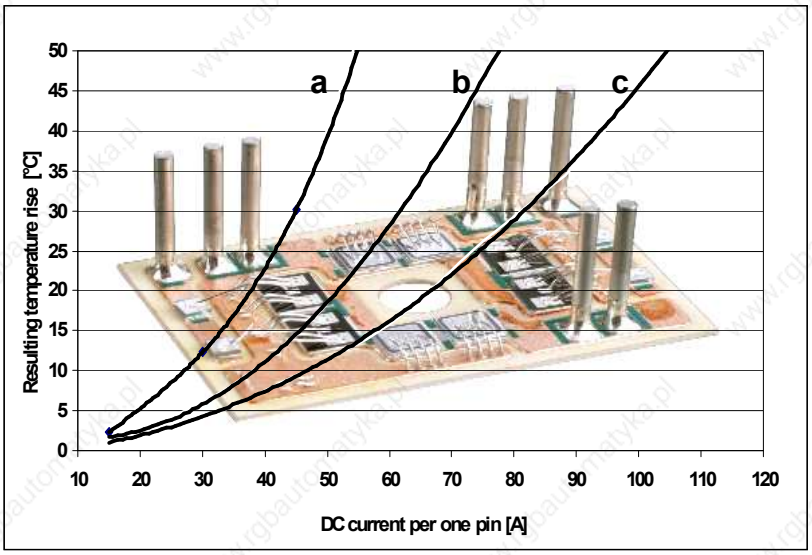


Fig. 6.1 - Pin Temperature rise, at the PCB contact, as function of the PCB track width and of the DC current

The results show as the boundary conditions could influence the pin current capability. These results come from experimental test and are referred to specific boundary conditions. These result SEMITOP modules have been designed in order guarantee that the physical limit is due to the silicon and not by the pin out.

Customers have to take care about the right PCB track dimensioning in order to avoid any PCB over temperature at the pin contact.

6.2 Tin Whisker formation

Electroplated tin layers as used as lead-free solderable finish on the terminations of semiconductor devices are known to form whiskers.
These whiskers are monocrystals of tin and grow within weeks to years with a diameter of some microns up to a length of several hundreds of microns or even millimetres.
Thus they can cause shorts and failure of a whole electronic circuit.
The following picture shows the cross section of a tin layer on copper where large intermetallics can be observed which grow into the tin grain boundaries:

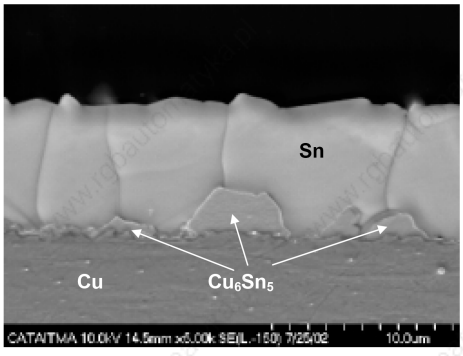


Fig. 6.2 – Electroplated tin on copper with large Cu_6Sn_5 intermetallics

Some studies demonstrate that the whisker formation is due to compressive stresses that can be originated from the co-deposition of organics (e.g. in bright tin layers), from the irregular growth of intermetallics or from temperature variation in combination with large mismatch in CTE (coefficient of thermal expansion) between the base material and the tin layer.
Effective countermeasures to avoid or minimise whisker growth is the deposition of thick tin layers (e.g.7,5 μm minimum) or the use of diffusion barriers as suppressors of irregular intermetallics.

In SEMITOP® modules the whisker formation is avoided with the use of 8 μm tin layer.

6.3 Thermal compound

Thermal grease must be applied to avoid air gaps at the interface between the module and the heat sink.
The function of the grease is to flow according to the shape of the interface, allowing a metal-to-metal contact where it is possible, and filling the remaining gaps.
SEMIKRON recommends **Wacker-Chemie P 12** as thermal grease material.
The thermal resistance junction to heatsink stated in SEMITOP data sheets is valid for SEMITOP modules assembled on the heatsink as described on the SEMITOP mounting instructions.
Other thermal interface materials could be used but has to be put in evidence that the thermal resistance value junction to heatsink could results different from the value stated in the data sheet.
Normalized thermal resistance value junction to heatsink for different thermal foils is shown in fig. 4.6
Thermal foils usually perform the best thermal resistance value after a curing phase.

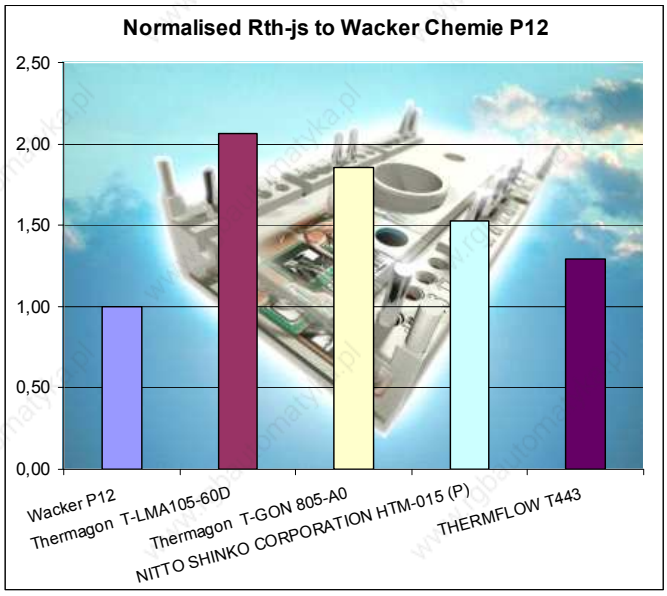


Fig. 6.3 - Normalized Thermal resistance value junction to heatsink for different thermal compound

Analysed thermal foils, even after the curing phase, present worst thermal resistance values compared to the thermal resistance value measured using SEMIKRON recommended **Wacker-Chemie P 12** thermal grease.
This has to be kept in consideration in order to avoid any junction over heating. Other comparative measurements could be performed on request.

7 Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)

SEMITOP® modules are a lead-free design in accordance with the stipulations of the EU Directive proposal 2002/95/EG.
The usage of lead-free products is a strong customer requirement for all future designs. This is especially mandatory for some parts of Asia.
SEMITOP® terminals are tin plated and are soldered to the DCB using lead free solder, SnAg(3,5).
There are no problem in using lead free solder with SEMITOP modules (Test had been performed in Reference to IEC 68-2-20A).

8 Laser marking

All SEMITOP® modules are laser marked. The following figure shows the result of a laser marking on a SEMITOP® module:

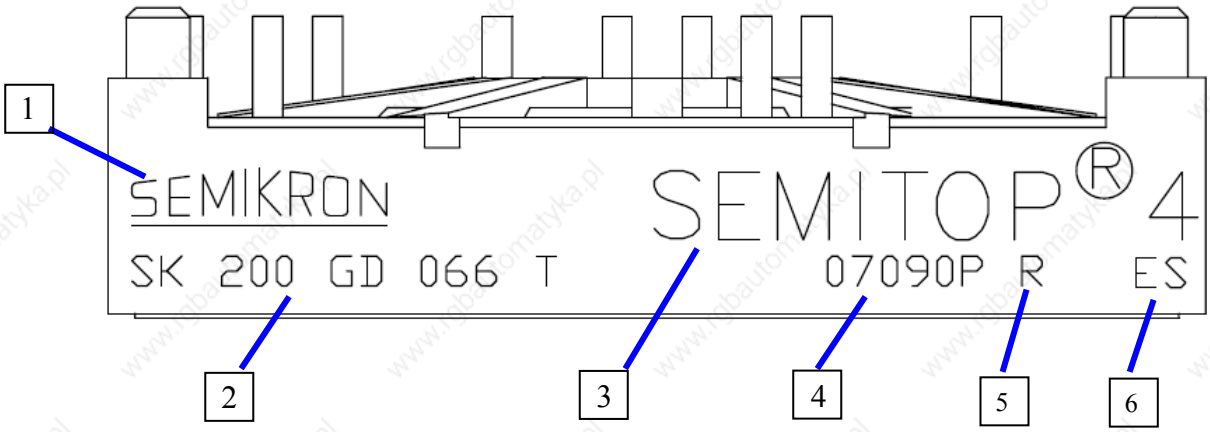


Fig. 8.1 – SEMITOP laser marking

The marking contains the following items :

1	=	SEMIKRON logo
2	=	Type designation
3	=	Type of SEMITOP module
4	=	Data code: 6 digits →YYWWL (L= lot)
5	=	“R” identification for RoHS compliance
6	=	“ES” stands for Engineer Sample. All SEMITOP® modules will be laser marked with this label until the release for zero series production.

9 Packing specification

9.1 Packing box

SEMITOP® modules are all packed in a standard box:

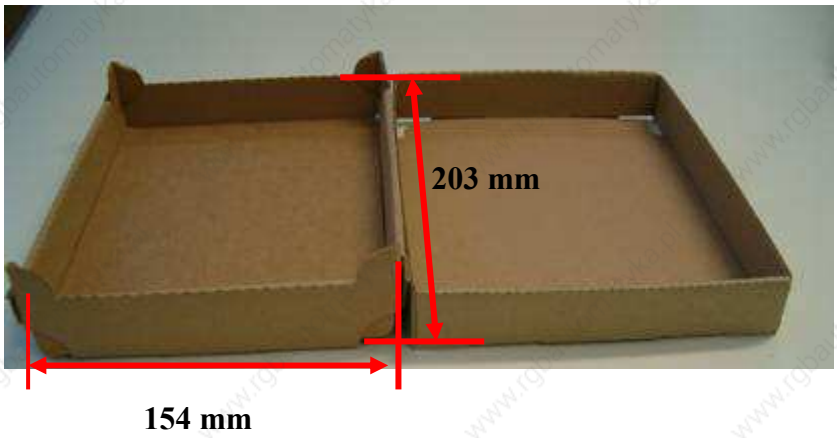


Fig. 9.1 – SEMITOP packaging

The modules are inserted in ESD (not electrically chargeable) blister:

Fig. 9.2 – ESD blister with module inside

The quantities per package are: **SEMITOP® 1** : 16 modules
SEMITOP® 2 : 15 modules
SEMITOP® 3 : 10 modules
SEMITOP® 4 : 6 modules

9.2 Marking of packing boxes

All SEMITOP® packing boxes are marked with a sticker label.
This label is placed on the packing box as in the following figure:

Fig. 9.3 – Place for label on SEMITOP® packing boxes

The yellow label means that the packing contains electrostatic sensitive devices.
The label contains the following items:

Fig. 9.4 – Label of SEMITOP® packing boxes

1 = SEMIKRON logo

2 = Type designation

3 = Data code with 6 digits “YYWWL”. L=lot of production. “R” means the module is RoHS compliance

4 = Lot number

5 = Quantity per package (depending from module type) with relative bar code

6 = part number of the module with relative bar code

7 = barcode made by 12 digits that should identify univocally every SEMIBOX

New barcode contents:

- 2 digits to identify SK-C origin (IT for Italy)
- 1 digit to identify the department originating the SEMIBOX
- 2 digits for the year
- 2 digits for the week
- 5 digits sequential number

Barcode example: ITA073012345
The new label will maintain the same overall dimensions

9.3 Storage conditions

The shelf life for SEMITOP products can be summarised as follow:

packed	Temperature range	-40°C … +125°C
	Humidity range	< 85% RH
	Application time limit	24 months without dew
opened	Temperature range	-40°C … +125°C
	Humidity range	< 85% RH
	Application time limit	24 months without dew

10 Reliability

10.1 Qualification test and special test

All SEMITOP® modules passed the following qualification tests:

No	Test	Test Conditions	Standard	Samples
01	High Temperature Reverse Bias Rectifier	1000h, DC, 66% of voltage grade Tc=Tvjmax-20K, max. 120°C		0/6
02	High Temperature Reverse Bias Mos IGBT 600/1200 V 1700 V	1000h, V_{GE} = 0V 95% V_{DSmax} / V_{CEmax}, Tc = 145°C Tc = 140°C Tc = 125°C	IEC 60747	0/6
03	High Temperature Gate Stress	1000h, ± V_{GSmax} / V_{GEmax}, T_{vjmax}	IEC 60747	0/6
04	High Humidity High Temperature Reverse Bias	1000h , 85°C, 85% RH V_{DS}/V_{CE}= 80% V_{DSmax}/V_{CEmax}, max. 80V, V_{GE} = 0V	IEC 60068 Part 2-67	0/6
05	High Humidity High Temperature Reverse Bias Inverter	1000h , 85°C, 85% RH V_{DS}/V_{CE}= 80% V_{DSmax}/V_{CEmax}, max. 80V, V_{GE} = 0V	IEC 60068 Part 2-67	0/6
06	High Temperature Storage	1000h, T = + 125°C	IEC 60068 Part 2-2	0/6
07	Low Temperature Storage	1000h, T = - 40°C	IEC 60068 Part 2-1	0/6
08	Temperature Cycling	100 cycles - 40°C + 125°C	IEC 60068 Part 2-14 Test Na	0/6
09	Power Cycling	20000 load cycles ΔT_j = 100K	IEC 60747	0/4
10	Resistance to solder	260°C ± 5°C 10 sec ± 1 sec	IEC 60068 Part 2-20 Test Tb	0/4
11	Solderability	235°C ± 5°C Ageing 3	IEC 60068 Part 2-20 Test Ta	0/4
12	Vibration	Sinusoidal Sweep, 5 g, x, y, z – axis, 2h/axis	IEC 60068 Part 2-6 Test Fc	0/4
13	Shock	Halfsinusoidal Pulse, 30 g, ±x, ±y, ±z direction, 3x/direction	IEC 60068 Part 2-27 Test Ea	0/4
14	Tensile Strength		IEC 60068 Part 2-21 Test Ua1	0/4

SEMITOP® modules also passed the following **special tests:**

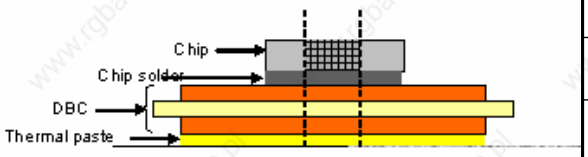
- **Vibration test** (up to 10g along 3 axes) according to Q101 Rev. May 15, 1996 **"Stress test qualification for automotive grade discrete semiconductors"** There was no change in static parameter before and after the test.
- **Salt Spray Test** according mil-std-810F method 509.4 +JESD22-a107-a
- **Corrosive Atmosphere test** according to DIN EN 60068-2-60Ke method 3including SO_2 in addition to H_2S, NO_2 and Cl_2 (see table below)

condition	unit	SEMIKRON test conditions
H_2S	[ppm]	0,4
NO_2	[ppm]	0,5
Cl_2	[ppm]	0,1
SO_2	[ppm]	0,4
T	[°C]	25
RH	%	75
duration	days	21

Fig. 10.1 – Summary of Special test for SEMITOp modules

10.2 Lifetime calculation

Lifetime of power modules is limited by mechanical stresses that occur among the different materials of the package during working. These mechanical stresses are due to the different CTEs (coefficient of thermal expansion) of such materials.
A cross section of SEMITOP®4 module and the corresponding CTEs values are shown in the following picture:



Material	Thickness [mm]	CTE [10^{-6}/°C]
Chip	0,203	3,2
Chip solder	0,130	28
DBC (copper)	0,3	16,7
DBC (Al_2O_3)	0,38	6-7
DBC (copper)	0,2	16,7

Fig. 10.1 – SEMITOP®4 layers cross section and CTEs for the different materials

During heating up and cooling of a module the different materials expand according to their different CTEs; these materials are joined and therefore they don't expand freely and this leads to the above mentioned mechanical stresses. Result is that after a certain number of power cycles the module fails. Typical example is the wire bond "lift off", that means contact between chip (or DCB copper) and wire bonds is lost (refer to the picture below):

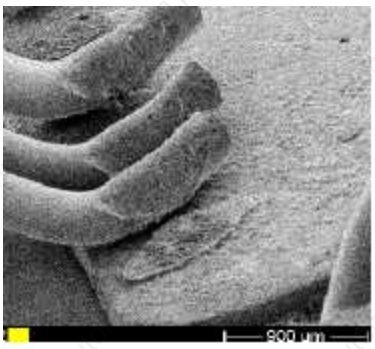


Fig. 10.2 – Typical wire bonding lift-off observed to the electron microscope

Lifetime of a module is related to the temperature swing that is the difference between the maximum reached temperature and the minimum temperature value. So, lifetime is determined from the power cycle of a module. The bigger is the temperature difference, the more stress is induced.
Different investigations have been carried in this area, including a research project known as “LESIT study”. This study puts in evidence the relationship between the number of cycles, the junction temperature difference and the medium temperature.

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \qquad \text{[EQ.5]}$$

with: N_f = number of power cycles
k_B = Boltzmann-constant ($1{,}380 \cdot 10^{-23}$ JK^{-1})
E_a = activation energy ($9{,}89 \cdot 10^{-20}$ J)
A = constant (302500 $K^{-\alpha}$)
α = constant (-5,039)
T_{jm} = medium junction temperature [K]

SEMITOP® modules are baseplate free technology. Curves for lifetime estimation of baseplateless modules can be extrapolated from the existing LESIT curve, to obtain the ones in the following picture:

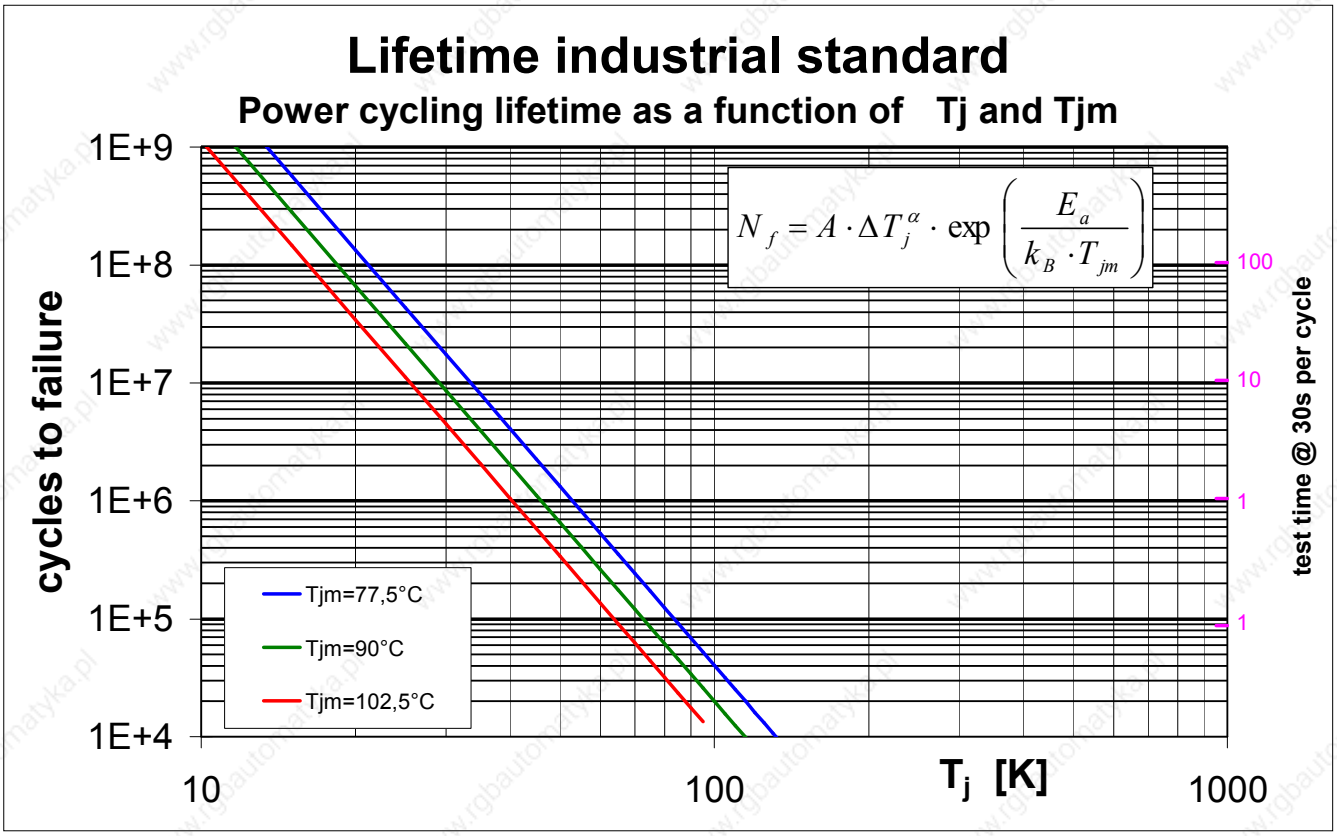


Fig. 10.3 – Lifetime estimation for modules without base plate

SEMITOP modules integrating IGBT4 and CAL4 can operate up to 150°C (175°C maximum junction temperature). By chip wire bonding optimization, 25K higher junction temperature swing is achieved now, not reducing life time cycle of the device.
The following curve for lifetime prediction has to be used for SEMITOP modules integrating IGBT4 and CAL4:

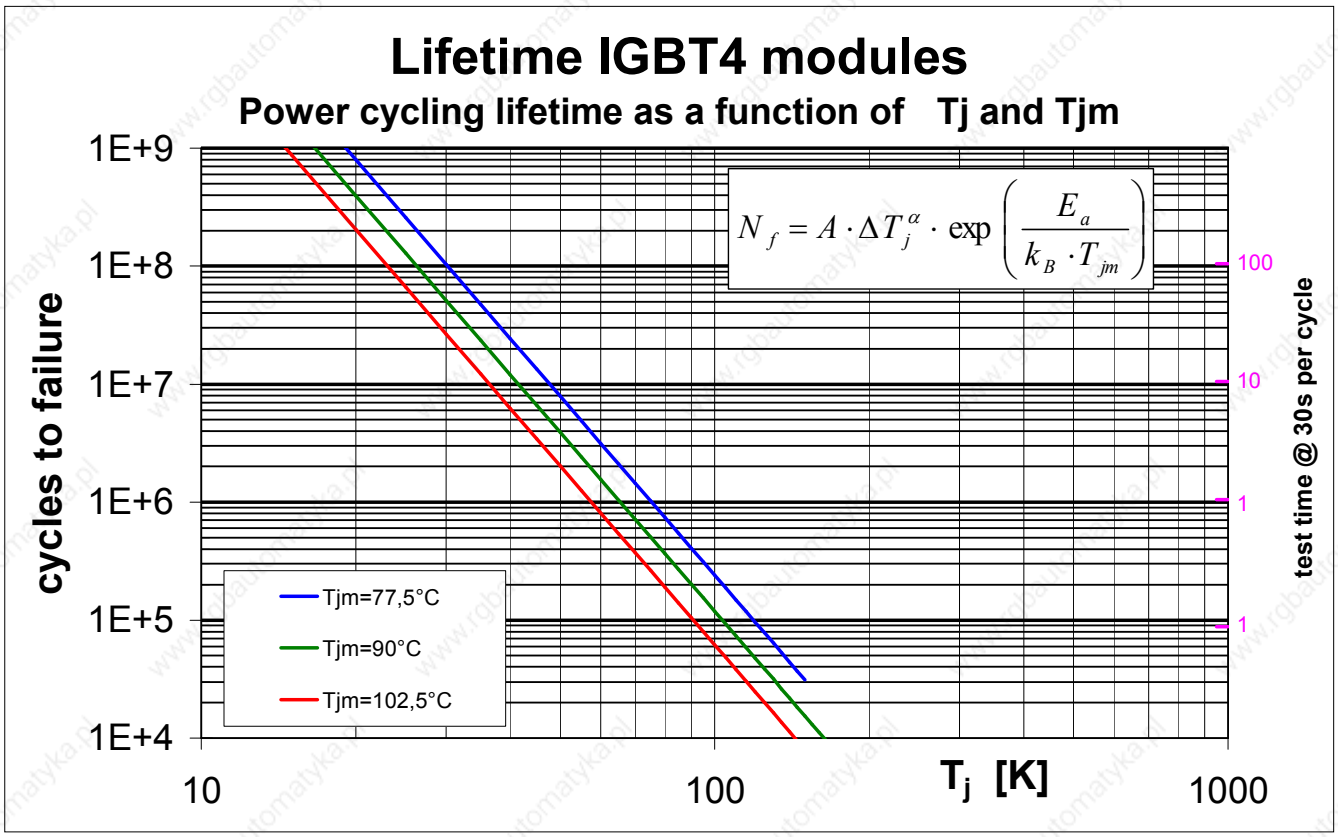


Fig. 10.4 – Lifetime estimation for modules without base plate integrating IGBT4/CAL4

