EMIPAK 2B PressFit Power Module
3-Levels Half Bridge Inverter Stage, 150 A

EMIPAK-2B
(package example)

FEATURES

- Trench IGBT technology
- FRED Pt® clamping diodes
- PressFit pins technology
- Exposed Al_2O_3 substrate with low thermal resistance
- Short circuit rated
- Square RBSOA
- Integrated thermistor
- Low internal inductances
- Low switching loss
- PressFit pins locking technology. Patent # US.263.820 B2
- UL approved file E78996
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

DESCRIPTION

VS-ETF150Y65N is an integrated solution for a multi level inverter stage in a single package. The EMIPAK 2B package is easy to use thanks to the PressFit pins and the exposed substrate provides improved thermal performance. The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

PRIMARY CHARACTERISTICS	
Q1 to Q4 IGBT	
V_{CES}	650 V
$V_{CE(on)}$ typical at I_C = 150 A	1.70 V
I_C at T_C = 82 °C	150 A
Speed	8 kHz to 30 kHz
Package	EMIPAK 2B
Circuit configuration	3-levels half bridge inverter stage

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
Operating junction temperature	T_J		175	°C
Storage temperature range	T_{Stg}		-40 to +150	
RMS isolation voltage	V_{ISOL}	T_J = 25 °C, all terminals shorted, f = 50 Hz, t = 1 s	3500	V
Q1 to Q4 IGBT				
Collector to emitter voltage	V_{CES}		650	V
Gate to emitter voltage	V_{GES}		20	
Pulsed collector current	I_{CM}		450	A
Clamped inductive load current	I_{LM}		180	
Continuous collector current	I_C	T_C = 25 °C	201	A
		T_C = 60 °C	171	
		T_{SINK} = 60 °C	77	
Power dissipation	P_D	T_C = 25 °C	600	W
		T_C = 60 °C	460	
D5 - D6 CLAMPING DIODE				
Repetitive peak reverse voltage	V_{RRM}		650	V
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	750	A
Diode continuous forward current	I_F	T_C = 25 °C	161	
		T_C = 60 °C	140	
		T_{SINK} = 60 °C	74	
Power dissipation	P_D	T_C = 25 °C	319	W
		T_C = 60 °C	245	

PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and International patents.

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MAX.**	**UNITS**
D1 - D2 - D3 - D4 AP DIODE				
Single pulse forward current	I_{FSM}	10 ms sine or 6 ms rectangular pulse, T_J = 25 °C	500	A
Diode continuous forward current	I_F	T_C = 25 °C	102	
		T_C = 60 °C	92	
		T_{SINK} = 60 °C	57	
Power dissipation	P_D	T_C = 25 °C	238	W
		T_C = 60 °C	182	

Notes

- Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur

(1) V_{CC} = 325 V, V_{GE} = 15 V, L = 500 µH, R_g = 4.7 Ω, T_J = 175 °C

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Q1 to Q4 IGBT						
Collector to emitter breakdown voltage	BV_{CES}	V_{GE} = 0 V, I_C = 100 µA	650	-	-	V
Collector to emitter voltage	$V_{CE(on)}$	V_{GE} = 15 V, I_C = 150 A	-	1.70	2.17	
		V_{GE} = 15 V, I_C = 150 A, T_J = 125 °C	-	1.95	-	
Gate threshold voltage	$V_{GE(th)}$	V_{CE} = V_{GE}, I_C = 5.0 mA	5.0	6.0	8.4	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_J$	V_{CE} = V_{GE}, I_C = 1.0 mA (25 °C to 125 °C)	-	-18	-	mV/°C
Forward transconductance	g_{fe}	V_{CE} = 20 V, I_C = 150 A	-	102	-	S
Transfer characteristics	V_{GE}	V_{CE} = 20 V, I_C = 150 A	-	10.2	-	V
Zero gate voltage collector current	I_{CES}	V_{GE} = 0 V, V_{CE} = 650 V	-	0.1	100	µA
		V_{GE} = 0 V, V_{CE} = 650 V, T_J = 125 °C	-	130	-	
Gate to emitter leakage current	I_{GES}	V_{GE} = ± 20 V, V_{CE} = 0 V	-	-	± 600	nA
D5 - D6 CLAMPING DIODE						
Cathode to anode blocking voltage	V_{BR}	I_R = 500 µA	650	-	-	V
Forward voltage drop	V_{FM}	I_F = 100 A	-	1.64	2.2	
		I_F = 100 A, T_J = 125 °C	-	1.35	-	
Reverse leakage current	I_{RM}	V_R = 650 V	-	0.3	100	µA
		V_R = 650 V, T_J = 125 °C	-	100	-	
D1 - D2 - D3 - D4 AP DIODE						
Forward voltage drop	V_{FM}	I_F = 100 A	-	2.1	2.9	V
		I_F = 100 A, T_J = 125 °C	-	1.64	-	

SWITCHING CHARACTERISTICS (T_J = 25 °C unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Q1 to Q4 IGBT						
Total gate charge (turn-on)	Q_g	I_C = 150 A V_{CC} = 400 V V_{GE} = 15 V	-	310	-	nC
Gate to emitter charge (turn-on)	Q_{ge}		-	95	-	
Gate to collector charge (turn-on)	Q_{gc}		-	130	-	
Input capacitance	C_{ies}	V_{GE} = 0 V V_{CC} = 30 V f = 1 MHz	-	9900	-	pF
Output capacitance	C_{oes}		-	460	-	
Reverse transfer capacitance	C_{res}		-	250	-	