Socapel PAM

A Programmable Axes Manager

PAM Simatic S5

Technical Manual

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This upgraded and improved version replaces all the previous. We reserve the right to amend this document without prior notice and decline all responsibilities for eventual errors.

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1 PAM SIMATIC S5 TECHNICAL MANUAL

1.1 MANUAL SCOPE

This manual is intended to serve as a reference for individuals who will be using the PAM Simatic S5. It provides details on the hardware aspects of the Simatic interface for PAM.

The scope of this manual is limited to the PAM Simatic S5. For a complete listing of all technical publications covering PAM and its associated peripherals (i.e. ST1, Smart I-O, VME Bus Master, etc..), refer to the Technical Publications Overview in the PAM User's Manual (p/n 006.8017.A) and to the Technical Documentation, Available Manuals list (p/n 080.8010).

1.2 MANUAL ORGANIZATION AND CONTENTS

This manual is organized into four chapters. The following is a summary of the manual contents by chapter:

Chapter 1	Description of manual organization and contents
Chapter 2	PAM Simatic S5 description
Chapter 3	PAM Simatic S5 configuration
Chapter 4	Analog outputs description

2 INTRODUCTION

2.1 GENERAL INFORMATION

The PAM - Programmable Axes Manager - is a module developed by Atlas Copco Controls to precisely control and synchronize multiple ST1 digital motion controllers. The PAM and all ST1 controllers are interconnected on EasyBus, a proprietary optical fiber fieldbus (see Figure 1).

The PAM Simatic S5 is a PAM with a fully integrated Simatic S5 interface which permits communications with a Siemens Simatic S5 PLC host via the S5 parallel bus. The PAM Simatic S5 is designed to be installed directly in an available slot of a Simatic S5 PLC. Two connectors at the back of the unit mate directly with S5 data bus connectors on the S5 PLC backplane.

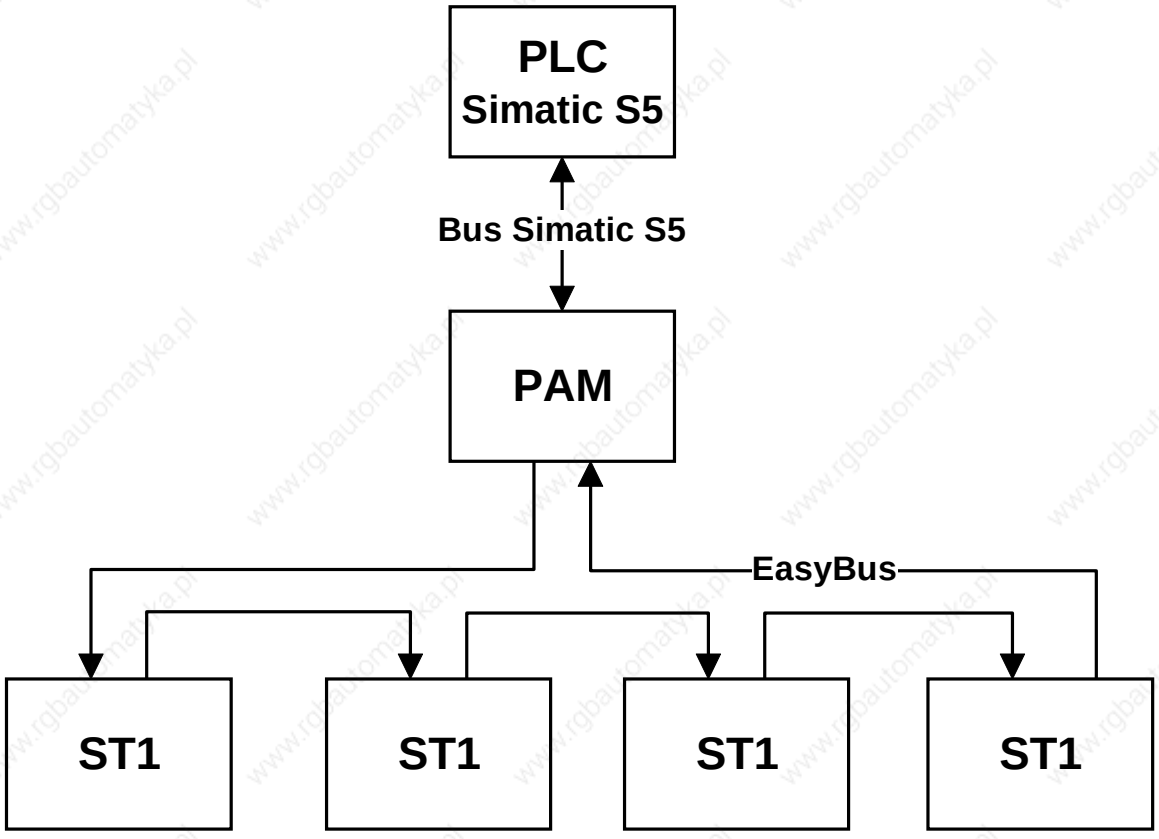


Figure 1: PAM Simatic S5 System Architecture

2.2 PAM SIMATIC S5 ARCHITECTURE

PAM is based on a high performances RISC processor. Supporting this processor (see Figure 2) are memory, a serial interface, the EasyBus interface, analog outputs and the Simatic S5 interface.

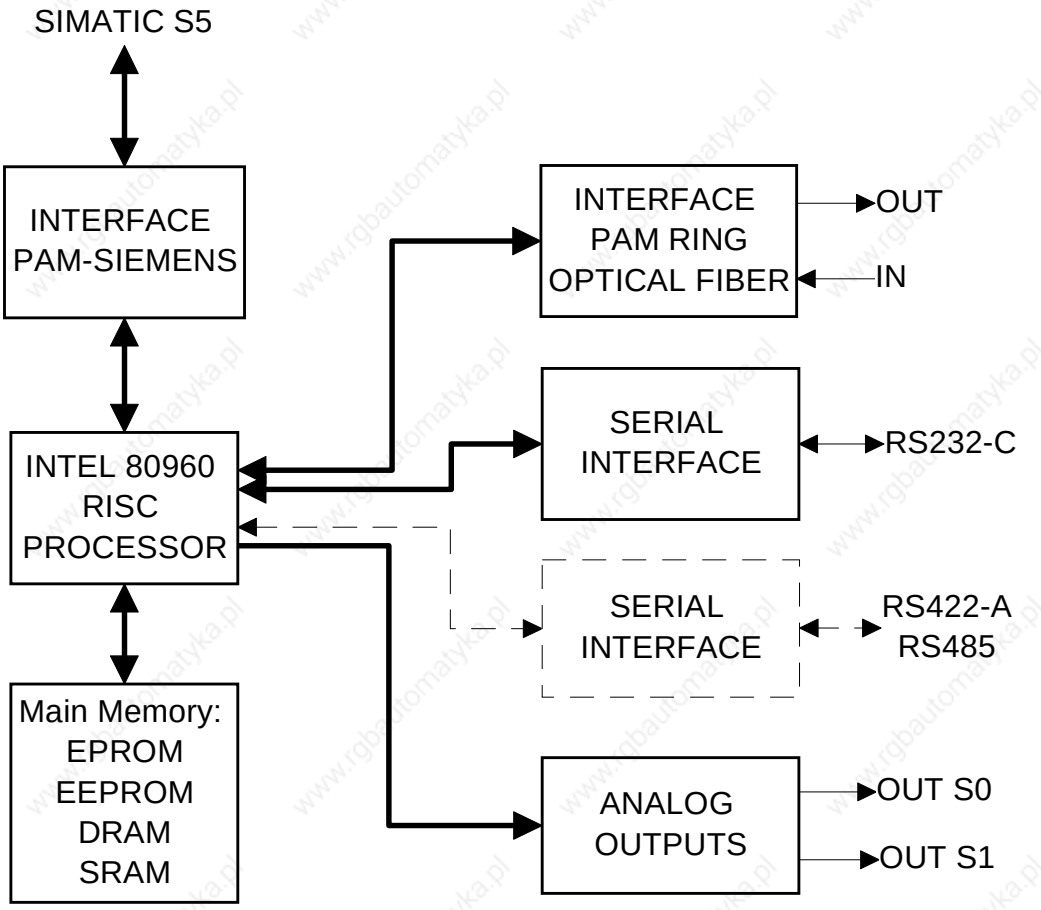


Figure 2:PAM Simatic S5 block diagram

The RS-232-C interface is used to connect PAM with a terminal or a computer for application monitoring and debugging purposes. An optional RS-422-A/RS-485 is available to connect another host (PLC, PC, etc.).

2.3 SIMATIC INTERFACE ARCHITECTURE

Figure 3 illustrates the architecture of the Simatic interface. Pin assignments for the upper and lower interface connectors are listed in Table 1 and Table 2 respectively.

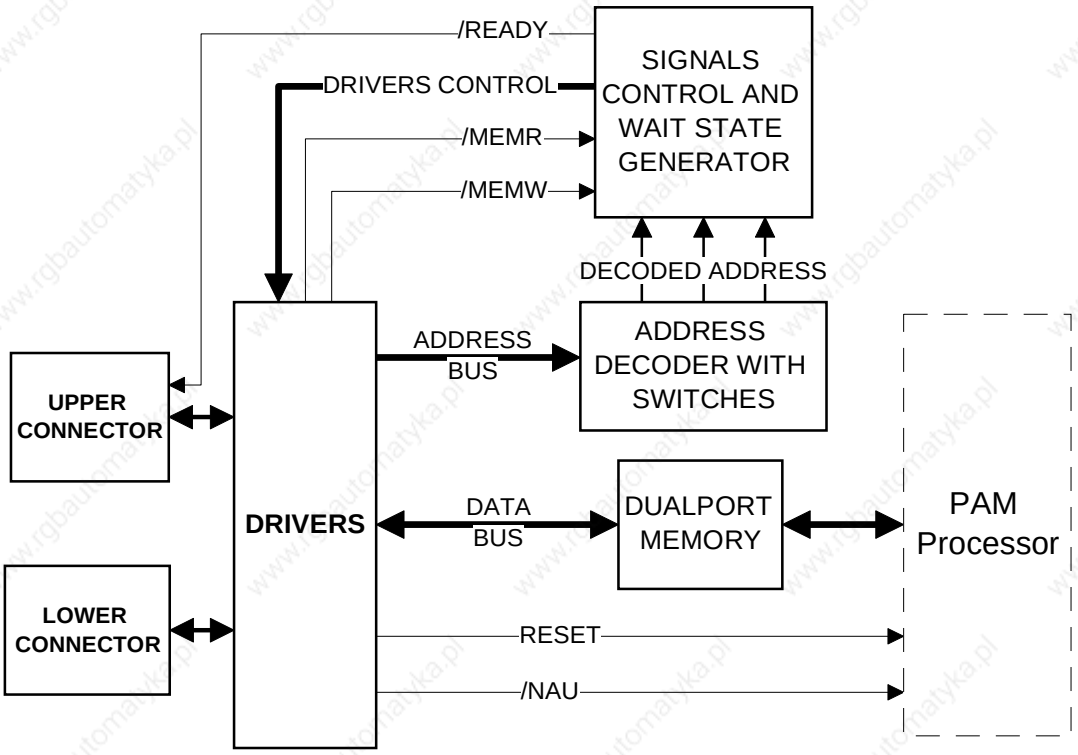


Figure 3: Simatic Interface block diagram

PIN ↓ ROW →	D	B	Z
2	not used	GROUND	+5V
4	not used	not used	not used
6	ADB12	ADB0	RESET
8	ADB13	ADB1	/MEMR
10	ADB14	ADB2	/MEMW
12	ADB15	ADB3	/READY
14	not used	ADB4	DB0
16	not used	ADB5	DB1
18	not used	ADB6	DB2
20	not used	ADB7	DB3
22	not used	ADB8	DB4
24	not used	ADB9	DB5
26	not used	ADB10	DB6
28	not used	ADB11	DB7
30	not used	not used	not used
32	not used	GROUND	not used

Table 1: Upper Connector Signal & Pin Assignments

PIN ↓ ROW →	D	B	Z
2	not used	GROUND	+5V
4	not used	DB8	DB12
6	not used	DB9	DB13
8	not used	DB10	DB14
10	not used	DB11	DB15
12	not used	not used	not used
14	not used	not used	/NAU
16	not used	not used	not used
18	not used	not used	not used
20	not used	not used	not used
22	not used	not used	not used
24	not used	not used	not used
26	not used	not used	not used
28	not used	not used	not used
30	not used	not used	not used
32	not used	GROUND	not used

Table 2: Lower Connector Signal & Pin Assignments

The comment "not used" mean that the SIMATIC S5 signal is not used by the PAM.

The PAM system needs in all cases both the upper and lower connectors for power distribution purposes.

2.4 COMPATIBILITY WITH SIMATIC S5 MODELS AND CPUS

Communication compatibility between the PAM SIMATIC and a number of Simatic S5 models with different CPUs has been verified by test. Siemens specifications for other CPUs indicate compatibility. Refer to Table 3 for a summary of current compatibility information.

PLC MODEL → STATUS ↓	115U/135U	155U
TESTED WITH (CPU)	941,944, 944B	946/947
SIEMENS SPECS. INDICATE COMPATIBILITY WITH (CPU)	942,943,941B,942B,943B	948

Table 3: Siemens S5 Compatibility

SIEMENS documentation, states the new 945 CPU is compatible with older CPUs; however, ACC has neither tested nor verified compatibility with the 945.

3 CONFIGURATIONS

The PAM Simatic S5 may be used with the Simatic S5 model 115U, 135U and 155U PLCs. The 115U and 135U use an 8 bit data bus The 155U uses a 16 bit data bus. Figure 4 shows the location of jumper (S2) and other configuration components.

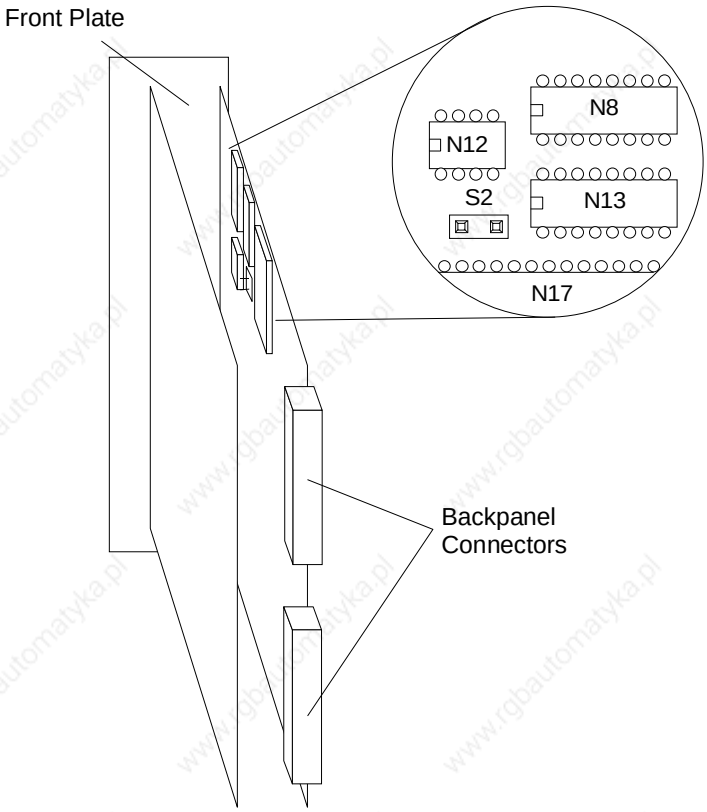


Figure 4: Configuration Jumper and Switches Location

3.1 CONFIGURATION FOR 115U AND 135U

When interfacing to a 115U or a 135U, jumper **S2 must be removed.** In this configuration, SIMATIC uses a 8 bit data bus and always makes two accesses to read or write a 16 bit word (see Figure 5). The signals DB8 to DB15 are not used by the 115U/135U.

The organization of PAM Dual Port Memory (DPM) is 2K * 16. This is the reason for the double connection of the data bus on the PAM side. However, to the SIMATIC S5 115U/135U, the DPM looks like a 4K*8 memory. Switching of the data bus at the PAM side is controlled by the value of the address on the bus.

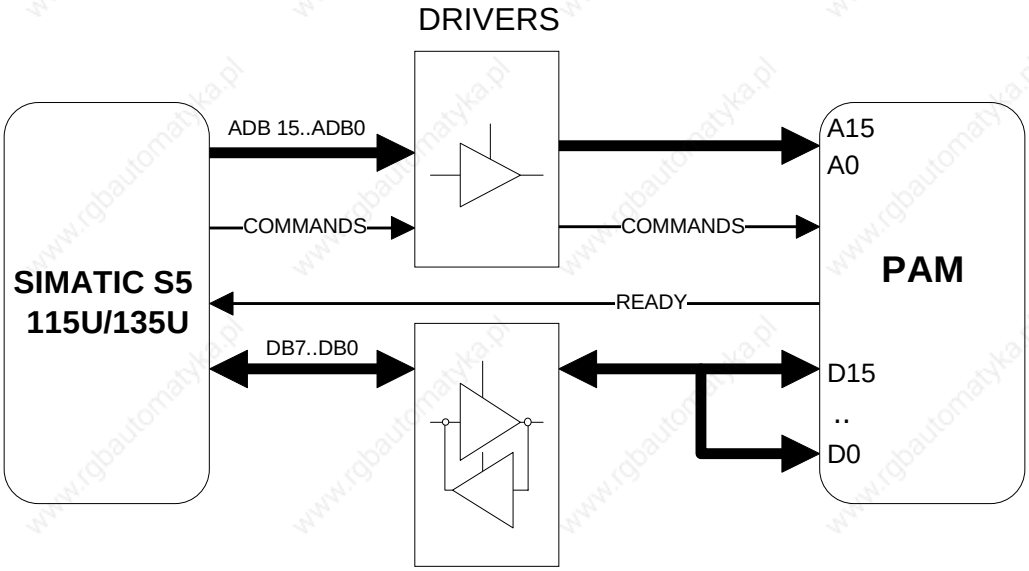


Figure 5: 115U/135U Mode

3.2 CONFIGURATION FOR 155U

When interfacing to a 155U, jumper **S2 must be installed.** In this configuration, SIMATIC uses a 16 bit data bus and accesses 16 bit words (see Figure 6). It sees the PAM DPM as a 2K * 16 bit memory.

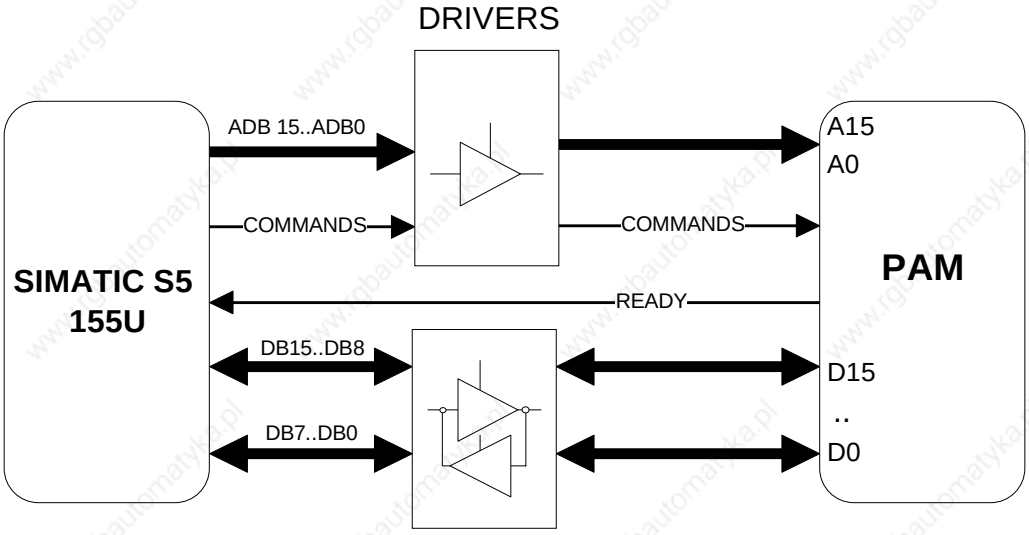


Figure 6: 155U Mode

3.3 PAM DUAL PORT MEMORY ADDRESS CONFIGURATION

The SIMATIC S5 can access up to 64Kbytes of memory (0000h to FFFFh). But, since the total capacity of the DPM is 4K bytes, this address space is divided by PAM into sixteen 4K byte pages of (see Figure 7). PAM DPM is mapped into one of these pages, as determined by the setting of configuration switch N12 (see Figure 4).

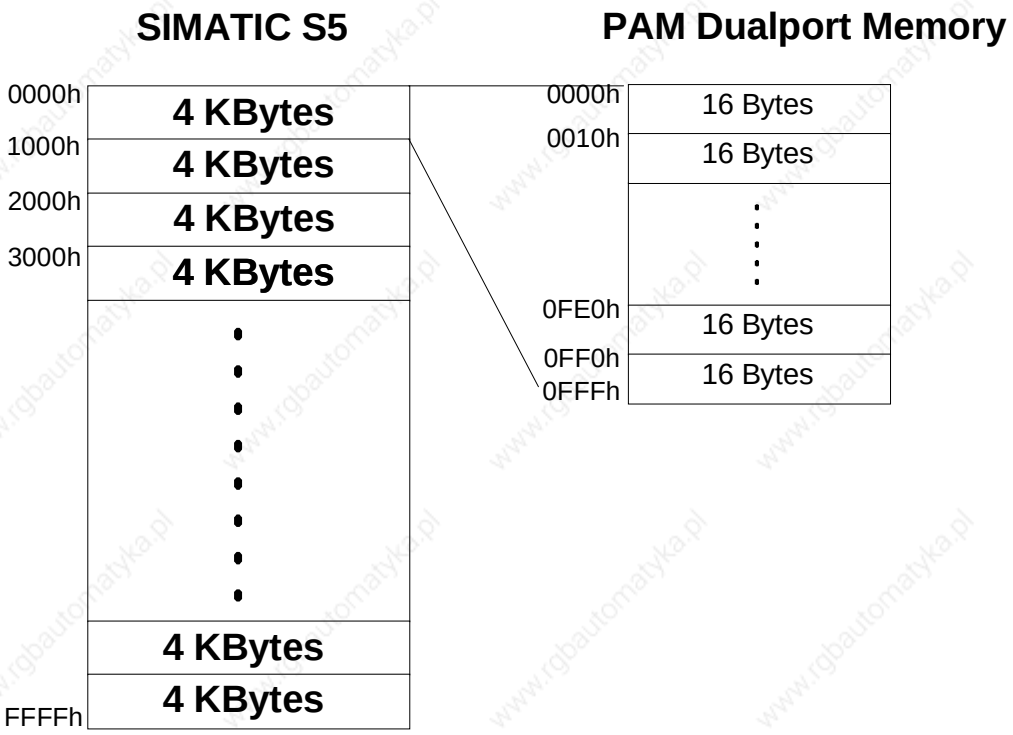


Figure 7: Memory configuration

If the application uses a large complement of Siemens peripheral cards requiring a lot of memory space on the bus, it is possible to reduce the size of the DPM using configuration switches N13 and N8 to define the start and end addresses of the Dual Port Memory in increments of 16 bytes. Switches N8 and N13 are located next to jumper S2 (see Figure 4).

Figure 8 illustrates the factory (default setting) of the address configuration switches which is:

- N12: Page 0 selected (DPM maps into addresses 0000 - 0FFF of Simatic bus address space)
- N13: Starting address of DPM in the selected page is 000
- N8: End address of DPM in the selected page is FFF

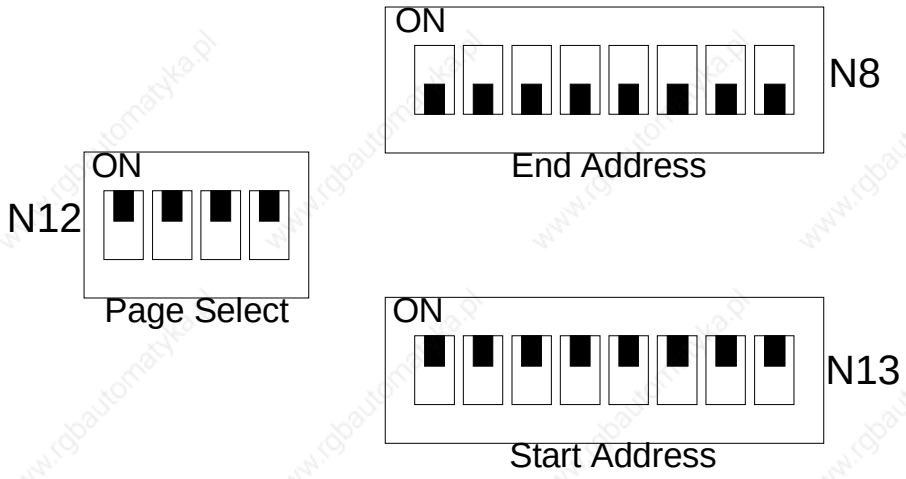


Figure 8: Address Configuration Switches (Factory configuration)

Logical values: **Switch "ON" -> "0"**
Switch "OFF" -> "1"

The factory configuration (as shown in Figure 8) is: selected page: 00h, start address: 00h, end address: FFh.

3.4 CONFIGURATION EXAMPLES

EXAMPLE 1

A PAM must communicate with a SIMATIC S5 115U. There is a free space between physical address 2000h and 3000h on the SIMATIC Bus.

Solution:

Free Space between 2000h and 3000h	=>	Page selection :	2xxxh
No memory restriction	=>	Start address :	x000h
		End address :	xFFFh

Figure 9 illustrates the address switch configuration for example 1.

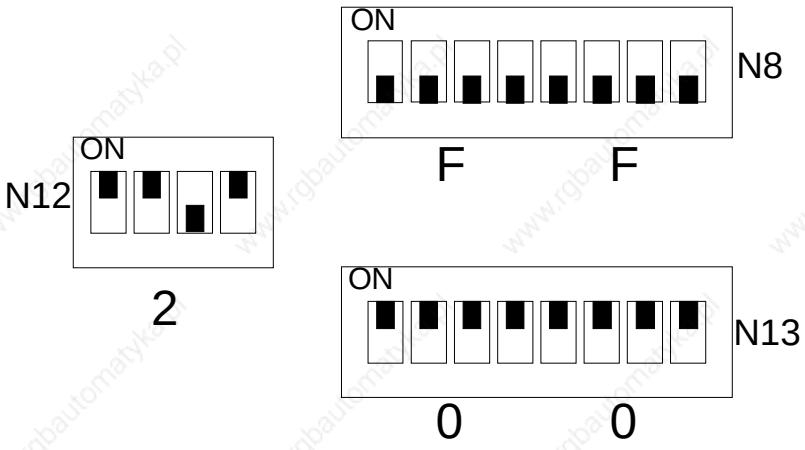


Figure 9: Address Switch Configuration for Example 1

EXAMPLE 2

A PAM must communicate with a SIMATIC S5 135U. With the 135U, the free memory space is restricted (see Simatic S5 Driver for PAM, Technical Manual, p/n 006.8023.B). Typical free memory space is FC00h to FDFFh.

Solution:

Free Space between FC00h and FDFFh	=>	Page selection :	Fxxxh
		Start address :	xC00h
		End address :	xDFFh

Figure 10 illustrates the address switch configuration for example 2.

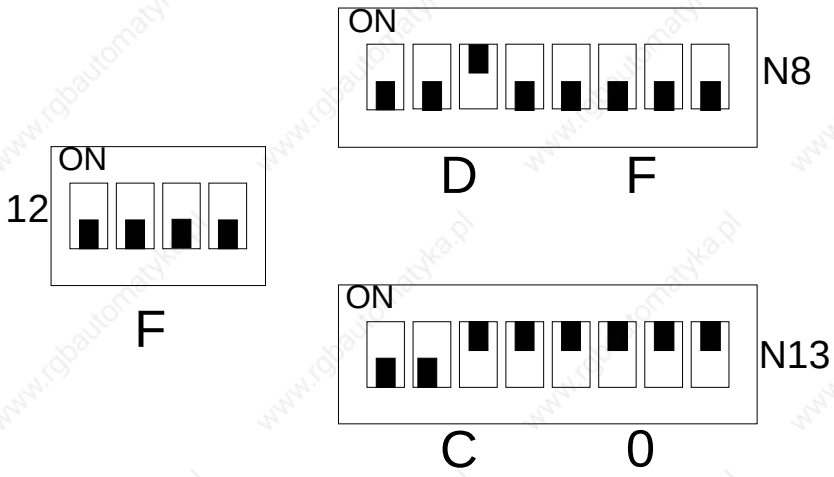
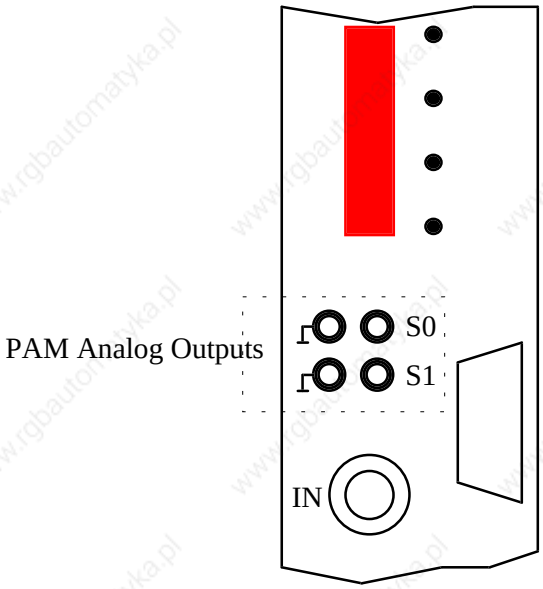


Figure 10: Address Switch Configuration for Example 2

3.5 OTHER SWITCHES

All other switches of the SIMATIC S5 interface board, from S3 to S15, and all switches of the CPU board are configured at the factory and may not be modified.

4 ANALOG OUTPUTS

Two analog outputs are accessible on the PAM Simatic front panel. These analog outputs which may be used by the application for monitoring or debug purposes (see PAM Reference Manual) have 8 bit resolution, 0V to 10V amplitude and are not isolated.