# SIEMENS

# Programmable Controller S5 110S/B

**Operating Instructions** 



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# SINATICS55

# SIMATIC S5–110S/B Programmable Controller

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# SIMATIC S5–110 S/B Programmable Controller

# 6ES5 110



Fig. 1 S5–110S programmable controller. On the left: Central controller. On the right: I/O modules. In the foreground: the 670 programming unit.

#### 1.1 Application

1.2 Construction

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#### **1.1 Application**

The 110S programmable controller (PC) is part of the SIMATIC S5 System.

It is designed for automation tasks in the middle and upper performance ranges. The degree of expansion and the range of functions are matched to the typical requirements in these ranges.

The PC can be easily adapted to the required tasks on account of its expandibility.

Combination with other SIMATIC programmable controllers and hard-wired controllers is possible.

#### **1.2 Construction**

The 110S is available in various basic versions and can be equipped with different power supply units (220 V AC/240 V AC, 115 V AC or 24 V DC). The programmable controller is designed for operation without fans.

The modules are accommodated in a rugged housing, which can be mounted without difficulty in electronic cabinets and which is also suitable for wall mounting. The modules are interconnected via the flow-soldered backplane PCB located in the rear wall of the housing. Connectors with 48 or 64 pins are used in the backplane PCB.

The programmable controller uses the familiar digital input/ output modules of the 110 A PC range. These modules are available in 24 V AC/DC, 48 V AC/DC, 115 V AC and 220 V AC versions and contain either 8 inputs or 8 outputs each. The modules are mounted on a separate mounting rack and controlled directly from the CPU.

In addition, module locations 3, 4, 5 or 6 of the central controller in Fig. 3 can also be used for digital/analog peripheral I/O modules (compact version 20 mm wide), the 302 serial peripheral interface module and the MC210 monitor interface module.

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Fig. 2 Application of the S5-110S programmable controller



Fig. 3  $\,$  S5–110S central controller (equipped with power supply unit and CPU module)

- 1 Power supply (PS) (220 V AC/240 V AC; 115 V AC or 24 V DC)
- 2 CPU 3 Test module
- 4 Memory module 340 (RAM) or 350 (RAM/EPROM)
- 5 PU interface module 511
- 6 Interface module 512C

1.3 Principle of operation



Fig. 4 Block diagram of the S5–110S programmable controller

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# 1.3 Principle of operation

S5 bus:	For exchanging data within the CPU and between the CPU and the various inter- face modules.	Interface module 512C:	Used for connecting up 4 external units: a) SIMATIC S5 programmable controllers b) Terminals
IV bus:	Input/output bus of the microprocessor.		<ul> <li>c) Process computers</li> <li>d) Keyboard printers</li> </ul>
Microbus:	Used for controlling the central processor.	PU interface module	For connecting the 670/675 programming
110 bus:	Input/output bus connecting the I/O pro- cessor and the digital input/output	511:	unit.
*	modules.	PU 670C/675:	The 670/675 is a very powerful video pro- gramming unit. It is used for programming
User EPROM module:	Contains the user program (2K, 4K or 8K statements, EPROM)		and debugging all SIMATIC S5 pro- grammable controllers. The user can pro- gram in ladder diagram, control system
User memory:	Contains the user program (½K state- ments, RAM)		flow-chart or statement list represen- tations.
Blocks:	128 program blocks	Monitoring and logic in the PS:	For monitoring the external and internal voltages.
	63 data blocks (without DB0)	I/O modules 110:	A max. of 128 input and output modules each with 8 inputs or outputs can be
I/O processor:	The I/O processor scans the digital in- puts/outputs and transfers the contents		connected.
	to the central processor and also sets the digital outputs as required by the CPU.	Service unit 333C:	Used for festing the 110S PC. The following functions are possible: Output of data, timer and counter values.
CPU and microprogram:	Decoding and execution of the STEP 5 statements.		Input of data, timer and counter values. Signal state display of inputs, outputs and flags.
Flags:	1K bits retentive, 1K bits non-retentive		(The user program of the PC cannot be modified with the service unit).
Process image:	Signal state of the digital inputs and outputs stored in memory.		The service unit is connected to the PC via digital inputs and outputs.
Timers:	128 integrated timers.		
Counters:	128 integrated counters.		
Monitor:	Monitors faults such as acknowledge- ment delay (time-out) or cycle time ex- ceeded.		
Memory module: 340 or 350 (with battery backup)	Data expansion and extension of user program. RAM module 340; 8 or 16K statements RAM/EPROM module 350; 4K statements	tonast	
	(RAM) and 2 to 12K statements (EPROM)		

**1.3 Principle of operation** 

#### **Function diagram**



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#### **1.4 Technical specification**

#### 1.4 Technical specification

#### 1.4.1 General data of the 110S programmable controller

Input voltage:	a) 220 V/240 V AC b) 115 V AC c) 24 V DC	(+10%, -15%) (+10%, -15%) (+25%, -17%)		
Current input:	a) 0.6 A at 220 V AC b) 1.2 A at 115 V AC c) 3.2 A at 24 V DC			
Ambient temperature:	According to SN 26556 B, the air intake temperature can be 0 to 55 °C (5 °C derating per 1000 m altitude difference); storage temperature: $-40$ to $+70$ °C.			
Humidity rating:	F to DIN 40040 (95 % 25°C).	relative humidity at		
Degree of protection	: IP 20 to DIN 40050.			

Shock test: to SN 29010, class 13.

Frequency	Consta	Constant amplitude of the					
range Hz	displacement	acceleration					
10 to 58	0.15 mm	ways -					
over 58 to 500	an IS	2 g					

Shock test:

15 g/11 ms, trapezoidal to DIN 40046, Section 7.

All parts of the central controller are connected galvanically to each other. In order to achieve effective electromagnetic shielding, all the parts are connected to each other through low resistance paths. I/O modules are galvanically isolated.



Fig. 5 Power supply units a) 220 V AC/240 V AC b) 24 V DC

#### 1.4.2 Power supply unit with housing

Power supply	6ES5 932-3SA12	6ES5 932-3SA22	6ES5 932-3SA32
Input voltage	220 V AC or 240 V AC	115 V AC	24 V DC
Tolerance of the input voltage	+10%, -15%	+ 10 %, - 15 %	+25%, -17%
Permissibe mains frequency range	48 to 63 Hz	48 Hz to 63 Hz	
Current input for rated load	0.6 A	1.2 A	3.2 A
Max. input current	approx. 0.9 A	approx. 1.8 A	3.3 A
Fuse	0.8 A	1.6 A	- 50
Output voltage	+5 V DC ±1%	+5 V DC ±1%	+5 V DC ±1%
Rated current I <sub>AN</sub>	10 A	10 A	10 A
Maximum output power	50 W	50 W	50 W
Overvoltage protection	6 V DC +4 %	6 V DC +4 %	6 V DC +4 %
Current limiting	$1.05 \times I_{AN}$	$1.05 \times I_{AN}$	$1.05 \times I_{AN}$
Galvanic isolation between input and output circuits	yes	yes	no
Back-up battery	Lithium	Lithium	Lithium
Battery voltage	approx. +3.4 V DC/5 Ah	approx. +3.4 DC/5 Ah	approx. +3.4 V DC/5 Ah
Life of back-up battery	6 years	6 years	6 years
Back-up period	1 year at 25 °C	1 year at 25°C	1 year at 25°C
Connection for monitoring the 24 V DC load voltage	yes	yes	no
Weight of the PSU with housing	9.5 kg	9.5 kg	6.7 kg

1.4 Technical specification

	S. S.				)-	
1.4.3 CPU / Memor	ry submodule					
DC voltage supply:	+5 V +1 %					
Current input typ.:	1.6 A			2		
max:	2.6 A		23			
Comment in such a fith a				-		
Current input of the						
with 2K statements	max. 160 mA			line Norma		
with 4K statements	max. 185 mA					
with 8K statements	max. 235 mA 🔊 👋		1			
Current input during	1. two 2.0A					
back-up operation:	max. 128 μA			S		
baon up oporation	S.					
Execution time for a	< 8 μs					
S binary statement:						
Bus driver (110 bus)	designed for driving max	c 64 input/output				
Bus anver (The Bus)	modules	(ormpat) output				
24						
Range of operations	s: 45 binary statements	tatamanta				
	15 block call and jump s					
	27 load and transfer sta	tements				
	16 organizational staten	nents				
	21 digital substitution st	atements				
	17 logical and arithmetic	cstatements				
Adressing range:	max, 512 inputs/outputs	3		19		
, laroosing ranger	1024 retentive flags (0.0	) 127.7)				
	1024 non-retentive flags	3	Fig. 6 CPU			
	(128.0 255.7) 129 integrated timera or	ab with one of				
	4 optional time bases	ach with one of				
	0.01 s					
	0.1 s					
	1 s					
	Time base 0 999					
	128 integrated counters	s from 0 99				
2						
Memory:	1K statements for opera	ating system				
	1 FPROM memory subr	nodule for the				
	user program consisting	g of:	100 B			
	1×2532 up to 2K statem	nents				
	$2 \times 2532$ up to 4K statem	nents				
		lents	1			
Weight:	approx. 1100 g					
4 4 4 E44 (E40 inter	face medule and 740 or 7	E0				
module	race module and 540 of 3	oou memory	(Q)			
modalo			P			
a) PU interface mod	lule 511	S				
DC supply voltag	je:	-5 V	5			
Weight	וכמון: ו ב	.7 A pprox. 300 a		1		
troight.	à	PPION DOD 9				
b) Interface module	512C	No.	a)	b)	c)	
DC supply voltag	je: +	-5 V				
Current input (typ	Dical): 1	.0 A	Fig. 7 (a) 340 mor	mony module b) 511 DI	Linterface mor	tule
weight.	a d	ppion. 000 g	ing. / a) 5-to mer	nory module, by off FC		

a) 340 memory module, b) 511 F c) 512C interface module ace module.

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# 1.4 Technical specification

S		
c) Memory module 340 (RAM)		1.4.6 I/O modules (digital inputs/outputs)
8 or 16K statements		
DC supply voltage:	+5 V	The following I/O modules are available:
Current consumption (typ):	0.8 or 0.9 A	Input modules
Current consumption		Output modules
in backup operation:	max 0.6 or 1 mA	(Dimensions $H \times W \times D$ : 166 mm $\times$ 40 mm $\times$ 150 mm)
And the second s		The input/output modules described on the following pages are
Approx. weight:	500 g	ine input/output modules described on the following pages are
		Identical to those of the TTU A PC.
<ul> <li>d) Memory module 350 (RAM/EPROM)</li> </ul>	100 No.	
4K statements (RAM) and 2K to 12K		The modules are snapped onto a mounting rack. This consists of
statements (EPROM)		a 75 mm high standard sectional rail with either ten or eighteer
DC supply voltage:	+5 V	socket connectors wired up to the 110 bus.
Current consumption:	max, 1,4 A	
(memory submodule 370/371)	0.27 A each)	The socket connectors for the input/output modules are wired
Current concurrention in	0.277(Cdoll)	according to their mounting locations, i.e. a module on the first
	may 0.7 m A	I/O mounting location has the address 0 (see diagram on p. 30)
backup operation:	max. U.5 mA	
Approx. weight:	300 g	The modules are simply snapped onto the module mounting rail
		This simultaneously establishes the electrical connection be
S <sup>0</sup>	10°	tween the module and the appliest approactor
1.4.5 Digital/analog compact periph	neral I/O modules,	tween the module and the socket connector.
302 serial peripheral interface	module and	The maximum I/O configuration consists of 16 racks each with
210 monitor interface module		8 module locations or 8 racks each with 16 module locations
		o module locations of o facks each with to module locations.
a) Digital I/O compact modules (only 2	0 mm wide)	Each input/output module has 8 inputs or 8 outputs
Digital I/O compact modules with	16 to 32 inputs/outputs	Each input/output module has o inputs of o outputs.
(also as mix) can be plugged into lo	cations 3 4 5 or 6 in the	The effective strengthere of the distant in the strengthere is a second strengthere is a second strengthere is
control controller (Fig. 7)		Five different versions of the digital input module are available.
Central controller (Fig. 5).	EV 5	a) 24 V DC
DC supply voltage:	57	<ul> <li>b) 24 V DC with interrupt processing (group signal)</li> </ul>
Current consumption:	approx. 0.2 A	c) 48 V AC/DC
Weight:	approx. 200 g	d) 115 V AC
		e) 220 V AC
b) Analog I/O compact modules		A. A. A.
Analog I/O compact modules wit	h 4 to 16 input/output	Digital output modules are available in five different versions:
channels can be plugged into loca	tions 3 4 5 or 6 in the	a) 24 V DC 2 A
central controller (Fig. 3)		b) 48 V DC 2 A
DC supply voltage:	5 V	c) 24 V AC /48 V AC 2 A
Current concurrention		d) $115 V AC = 2 A$
Current consumption.	approx. 0.5 A	
vveignt:	approx. 200 g	e) 220 V AC 2 A
<u>x</u>		The signals in the input/output modules are galvanically isolat
<li>c) 302 serial peripheral interface modul</li>	e	ed by opto-couplers. The signal states of the inputs or outputs
The 302 interface module can be plu	gged into locations 3, 4,	are indicated on the front of the modules by light-emitting
5 or 6 in the central controller (fig	. 3). However, only one	diodes.
expansion unit (EU182) may be conne	ected to each connector.	
DC supply voltage:		SIMATIC S5-110 input/output modules
Current consumption:	2 A 🔊	1024 inputs (outputs (max.)
Weight:	approx 300 g	roz4 inputs/outputs (max.)
Weight.	approx. 500 g	
a) 210 monitor internace module		
The 210 monitor interface module	from the ESU902 pack-	
aging system can be plugged into	location 3 in the central	
controller (Fig. 3). The image memor	y is a 2K byte RAM.	
DC supply voltage:	+5 V	
Current consumption:	1.2 A	atter ter for the second and the second atter the second sec
Weight:	approx, 200 a	

Fig. 8 I/O modules

1.4 Technical specification

Digital input modules	6ES5 400-7AA13	6ES5 401-7AA13	6ES5 405-7AB11	6ES5 405-7AB21	6ES5 405-7AB31
Number of inputs Galvanic isolation	8 yes	8 (with group signal)	8 yes	8 yes	8 yes
Input voltage $U_N$	24 V DC		115 V AC/DC	220 V AC/DC	48 V AC/DC
Input voltage corresponding to – "0" signal – "1" signal	-35 V to +4.5 V +13 V to +35 V		0 to 40 V AC/DC 85 V AC/DC to 132 V AC/DC	0 to 70 V AC/DC 170 V AC/DC to 264 V AC/DC	0 to 18 V AC/DC 38 V AC/DC to 65 V AC/DC
Input current at "1" signal - connectable proximity switches	8.5 mA DC BEROs	8.5 mA	10 mA AC, 5.7 mA DC AC BEROs	15 mA AC, 2.4 mA DC	13 mA AC, 12 mA DC -
Delay on signal change - ON: "0" → "1" - OFF: "1" → "0"	1.5 ms to 5 ms 1.5 ms to 5 ms		2.3 ms to 13 ms 2.0 ms to 20 ms		
Total load capability at 1.2 $U_{\rm N}$	100% referred to sum all inputs	of currents of	75% referred to sum of cur	rents of all inputs	
Max. permissible length of leads – in common cable (multi-core cables) max.	1000 m at 24 V/48 V A0 100 m at 115 V A0	C/DC C	100 m at 24 V/48 V AC/DC 500 m at 115 V AC/DC	50 m at 24 V/48 V AC/DC 100 m at 115 V AC	800 m at 24 V/48 V AC/DC 400 m at 115 V AC
<ul> <li>with cables run separately max.</li> </ul>	600 m	. Kard	600 m	1 500 m at 220 V AC	1 200 m at 220 V AC
VDE 0160 – for rated value – tested with	Internal 5 V voltage to 36 V DC 500 V AC	external input voltage: l	nputs/outputs of one module 250 V AC/DC 2000 V AC	e with respect to each other	
Weight approx.	0.39 kg		0.4 kg		

The 24 V DC input module with interrupt can be mounted in locations 0, 16, 32 or 48. These input modules supply a group signal to the CPU when the signal state on an input changes from "0" to "1" or vice versa (can be switched on the input module via two externally accessible switches for each group of four inputs).

#### 1.4 Technical specification

Digital output modules, static	6ES5 410-7AA11	6ES5 410	0-7AA21	6ES5 415-7AB11	6ES5 415-7AB21	6ES5 415-7AA31
Number of outputs Galvanic isolation	8 yes	8 yes	2	8 yes	8 yes	8 yes
<b>Supply voltage</b> U <sub>s</sub> – rated value – permissible range	<b>24 V DC</b> 3 V DC to 33 V DC	<b>48 V DC</b> 3 V DC to	53 V DC	<b>115 V AC</b> 88 V AC to 132 V AC	<b>220 V AC</b> 176 V AC to 264 V AC	24 V AC to 48 V AC 20 V AC to 65 V AC
Output current at "1" signal max.	2 A	2 A resistive	0.5 A inductive	2 A	2 A	2 A
Short-circuit protection	Fuse (module 6ES5 410	–7AA21, only c	current limited	up to 24 V and with resisti	ve load)	
Limitation of voltage induced on circuit interruption to	at <i>U</i> <sub>s</sub> = 30 V DC: -17 V	at <i>U</i> <sub>S</sub> = 53   −13 V	V DC:	switch-off at $/ = 0$		
Switching frequency – resistive loads – lamps – inductive loads	100 Hz 11 Hz 2 Hz	11 Hz 11 Hz 0.1 Hz		20 Hz 11 Hz 2 Hz		
Total load capability	100% at 20°C (50% at	55°C) (with re	spect to sum	of the currents of all outpu	its)	
Residual current at "0" signal max.	1 mA	 5 mA		8 mA AC	10 mA AC	5 mA AC
Signal level of outputs – "1" signal	U <sub>s</sub> – 1.8 V					
Insulation voltage rating to VDE 0160 – tested with	Internal 5 V DC voltage 500 V AC	to external inp	out voltage, in	puts and outputs of a moc   2000 V AC	lule with respect to each of	ther   1500 V AC
Weight approx.	0.68 kg			0.68 kg		
Notes	Digital input modules w	ith the same v	oltage can be	driven (see page 9)	Contactors of 3TJ rang cannot be driven	le contraction

Digital output modules with relays	6ES5 417-7AA11	6ES5 417-7AA21
Number of outputs Galvanic isolation	8 yes, for 4 outputs eac	8 h
Supply voltage/ current input (rated)	24 V DC/0.1 A	24 V DC/0.2 A
Continuous current Ith2 max.	1A	5 A
Switching capacity of contacts - resistive load max. min. - inductive load max. min.	30 V AC/DC/0.5 A 80 mV/50 µA ∽ ∽	250 V AC/5 A 30 V DC/2.5 A 250 V AC/1.5 A 30 V DC/0.5 A
Contact life in switching cycles	at 0 to 30 V: 5 · 10⁵ at 80 mV: 10 · 10⁵	to DC11: 2 · 10⁵ to AC12: 1.5 · 10⁵
Switching frequency - resistive load max. - inductive load max.	100 Hz -	10 Hz 2 Hz
Simultaneity factor (with respect to sum of the currents of all outputs)	100% at 40°C 50% at 55°C	N.
Insulation voltage to VDE 0160 – tested with	500 V AC	2000 V AC
Weight approx.	0.7 kg	0.7 kg

NB: Relay modules require an additional internal 24 V DC power supply. (These power supplies are snapped at the end of the I/O mounting rack.)

#### 2.1 General 2.2 Central controller (CC)

#### 2.1 General

The following guidelines should be adhered to when wiring:

- The mains cables must be kept as far away as possible from the remaining cables.
- The M connection from the load power supply to the M<sub>ext</sub> terminal should be made via a short connecting wire (see Fig. 11).
- 24 V lines (input/output modules, power supply) and 220 VAC lines (input/output modules, power supply) should be run separately or bundled separately.
- If the 110S programmable controller is mounted inside a cabinet, the side sections and the door must have a low resistance interconnection. The cabinet must be connected to the PE conductor.
- The housing for the input/output modules should be connected via a low resistance path to M<sub>ext</sub> terminal of the CC housing (conductor cross-section 2.5 mm<sup>2</sup>).

#### Caution

The modules of the 110S programmable controller should not be inserted or removed with the power on.



Fig. 9 110S central controller (with full module complement)

#### 2.2 Central controller (CC)

The central controller can be mounted in cabinets with dimensions specified in inches, cabinets with metric units or on any vertical mounting surface.

The central controller should be mounted above the input/output modules. If the maximum configuration is used, the CC should be mounted between the second and third input/output mount-ing racks in order to keep the bus cable to the I/Os as short as possible and minimize external interference.





#### 2.2 Central controller

#### 2.2.1 Power supply (PS)

The power supply (220 V AC, 115 V AC or 24 V DC) should be connected according to the type of power supply used. The 24 V load voltage monitoring circuit should also be connected. If the 24 V load voltage monitoring is to be switched off, as is always required when using 220 V AC I/Os, two additional terminals next to the load voltage monitoring input have to be shortcircuited. There is never any load voltage monitoring in the 24 V DC power supply. For thermal reasons, the power supply unit is an integral part of the housing and cannot be removed.

The battery can be replaced by unscrewing the cover (1) and removing the battery. The battery should be changed at least once a year.

To prevent the battery from discharging when not in use, it must be correctly inserted (+ pole pointing to the front) when putting the programmable controller into operation.

In the case of the 24 V power supply, the negative potential is always connected to earth  $\bigoplus$ .







Fig. 12 Power supply unit

2.2 Central controller

#### 2.2.2 CPU / memory submodule

One or more front connectors are used for connecting up the 110 bus for the digital I/Os. Each front connector (1) connects a maximum number of 128 input/output modules to the CPU.

The connector designation (2) on the CPU corresponds not only to the numbering of the digital inputs/outputs (see p. 28) but also designates the I/O parameters during programming.

A maximum of 512 inputs/outputs can be accessed by the CPU, using all four front panel connectors.

The memory submodule (3) for the CPU has optional capacities of 2K, 4K or 8K statements.

The CPU is plugged in as follows: The module is pushed onto the guides of the housing as far as possible until the two knurled screws (4) grip. The module is then evenly pushed into the connector, using these screws.

The CPU and memory submodule must not be removed or inserted with the power supply turned on.

Do not touch the components or etched conductors with the hands or fingers! This can cause, destruction of the MOS chips!



#### 2.2.3 Interface module 511 and 512C

The 110S PC has locations for two interface modules. The 511 interface module is used for connecting the 670/675 programming unit. When using the 511 interface module, make sure that jumper 8 is connected and jumper 9 is open. (Changeover from 10 MHz operating frequency to 2 MHz.)

The 512C interface module is used for connecting keyboard printers, process computers, CRT monitors and other programmable controllers of the S5 family. Exact details are given in the description of the 512C interface module (jumper assignments, switch position).

Caution: The connecting lead for the 670 PU and the 511 interface module should not be used for connecting the 512C module.

The 110S can only be used with software version 08 of the 511 interface module and software version 07 of the 670 PU.







Fig.14 511 and 512C interface modules

#### 2.2 Central controller

#### 2.2.4 340 or 350 memory module

There are two different memory modules available:

- the 340 RAM module with 8 or 16K statements
- the 350 RAM/EPROM module with 4K statements (RAM) and 2 to 12K statements (EPROM)

The memory modules are used to extend memory space for data and user programs.

In the case of the 340 RAM module, jumpers 2, 6, 9 and 10 must be inserted. Jumpers 5–12 and 7–11 on address coding socket 51 must also be inserted for 8K and jumpers 6–11 and 7–10 for 16K statements.

If the 350 RAM/EPROM module is used, jumpers 3 and 6 must be inserted. On the RAM address coding socket, jumpers 4–13 and 5–12 must be inserted.

Coding socket 19 (memory submodule 1) and coding socket 26 (memory submodule 2) are used for addressing the EPROM submodules. If memory submodule 1 (3) is used, jumpers 6–11 and 7–10 must be inserted on coding socket 19. Depending on the configuration of memory submodule 2 (4), the following jumpers must be inserted on coding socket 26:

Configuration of memory submodule 1	2K statements	4K statements	8K statements
Jumper assignment on coding socket 26	6–11, 7–10, 8–9	5–12	5–12, 7–10
Max. configuration of memory submodule 2	8K statements	8K statements	4K statements

If the memory submodules are used on the 350 RAM/EPROM module, one EPROM submodule with 8K statements must always be plugged into the CPU of the PC even if it does not contain an user program.

If the user program is in the RAM, it is advisable to transfer it to a floppy disk of the programming unit before switching the PC off, otherwise the user program might be lost should the battery fail.

When installing the two interface modules and the memory modules, a frame (1) must be slipped over the front cover in order to be able to plug the modules in and withdraw them without having to apply force, using the two knurled screws (2).

#### 2.2.5 Digital I/O compact modules

512 digital inputs and 512 digital outputs of the rugged "A" type 110 A peripheral I/Os can be connected to the central controller of the PC (see 2.2.9 peripheral I/O modules). If this number of digital inputs and outputs is insufficient, the digital I/O compact modules can be plugged into locations 3, 4, 5 or 6 in the central controller (Fig. 3) or into the 182 expansion unit (only serial interface possible).

These compact modules can only be addressed from address 64  $(40_H)$  to 127  $(7F_H)$ . This makes it possible to address a further 512 digital inputs and 512 digital outputs. However, as these modules were not originally designed for the 110S PC, the process image exchange must be executed by the user program itself. This means that, at the beginning of organisation block 0B1, the process input image must be renewed and the process output image transferred to the peripherals at the end of 0B1. Only peripheral I/Os may be referenced which are actually connected, otherwise the PC will enter the "Stop" state due to



Fig. 15 Memory module a) 340 (RAM) b) 350 (RAM/EPROM) with memory submodules



an acknowledgement delay (time-out).

Examples of compact modules

0B1		i.
L PB64		
L PB65	Renew process image of the inputs	
T IB65	(insofar as peripheral inputs are conne	ected)
L PB127		
JU FB1	ALC: NO.	
:	User program	
L QB64		
T PB64		
L QB65	Transfer process output image to the	
T PB65	peripheral outputs (insofar as	
:	peripheral outputs are connected)	
L QB127		
т рв127 丿		

#### 2.2 Central controller 2.3 Input and output modules

#### 2.2.6 Analog I/O compact modules

Analog I/O compact modules can only be plugged into the central controller (locations 3, 4, 5 or 6, Fig. 3) or into a 182 expansion unit (only serial interface possible).

Like the digital I/O compact modules, the analog I/O compact modules can only be addressed from address 64 (40<sub>H</sub>) to 127 (7F<sub>H</sub>). See the operating instructions for "Analog I/O modules (compact version)" for notes on jumpering and modification of input range.

#### 2.2.7 302 serial peripheral interface module

The 302 serial peripheral interface module can be plugged into the locations 3, 4, 5 or 6 of the central controller (Fig. 3). This interface makes it possible to address three 182 expansion units or three 110S racks via a 311 interface module. Each 182 expansion unit with a 311 interface module can be further expanded with the 300 and 312 interface modules. It must be ensured that the analog modules are plugged into the 182 expansion unit containing the 311 interface module, whereas digital modules can be plugged into any parallel expansion unit. The 110S racks with the 311 interface module can be extended with further 110S racks.

Addressing on the 302 interface module for digital/analog peripheral I/Os starts at address 64 ( $40_H$ ) and can go as far as address 127 (7F<sub>H</sub>) (see 2.2.5, 2.2.6). For further details, see the operating instructions "Serial interface between central controller and expansion unit".

#### 2.2.8 MC210 monitor interface module

The 210 monitor interface module can be plugged into location 3 in the central controller (Fig. 3). This interface module makes it possible to operate a monochrome monitor with BAS input (BNC socket) via a 75  $\Omega$  coaxial cable. The image format of the monitor can consist of 16 or 32 lines per image and of 32 or 64 characters per line.

The image memory of the monitor interface has a capacity of 2K bytes RAM. The starting address of the image memory must be set to the address 2K ( $0800_H$ ), 4K ( $1000_H$ ) or 6K ( $1800_H$ ) for the 110S PC. The interface module must be assigned parameters in order to be able to be addressed by the CPU. These parameters take up 16 addresses in the peripheral address area and must be situated between peripheral adresses 64 ( $40_H$ ) and 127 ( $7F_H$ ) in the case of the 110S PC.

For further information, see the operating instructions "Monitor interface module for the 210 micro-computer system".

Note: When using the compact modules, the plastic snap-in holders at the back of the rack must be removed.

#### 2.3 Digital input/output modules

The mounting rack for the input/output modules can be attached to mounting plates or any other vertical mounting surface or mounted in cabinets with dimensions in inches or metric units.

Fig. 17 shows the configuration (32 module locations) of the I/O modules for one connector in the CPU. The modules are location-coded. Identical modules must not be plugged into locations with the same address, i.e. if an input module is plugged into the location with the address O, only on output module way be plugged in under the same address (see Fig. 17). The maximum I/O configuration consists of eight extra-long mounting racks or 16 short mounting racks (corresponding in both cases to 128 module locations for the input/output modules).



a) with dimensions in inchesb) with metric dimensions (e.g. 8MF cabinets)

Fig. 16 Installation in cabinets

The length of the mounting rack is determined by the space available. If wide cabinets are used (Fig. 16), two mounting racks each with eight module locations (Fig. 17b) can be replaced by one mounting rack with 16 module locations (Fig. 17a).

In this case, the addressing is not changed and one less cable connector (3) is required. The complete addressing for the maximum configuration is shown in a diagram in the appendix (Page 30).

#### 2.3 Input/output modules



Fig. 17 I/O module configuration for one CPU connector a) With extra-long mounting racks b) With short mounting racks 1 Cable to central controller, 2 Cable between two extra-long mounting racks, 3 Cable between two short mounting racks, 4 Mounting rack, 5 Socket connector, 6 Earth connection (M<sub>ext</sub>)

The I/O modules are mounted as follows:

- Securely mount the sectional rail. Make sure that the terminals (6) on the left hand side are connected up (earth connections).
- 2. Snap the socket connectors onto the rail.
- 3. Snap the input/output modules onto the connectors.

4. Wire up the input/output modules to sensors, contactors etc.

In order not to impede the air circulation and to allow easy access, a centre spacing of at least 300 mm should be observed between the rails.



Fig. 18 Snapping an I/O module onto the mounting rack



# 3. Operation

3.1 Power supply (PS)



Fig. 19 Controls and displays on the power supply module

Control or display element	Function	Control action	Cause	Effect	LED
Green LED (1) "Power supply OK"	indicates that the internal voltage $U_A = 5$ V is present	. Chailomatika	al adationatives	If the internal power supply $U_A \le 4.75$ V or $\ge 5.7$ V, the LED goes out	
Yellow LED (2) "Battery low"	indicates that the back-up voltage is too low	and automatike	Back-up voltage of the Lithium cell ≤ 3 V	If, <b>during operation</b> , a back-up voltage of less than 3 V is detected, the "Battery low" signal is given. This does not affect the back-up RAM area in the CPU if the battery is exchanged during operation	anna anna anna anna anna anna anna ann
Bautonatyka d	www.wiche	m <sup>mandbu</sup>	A chaitemankar	If a <b>back-up voltage</b> of $\leq 3^{N}$ is detected after power-up, the "Battery low" signal also appears. In this case, the back-up battery must be changed and a system reset function and system boot function must be carried out with the programming unit since the complete RAM contents have been erased.	.e
	Art Million	Andre 1	2 www.	A AND AND A	www.
Red LED (3) "24 V low"	indicates the absence of or an excessively low 24 V load voltage	Mark Obstonade	24 V load voltage absent or too low (≤ 17.5 V)	If the load voltage fails below a value of 17.5 V, the output modules are disabled The central processor continues to process the user program.	I. Martinopaulo
	-automativa hi	-saitonatika	2 mailonable	If the voltage again exceeds 17.5 V, the output modules are enabled again.	e e e e e e e e e e e e e e e e e e e

# 3. Operation

# 3.1 Power supply (PS)

Control or display element	Function	Control action	Cause	Effect	LED
Pushbutton "Reset"	Acknowledges fault states in the power supply	The power supply can be switched on again by pressing the acknowledge- ment pushbutton	In the event of overvoltages $(U_{AN} \ge 5.7 \text{ V})$ or short-circuits on the internal power supply PS bus, the power supply switches off automatically. "Power Supply OK" LED is no longer illuminated.	"Power supply OK" LED lights up again	green
	-maska a	Pressing the acknowledge- ment pushbutton resets the "Battery low" signal	During operation or when switching on the power, an excessively low backup voltage (≤3 V) has been detected. The "Battery low" display appears (see explan- ation for yellow LED).	"Battery low" LED is no longer illuminated	green
	and a second	Salle	(B <sup>BBUC</sup>	www.cballe	www.coout
Test socket " <i>U</i> <sub>AN</sub> = 5 V" (5)	• Test socket for output voltage (5 V) of the power supply	Connecting a measuring instrument to the measuring sockets with the polarity designations.	acomatyka.pl	tonasta p	, si
Back-up battery	Back-up of the internal RAM memory of the CPU (timers, counters, retentive flags, user program) and also the 340 or 350 memory module.	The lithium primary battery must be changed at least <b>once a year</b> . This should be carried out with the power supply voltage switched on in order to prevent loss of information from the RAM. The battery is inserted in	, dia	MARCHON CONTRACTION	www.blan
	and the second	the compartment as indicated on the screw-on cap with the minus pole first.	, Star	and bot	ANNAN GOOL
Terminal block	Power supply 220 V AC/ 240 V AC or 115 V AC For connecting the cables for 240 V AC, 220 V AC or 115 V AC, including the PE conductor.	Connection of the mains supply cable is carried out as shown on the terminal block.	doutonation?	obaltomatikapi	
	Connecting up the load voltage monitoring circuit (24 V DC)	The 24 V load voltage to be monitored is connected up as indicated on the terminal block.	2 2 2	1997	Manage 1
	Switching off the load voltage monitoring circuit (24 V DC)	The "Off" jumper should be connected if monitoring is to be switched off when the load power supply is not connected.	chaitonacka.	Witchautomatika.	which all
Terminal block	Power supply 24 V DC Connecting the power supply cables for + 24 V and N.	The mains cable is connected up as indicated on the terminal block.	12 <sup>2</sup> 2	12.A	
matri.	There is no load voltage monitoring	automan	automac	- automach	

- 3. Operation
- 3.2 CPU



Fig. 20 Controls and displays elements on the CPU

Control or display element	Function	Control action	Cause	Effect	LED
OFF/ON" switch (1)	For service functions only	1. Set switch to "OFF"	onaska p	The central processor executes the microprogram cyclically (normal state)	green and orange
	Starting and stopping the central processor (micro- program). In the stop state, the microprogram can be enabled for single step operation. This can only be done in conjunction with a test module plugged into the central controller.	2. Set switch to "ON"	www.obautomaskan	The central processor <b>is</b> <b>stopped immediately</b> . The I/Os are disabled (BASP signal). Since the micro- program stop loop, which switches over the LEDs, is not processed, the green LED remains illuminated.	green and yellow
Single step" button (2)	For service functions only Initiates single micro- instructions Can only be used in	Set "OFF/ON" switch to "ON". Then operate the single step pushbutton.	And and a second second	One microinstruction is executed each time the button is actuated.	www.
	conjunction with the test module in the central controller.	obaltonatika	dbaite matthe	diautomatika	
Red "Stop" LED (3)	Indicates the "Stop" state of the central processor and lights up together with the yellow "Output Inhibit (BASP)" LED.	wan .	Mains failure, acknowledge- ment delay (time-out), cycle time exceeded, "Run/Stop" switch at "Stop", programmed stop, program error, etc.	The programmable controller is in the microprogrammed stop loop (no user program processing). The I/Os are disabled (BASP signal).	red and yellow
Green "Run" LED (4)	Indicates the run state of the central processor (cyclic processing of the microprogram). The following combinations can occur:	and Bar	ware chart	www.chool	-second (C)
	Green + orange LED	Caller and	After completed cold restart routine	User program is executed	green and orange

# 3. Operation

# 3.2 CPU

Control or display element	Function	Control action	Cause	Effect	LED
Green "Run" LED (4)	Green + red + yellow LED (only for a few seconds)	paulomatikan)	The mains voltage has been switched on or the "Run/ Stop" switch has been moved to the "Stop" position and then back to the "Run" position.	Cold restart routine is processed. The following are reset: – system data – block address list – non-retentive flags – process I/O image – memory module system and user memory check	red and green and yellow
	Green + yellow LED	automatikan)	The "OFF/ON" switch has been put to the "ON" position (test state of the central processor). Undefined state of the central processor.	The outputs are disabled (PESP signal)	green and yellow
	and the second literation of the second litera	en and a second	. B	ward Con	ANNAN COS
"Run/Stop" switch (5)	Cold restart and stop of user program execution	1. "Run" switch position (The user program is only executed if the "OFF/ON" switch is in the "OFF" position).	dautonaska d	The user program is pro- cessed. The cold restart routine is started auto- matically on power-up.	green and orange
	annable.d	2. "Stop" switch position	ecmatkapt	The central processor is brought to the micro- programmed stop loop (the user program is not executed). The outputs are disabled (BASP signal).	red and yellow
	Soo water	<b>Caution:</b> When initiating a cold restart, the switch should be put to "Run" then to "Stop" and back to "Run".	.50	and the second	Margar, Bar
	NO.S.	NO.S	. NOR	N.C.S.	
Orange LED (6) "Program running"	Shows the cyclic processing of the user program (lights up together with the green "Run" LED)	Dattornas,	Completed cold restart routine	Cyclic execution of the user program. <b>Cycle time is max. 270 ms.</b>	orange and green
Yellow "Output Inhibit" LED (7)	Indicates the state of the disabled I/Os (BASP)	paulomashan)	Mains failure, acknow- ledgement delay (time-out), cycle time exceeded, "Run/Stop" switch at "Stop" position, programmed stop, program error	The outputs are disabled	, chast
"Reset" button (8)	Resetting of counters, timers and flags.	The reset button is pressed simultaneously with the initiation of the cold restart, i.e. putting the "Run/Stop" switch from "Stop" to "Run"	acomatyka pl	Resetting of all counters, timers, retentive and non- retentive flags during the cold restart routine.	red and green and yellow

Caution: The memory submodule must not be inserted or removed with the power on.

#### 4.1.1 S5-110S fault diagnosis

Start Put control switch from "Stop" to "Run" Green LED on the PS for "Power supply OK" illuminated? No Check mains fuse and connections, check power supply Yes Yes Only yellow "Output inhibit" LED on CPU illuminated? Put the "OFF/ON" switch for the service functions on the CPU to the "ON" position No Red and yellow LEDs on CPU for "Stop" and "Output inhibit" illuminated? Yes Interrupt analysis (see next page) No Yes Green and yellow LEDs on CPU for "Run" and "Output inhibit" illuminated? Switch off mains Replace interface modules 511/512 No Yes All inputs always zero or all outputs not set? Check user program Check peripheral cables and load voltage No Yes Check user program Check peripheral cables and I/Os Input always zero or output not set? No Yellow "Battery low" LED on power supply illuminated? No Yes Replace battery Fig. 21 Sequence diagram for fault diagnosis

In the case of a fault, the S5-110S programmable controller should be checked in the following sequence.

4.1.2 Interrupt analysis



Fig. 22 Sequence diagram for interrupt analysis

23

#### 4.1.3 Interrupt stack

#### 4.1.3 Interrupt stack

The interrupt stack (ISTACK) is a stack register in which the system program stores information when the PC enters the stop state.

- 1. In the case of "Output ISTACK" with the 670/675 programming unit, the control bits (Fig. 23a) which are contained in the system data words SD 5 to SD 7 (absolute address EAOA<sub>H</sub> to EAOE<sub>H</sub>) are output in the first part. The control bits have the following significance:
  - a) PBS SCH: shift block before PROM
  - b) BST SCH: shift block
  - c) SCHTAE: shift operation
  - d) ADR BAU: address list construction
  - e) SPABBR: memory shift discontinuation
  - f) NAU AS: mains failure for interface modules
  - g) QUITT: acknowledgement for PBS SCH
  - h) STOZUS: the PC is in the microprogrammed stop loop (external request/cold restart)
  - i) STOANZ: the PC is in the microprogrammed STOP state (internal request/cold restart)
  - j) NEUSTA: the PC is in the cold restart (new start) routine
  - k) BATPUF: back-up battery for internal RAM memory is ok
  - I) BARB: the PC is in the single step mode

ONTRLBITS

С

- m) BARB END: the PC indicates the end of the single step mode
- n) MAFEHL: group alarm for machine error word SD 7
- e) EOVH: interrupt input byte Ø present
- p) ASPNPR: only EPROM user memory present
- q) ASPNRA: only RAM user memory present
- r) KOPFNI: block header cannot be interpreted (erase, boot and cold restart)
- s) PROEND: shift before EPROM use ended (cold restart)
- t) PADRFE: addressing error in EPROM memory (reset, boot and cold restart)
- u) ASPLUE: address gap in user memory (erase, boot and cold restart)
- RAMADFE: addressing error in RAM memory (erase, boot and cold restart)
- w) KEINAS: no user memory module inserted
- x) SYNFEH: synchronization error (erase, boot and cold restart)
- y) NINEU: cold restart not possible (erase, boot and cold restart)

ata word

z1)SUMF: sum error in system program (cold restart) z2)URLAD: boot (reset and boot)

NB	PBSSCH	BSTSCH	SCHTAE	ADRBAU	SPABBR	NAUAS	QUITT	System d
NB	NB	NB	NB	NB	NB	NB	NB	ΕΑ ∅ Α <sub>Η</sub>
		automato					120	
STOZUS	STOANZ	NEUSTA	NB	BATPUF	NB	BARB	BARBEND	1.80°
	x			x			1	SD 6 EA Ø C <sub>H</sub>
NB	NB	MAFEHL	<b>EOVH</b>	NB	NB	NB	NB	J
			x				1815 T	1000
ASPNPR	ASPNRA	KOPFNI	PROEND	NB	PADRFE	ASPLUE	RAMADFE	ed char
								SD 7 EA Ø E <sub>H</sub>
KEINAS	SYNFEH	NINEU	NB	NB	NB	SUMF	URLAD	J

Fig. 23a Interrupt stack, part 1 (control bits) NB signifies unassigned

2. The interrupt stack proper is output in the second part of the ISTACK (Fig. 23b)

The "Cause of interrupt" is displayed in the interrupt condition code word (SD 214 absolute address  $\text{EBAC}_{\text{H}}$ ) – one of the most important debugging aids. The mnemonics have the following significance:

- a) STOPS: "Run/Stop" switch is in stop position
- b) STUEB: block stack overflow

- c) NAU: mains voltage failure
- d) QVZ: acknowledgement delay (time-out)
- e) ZYK: cycle time exceeded
- f) BAU: battery failure
- g) NNN: programming error; statement is not permissible in the 110S or block number is not permitted or data block not present
- h) STS: programmable STOP

#### 4.1.3 Interrupt stack 4.1.4 System parameters

- 3. The "Result bits" (absolute address EBAA<sub>H</sub>) show the state the PC was in when the interrupt occurred.
  - a) FLG1 (CC1); FLG0 (CC0): condition code for arithmetic, logical and shift operations
  - b) OVFL: condition code for arithmetic overflow
  - c) OR: condition code for OR memory
  - d) RLO: condition code for result of logic operation
  - e) FOP: condition code first scan

The "Brackets" line (SD 209 - SD 212) indicates which bracket level the PC was in when the interrupt occurred. The condition codes for OR, RLO and AND/OR are displayed.

The contents of the accumulator (SD 203 and SD 204), the step address counter SAC (SD 206), the block stack pointer BK-STP (SD 207) and the initial address of the data block selected DB-ADD (SD 208) at the time the interrupt occurred are also displayed.

INTE	RRUPT	5 Т А	СК		201-2.C		
DEPTH:	01					J.S	
						And and a second	
INS-REG:	0000	SAC:	0638 SD 206 EB 9 CH	DB-ADD:	0000 SD 2 EBA	208 Øн	
BLK-STP:	EB03 SD 207 EB 9 EH	-NO.:		DB-NO.:			
		REL-SAC:					
		8				.80	
						Janah	
ACCU1: E	F 3 F SD 203	ACCU2: FD	3F SD 204 EB 98.				
	S.		1 alera				
							SD 209-SD 212 EBA 2 <sub>H</sub> EBA 8 <sub>H</sub>
					_	Ś	
RESULT B	ITS:	FLG1 FLG0	OVFL CARR	Y OR ST	ATUS RLO F	.OP	SD 213 EBAA <sub>H</sub>
		×				x	
							No.x
CAUSE OF	INTERR.:	STOPS STU	EB NAU QVZ	ZYK BAU	NNN STS		Interrupt word
		x 🔊				J.S	EBAC <sub>H</sub>
	den.	and and the second seco		and the second			

Fig. 23b Interrupt stack, part 2

#### 4.1.4 System parameters

The system parameters provide information about the PC and the memory configuration.

- 1. Release of the PC software
- 2. CPU identifier
- 3. Release of the PU and IM software
- 4. Memory configuration (absolute addresses)
  - a) Input modules (I/O memory F000<sub>H</sub> to F07F<sub>H</sub>) b) Output modules (I/O memory F080<sub>H</sub> to F0FF<sub>H</sub>)
- c) Process image of the inputs  $\mathsf{EF00}_\mathsf{H}$  to  $\mathsf{EF7F}_\mathsf{H}$
- d) Process image of the outputs  $\text{EF80}_{\text{H}}$  to  $\text{EFFF}_{\text{H}}$
- e) Retentive flags EE00<sub>H</sub> to EE7F<sub>H</sub>
- Non-retentive flags EE80<sub>H</sub> to EEFF<sub>H</sub> f) Timers ED00<sub>H</sub> to EDFF<sub>H</sub>
- g) Counters EC00<sub>H</sub> to ECFF<sub>H</sub>
- h) ST memory area (system data area)  $EA00_H$  to  $EBFF_H$

#### 4.2 Connector pin assignments in the central controller backplane

$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	Signal	ALCON STREET	h.	Connector with pin assignment				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	name	Power supply X 11	Indicating unit X 12	CPU-X 1	Diagnostics-X 3	RAM-X 5	IM 511-X 7	IM 512-X 9
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	+5 V	1/2		Z2	Z2	Z2	Z2	Z2
SAZL         Image: constraint of the sector of the se	F/A	5/4	2		d2	b2	b2	bZ
PCTL PESP UNATT         Z4         Z4 <thz4< th="">         Z12         Z12</thz4<>	SAZLL		Nº C	f2	f2		A.	2
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		8	<u>,                                    </u>	74	74	74	74	741)
UBATT SA2.H         b5         d4	PESP	10°		b4	b4	24 b4	24b4	b4
SAZH         Image: solution of the solutis oliticate solutis of the solution of the solution	UBATT	1000	b5	d4	10 <sup>2</sup>	d4	d4	d4
CPRL ADB/3 ADB12         12         26         27         26         26         26           SA7R.1         28 <td>SAZLH</td> <td>10</td> <td></td> <td>5 f4</td> <td> f4</td> <td></td> <td>1. St.</td> <td>70.</td>	SAZLH	10		5 f4	f4		1. St.	70.
ADB/3 ADB 1 SAZIL         b6         b6         b6         b6         b6         b6           IMB ADB 1 ADB	CPKL	and	a2 —	Z6	Z6	Z6	Z6	Z6
Ability SATRU         dis         dis <thdis< th=""> <t< td=""><td>ADBØ</td><td>20</td><td>24</td><td>b6</td><td>b6</td><td>b6</td><td>b6</td><td>b6</td></t<></thdis<>	ADBØ	20	24	b6	b6	b6	b6	b6
DEM         Image: Constraint of the constener of the constraint of the constener of the constraint of the	ADB12 SAZRI			d6	d6 f6	d6	d6	d6
EMR ADD 1 ADD 1 ADD 1 ADD 1 ADD 1 ADD 2 ADD 1 ADD 2 ADD 1 ADD 2 ADD 1 ADD 2 ADD	0, 12, 12		<u>Š</u>			- S		<u>ġ</u>
Abbits SAZEH         Basel (B	EMR		Nº.	Z8	Z8	Z8	Z8	Z8
SAZPH         III         IIII         IIIII         IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	ADB1 ADB13	8	S., ,	8d	8d		8d	8d
BMV AD2:4 AD2:4 AD2:4 AD2:4 AD2:4 AD2:5         Z10 L0 L0 L0 L0 L0 L0 L0 L0 L0 L0 L0 L0 L0	SAZRH	10		f8	f8		30	
Ano: ADB14         All Lio         Lio         Lio <thlio< th="">         &lt;</thlio<>				710	710	710	710	710
ADB14 SAZI         10         -10         -10         -10         -10         -10           RDY ADB5 SAZI         212         212         212         212         212         212         212         212         212         114         114	ADB2	. A. C.		b10	b10	b10	b10	b10
SALL         110         110         110         212         214 <td>ADB14</td> <td>She was</td> <td>35</td> <td>d10</td> <td>d10</td> <td>d10</td> <td>d 10</td> <td>d 10</td>	ADB14	She was	35	d10	d10	d10	d 10	d 10
ROY ADB3 ADB15 SAZB         Z12 L2 L2 L2 L2 L2 L2 L2 L2 L2 L2 L2 L2 L2	SAZL	1	24	f10	f10		L	14
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	RDY			Z12	Z12	Z12	Z12	Z12
August 10       d12       d14	ADB3		200	b12	b12	b12	b12	b12
DBC         IA         IA <thia< th="">         IA         IA         IA&lt;</thia<>	ADB15 SAZS		St.	d12	d12 f12	d12	d12	d12
DBØ ADB4 TXR1 INC         Z14 b14 b14 b14 b14 b14 b14 b14 b14 b14 b	0,00	5	0			1997		
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	DBØ	32		Z14	Z14	Z14	Z14	Z14
INC         III         IIII         IIII         IIII         IIII         IIII         IIII         IIII         IIIII         IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII	ADB4 TXR1	1000		d14	614	614 d14	614	614
DB1 ADB5 S:Test 0 DEC         Z16 bit         Z18 bit         Z10 bit         Z20 bit         Z20 bit         Z20 bit         Z20 bit         Z20 bit         Z20 bit         Z22 bit         Z22 bit         Z22 bit         Z22 bit         Z22 bit         Z22 bit         Z22 bit         Z22 bit         Z24 bit         Z24 bit         Z24 bit         Z24 bit         Z24 bit         Z24 bit </td <td>INC</td> <td></td> <td></td> <td>f14</td> <td> f14</td> <td></td> <td>1. South</td> <td></td>	INC			f14	f14		1. South	
DB1 ADB5 STest0         L10 b16 d16 d16 d16 d16 d16 d16 d16 d16 d16 d	DP1	198 - C	34	710	710	710	710	710
STeat 0 DEC         dife	ADB5	1	de.	b16	b16	216 b16		216
DEC         116         166         718         719         720         720         720         720         720         720         721         721         721         721 <td>S-Test 0</td> <td></td> <td></td> <td>d16</td> <td>d16</td> <td>d16</td> <td>d16</td> <td>d16</td>	S-Test 0			d16	d16	d16	d16	d16
DB2 ADB6 S:Test 1 INR         Z18 b18 b18 b18 b18 b18 b18 b18 b18 b18 b	DEC		28	f16	f16	2		S
ADB6         b18         b18 <td>DB2</td> <td></td> <td>d'</td> <td>Z18 ——</td> <td>Z18</td> <td>Z18</td> <td>Z18</td> <td>Z18</td>	DB2		d'	Z18 ——	Z18	Z18	Z18	Z18
S-lest 1 INR         d18         d18         d18         d18         d18         d18         d18           DB3 ADB7 RXR2 IMW         220         222         224 <td>ADB6</td> <td>8</td> <td>0</td> <td>b18</td> <td>b18</td> <td>b18</td> <td>b18</td> <td> b18</td>	ADB6	8	0	b18	b18	b18	b18	b18
IMA         I.0         I.0         I.0         I.0         III           DB3         ADB7 RXR2         Z20         Z20         Z20         Z20         E20         E22         E24	S-lest 1	3.0		d18	d18 f18	d18	d 18	d18
DB3 ADB7 RXR2 IMW         Z20 ADB7 RXR2 IMW         Z20 BASE         Z20 B20 B20 B20 B20 B20 B20 B20 B20 B20 B		200					200	
ADB/ EXERC       b20       b22       b24       b24       b24       b24       b24       b24       b24       b24       b24       b26	DB3			Z20 ——	Z20	Z20	Z20	Z20
IMW         Imm         Imm <thimm< th=""> <thimm< th=""> <thimm< th=""></thimm<></thimm<></thimm<>	ADB7 RXR2	55	55	d20	620	620	620	b20
DB4 ADB8 S-Test BASFI         Z22 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	IMW			f20	f20		ditto	d Lo
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $		1	2	700				
STest BASPI         d22 (22)         d23 (22)	ADB8		2.2.5	b22	b22	b22	b22	b22
BASPI         f22         f22         f22         Z24         Z26         Z28         Z28         Z28         Z28         Z28         Z28         Z28         Z28         Z28         Z28 </td <td>S-Test</td> <td></td> <td>ST.</td> <td>d22 ——</td> <td>d22</td> <td>d22</td> <td>d22</td> <td> d22</td>	S-Test		ST.	d22 ——	d22	d22	d22	d22
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	BASPI	8	0	f22	f22	S°	S	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	DB5	.30		Z24 —	Z24	Z24	Z24	Z24
DAST ANZØ         d24         d26         d28         d	ADB9	. A <sup>20</sup>		b24		b24	b24	b24 🔊
DB6 ADB100 OVF ANZ1         Z26         D26         b26         b28         b30         b30	ANZØ	24.50	1	f24	d24		A.S.	S. A.
DB6       Z26       Z26       Z26       Z26       Z26       Z26       Z26       Z26       Z26       D26       b26       b28       b30       b		- 19.	14 B.	· _ ·			1 <sup>2</sup>	
OVF       ANZ1       020				Z26	Z26	Z26	Z26	Z26
ANZ1       f26       f26       f28         DB7       ADB11       b2       b28       b30       b30       b30       b30       b30       b30       b30       b30       b30       b30 <td< td=""><td>OVF</td><td></td><td></td><td>d26</td><td>d26</td><td>U20</td><td> D20</td><td>D20</td></td<>	OVF			d26	d26	U20	D20	D20
DB7 ADB11 DSI QVZM         Z28 b2         Z28 b28 b28 f28         Z28 b28 b28 f28         Z28 b28 b28 f28         Z28 b28 b28 d28 d28         Z28 b28 d28 d28         Z28 b28 d28 d28         Z28 b28 d28         Z28 b28 d30         Z28 d30         Z28 d32         Z28 d32 <td>ANZ1</td> <td></td> <td>10.8</td> <td>f26 ———</td> <td>f26</td> <td>13.8</td> <td></td> <td>\$2°</td>	ANZ1		10.8	f26 ———	f26	13.8		\$2°
ADB11 DSI QVZM     b2     b28     b28     b28     b28     b28     b28       MWPH BASP MEMSEL QVZVM     b2     f28     f28     f28     d28     d28     d28       CSPAEV M BASPA QVZHM     3/4     Z30     Z30     b30     b30     b30     b30       CSPAEV M BASPA QVZHM     3/4     Z32     Z32     Z32     b32     b32     b32		1	S.	728	728	728	728	728
DSI QVZM         b2         d28 f28         d28         d28         d28           MWPH BASP MEMSEL QVZVM         Z30         Z30         B30         B32	ADB11	25	1	b28	b28	b28	b28	b28
UVZ.MI         128         128           MWPH BASP MEMSEL QVZVM         230         230         b30         b30         b30           QVZVM         3/4         232         232         b30         b30         b30         b30           CSPAEV M         3/4         232         232         b32         b32         b32         b32         b32           QVZHM         3/4         32         d32         d32         d32         d32         d32         d32	DSI	, Mor	b2	d28	100	d28	d28	d28
MWPH BASP MEMSEL QVZVM         Z30         Z30         b30         b30         b30         b30         b30         b30         b30         d30         d32         d32         d32	QVZM	2°°		t28	f28		N°	&
BASP MEMSEL QVZVM         b30         b30         b30         b30           QVZVM         d30         d32         d32         d32         d32         d32	MWPH	AN.	3	Z30	Z30	-	AN.	A.C.
MEMODEL QVZVM         d30         d30         d30         d30           CSPAEV M BASPA QVZHM         3/4         Z32         Z32         b32         b32         b32         b32         b32         b32         d32	BASP	All .		b30	b30	b30	b30	b30
CSPAEV         Z32         Z32         L32         L32 <thl32< th=""> <thl32< t<="" td=""><td>QVZVM</td><td></td><td></td><td>d30</td><td> f30</td><td>d30</td><td>d30</td><td>d30</td></thl32<></thl32<>	QVZVM			d30	f30	d30	d30	d30
CSPAEV         Z32         Z32         B32         B32<			~		+			
WI         D32         D33         D33 <thd33< th=""> <thd33< th=""> <thd33< th=""></thd33<></thd33<></thd33<>	CSPAEV	7/4	3.02	Z32	Z32	L 70	6.70	670
QVZHM   f32 - f32   dd2   dd2	BASPA	5/4	a3	bə∠ d32		d32	bs2 d32	b32
	QVZHM	2.		f32 ——	f32	S.		

Fig. 24a Upper connector row of the CC backplane

1) X9/Z4 connected to the lower connector row X10/Z32

## 4.2 Connector pin assignments in the central controller backplane

Signal name	Power supply-X 11	Indicating unit-X 12	CPU-X 2	nector with pin assignr	nent RAM-X 6	IM 511-X 8	IM 512-X 10
+5 V	<u>1/2</u>		Z2	Z2	Z2	Z2	Z2
NABA	3/4	4	Z24	D2 Z24 b32	b2	Z24	Z24
HOLD		~	d32			d32	d32
BUBE BUSEN 1ØMHZ	de la companya de la comp	8.		b4 — Z16 — Z32 —	e e e e e e e e e e e e e e e e e e e	Z28 d22 Z32	Z28 d22 Z321)
CPUK1 CPUKØ	10 The		d6 Z30			d6 Z30	d6 Z30
DB12 DB8 DB13 DB9 DB14 DB15 DB15 DB11	and the second second	and house		a muldbac	Z4 Z6 b6 Z8 b8 b10	Z4 Z6 b6 Z8 D8 Z10 b10	Z4 56 56 28 58 210 510 510
PLPG HOLDA HOLDA1 HOLDA2	and the second s	10.	Z20 d20 Z18	d20	Ka j	Z16 d20 Z20	d20
	100		d28	420		d28	220
NAU	10000	b1	Z14	b30		1000 C	1075
BAU	2 CO	a1	Z16	0		192 192	24
ul⊘ DBA8 EAZL	L.	A.C.	dz f2 Z4 d4	dz f2 Z4 d4			rd and
μl1 DBA9 DBA13 μl2	2	lq.	f4 Z6 b6 f6	f4 Z6 b6 f6	42.Q	342.01	
DBA1Ø DBA14 μΑØ μι3	~altonio		Z8 b8 d8 f8	Z8 b8 d8 f8		- altorno	-allo
DBA11 DBA15 μA1 μl4	and and the	survey. O	Z10 ——— b10 ——— d10 ——— f10 ———	Z10 b10 d10 f10	and the second	S	ANN N. OT
DBA12 μΑ5 μΑ2 μΙ5		2	Z12 b12 d12 f12	Z12 b12 d12 f12	à	2	
μΑ6 μΑ3 μΙ6 μΑ7	maste		b14 d14 f14 b16	b14 d14 f14 b16	Ye.	- STRANKS	. 6
μΑ4 μΙ7 μΑ8 ΕΑΖS		1.5°	d16 f16 b18 d18	d16 f16 b18 d18		Source and the second s	ALCORD.
μl8 μA9 μl9 EAPSF	14 · · · ·	ANCO -	f18 b20 f20 Z22	f18 b20 f20 Z22	P. Marken		4200
μΑ1Ø ΕΑΙΝΤ μ1Ø μΑ11	all a second	9	b22 d22 f22 b24	b22 d22 f22 b24	4a.9	8.848.9	
VKE µl11 EATAE OR	10 <sup>110</sup>	2	d24 f24 Z26 b26	d24 f24 Z26 b26		Sallon	abalito
ERAB μ12 EACSF μA12	and and is	www.co	d26 f26 Z28 b28	d26 f26 Z28 b28	And Mark	0	And M.
μ13 EICLEAR μ14 EAPRES	?	9	f28 d30 f30 Z32	f28 d30 f30 Z18	12.21	in the second	
ul15 SPKØ	Card.		f32 —	f32 Z30	AD	d26	d26
+5 V M	1/2 ——— 3/4 ———		36 <sup>1</sup>	and the second s	AEAC	V T	K G G
SPK1	ANI OF	. www.iOr		d6		b26 R	b26
+5 V M	1/2			2.	ABZ	S P	F D
SPK2		9	NO.S	Z14	<b>X</b>	Z14 M	Z14 B
+5 V M	1/2 3/4		-5 <sup>-5</sup> <sup>231</sup>		Y W	N PL	

Fig. 24b Lower connector row of the CC backplane

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#### 4.3 Connector pin assignments of the 110 bus

#### 4.3 Connector pin assignments of the 110 bus

Fig. 25 shows the pin assignments of the connectors for the 110 bus for each mounting rack. If the I/O bit is "0", only the inputs are addressed, whereas if it is "1", only the outputs are addressed. The addressing of each module on the mounting rack is carried out using bits Z1, Z2 and F0 to F7 (see Fig. 26). The individual inputs/outputs on the modules are selected by bits K0 to K2.

I/O	Enable the input $(= "0")$ or output modules (	= "1")
Z1, Z2 a	nd	

101017	Addressing of the input/output modules
K0 to K2	Addressing of the inputs or outputs on the selected
	modules
D <sub>IN</sub>	DATA IN, signal state of inputs
Dout	DATA OUT, signal state for setting the outputs
RI	Initialising pulse (resets output modules)
IR	Interrupt group signal of the corresponding digital
	input module
М	0 V DC

#### **Socket connectors**

	-4-"			- 12 m
2	+5 V		E/A	1
4	Z2	X	Z1	3
6	F6	onan	F7	5
8	JR	and a	RI	7
10	F4		F5	9
12	D <sub>OUT</sub>		D <sub>IN</sub>	11
14	F2	No	F3	13
16	К1	tothan	K2	15
18	FO	32	F1	17
20	M–		К0	19

Fig. 25 Pin assignments of the socket connector on the 110 bus



Fig. 26a Coding of the 110 bus with short mounting racks



Fig. 26b Coding of the 110 bus with extra-long mounting racks

# 5. Spare parts

Description	Order No.	Weight approx.
	-5 <sup>47</sup>	ry
Housing, complete with power supply 220 V AC/240 V AC/5 V DC	6ES5 932-3SA12	9.5
Housing, complete with power supply 115 V AC/5 V DC	6ES5 932-3SA22	9.5
Housing, complete with power supply 24 V DC/5 V DC	6ES5 932-3SA32	6.7
CPU	6ES5 902-3SA12	1.0
Memory submodul for CPU a) with EPROM for 2K statements b) with EPROM for 4K statements c) with EPROM for 8K statements	6ES5 911-0AA31 6ES5 911-0AA42 6ES5 911-0AA52	0.06
<b>340 Memory module*</b> RAM for 8K statements RAM for 16K statements	6ES5 340-5AA11 6ES5 340-5AA21	0.3 0.3
<b>350 Memory module*</b> RAM for 4K statements	6ES5 350-5AA21	0.3
Associated EPROM submodules* 371 for 2K statements 371 for 4K statements 371 for 8K statements	6ES5 371–0AA31 6ES5 371–0AA41 6ES5 371–0AA51	0.07 0.07 0.07
511 PU interface module*	6ES5 511-5AA12	0.3
512C Interface module* for computer, keyboard printer and CRT monitor	6ES5 512-5BC12	0.3
<b>302 Serial peripheral interface module*</b> (can be plugged into central controller)	6ES5 302-5AA11	0.3
<b>731 Cable connector*</b> between 670 PU and 511 IM	6ES5 731 – 00	
732 Cable sonnector between 512 IM and	6ES5 732-1000	
3914 keyboard printer (PT80, TTY)*	6ES5 732-2000	No.X
3964 Data transmission controller	6ES5 73230000	80.
3974 (TTY)* Alphanumeric display unit	6ES5 732-4000	
3974 R (TTY)* Alphanumeric display unit	6ES5 732-5000	
512 Interface module (S5–S5 interface TTY)	* 6ES5 732-6000	
3964 Data transmission controller*	6ES5 732-70000	
Length of 731 and 732 cable connectors		
,1 m	BBO	202
2 m	BCO	E.
4 m	BEO	
5 m	BFO	
10 m	CBO	
20 m .	CC0	
40 m	CE0	
80 m	C30	0
100 m	DB0	dr.
200 m	DC0	×
400 m	DEO	
800 m	000	
1000 m	EBO	
<b>736 Cable connector*</b> Length 3.20 m; for connecting a PT 80 (TTY) printer to the 670/675 PU	6ES5 736-0BD20	.0
737 Cable connector* Length 3.20 m; for connecting a printer (V.24) to the 670/675 PU	6ES5 737–0BD20	e de la
	10 M	1

Description .		Order No.	Weight approx. kg
	la *	- Ali	
consisting of:	IT."		
video monitor with UV e	rasing unit and	\$	
printer interface		Nº.	
German labelling		6ES5 670-0CA21	20
English labelling		6ES5 670-0CB21	
French labelling	~302	6ES5 670-0CC21	200
675 programming unit	* 🚫	· · · ·	Ś
consisting of:			
ideo monitor with print	er interface but	CECE CZE OLIA11	10
without UV erasing unit		0255 0/5-00ATT	10
Mounting rack		6	
with 8 module location	S	6ES5 710-0SA11	1.53
with 16 module location	S	6ES5 /10-05A41	2.56
Cable connector, shield	ding		
between CC and I/Os, I	0.9 m	6ES5 716-0AK00	25
between CC and I/Os, between CC and I/Os	1.5 m	6ES5 716-08850	3
	2.0 m		21
Cable connector, shiel	ded	SESE 717 00100	
between snort mounting	g racks, ປ.8 m	0E22 / 1/ - 0B100	
Cable connector, shield between extra-long mou	ded unting racks, 0.5 m	6ES5 718-0AF00	
Input modules, each w	vith 8 inputs	B	
Digital input module	24 V DC	6ES5 400-7AA13	0.4
Digital input module wit	ь — — — — — — — — — — — — — — — — — — —		1.50
aroup signal	24 V DC	6ES5 401-7AA13	100
Digital input module	115 V AC/DC	6ES5 405-7AB11	10.
Digital inpat incadio	220 V AC/DC	6ES5 405-7AB21	
	48 V AC/DC	6ES5 405-7AB31	
Output modules, each	with 8 outputs		
Digital output module	24 V DC, 2 A	6ES5 410-7AA11	0.68
	48 V DC, 0.5 A	6ES5 410-7AA21	
	115 V AC, 2 A	6ES5 415-7AB11	
×0 1	220 V AC, 2 A	6ES5 415 - /AB21 6ES5 415 - 7AA31	10,
P. I	0 V AC/24 V AC, 2 A	0E35415-7AA31	
Relay output module	o 30 V AC/DC/500 mA	6ES5 417-74411	07
up a	to 250 V AC/DC/1.5 A	6ES5 417-7AA21	0.7
777C Samiaa unit*		22	
without connector		6ES5 333-0AC21	3.0
Standard function blo	cks	P71200-40121-	
for 333C service unit, o	n mini-diskette	A253-04	
Eucos for		Ser.	
output modules	220 V AC, 6 3 A fast	261 312 GWA	
	115 V AC, 6.3 A fast	261 312 GWA	25
	24 V DC, 2.5 A fast	261 131 GWA	30
Power supply blocks		, A	
220	0/240 V AC, 0.8 A slow	256 263 GWE	
	115 V AC, 1.6 A slow	256 255 GWE	
Power supply module	S		
for external 24 V supply			
22	U V AC/24 V DC; 0.8 A	6ES5 931-7AA11	0.7
	5 V AC/24 V DC; U.8 A	0E33 331-/AAZ1	0.7
Back-up battery (Li) 3.	4 V 🔊	6ES5 980-0AA31	.30
			and the second se

\* Order from GWK

# 6. Maximum I/O configuration



Fig. 27a Maximum configuration of the I/Os with extra-long mounting racks and addressing of the input/output modules.



Fig. 27b Maximum configuration of the I/O modules with short mounting racks and addressing of the input/output modules.

# SIEMENS

Order No. GWA 4NEB 807 2121 – 02 Printed in the Federal Republic of Germany AG 07830.3 E 32 en

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